Design of a low cost BPSK modulator/demodulator for a practical teaching of digital modulation techniques

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Abstract : Teaching the digital transmission techniques- like other fields of electronic- is not always easy : There is classically theoretical courses and practical lessons. The link between the two is often the most important difficulty that appears for the students. An abundant literature on digital wireless, including high mathematical level approaches is available; since a few years, theoretical courses are easily illustrated by the 2D computer simulations. But simple descriptions or analysis are rarely found and simulations do not replace a concrete true design. In order to improve the efficiency of our teaching, we present here a practical and pedagogical low cost BPSK modulator/demodulator model kit to teach modulation during practical lessons.

Keywords : digital transmission and modulation, BPSK, education, practical lessons,

1 Introduction

Since a few years, we observed some major changes in student's behaviour in our engineer school: They are less interested in theory and "reject" all courses which have no concrete application. So, one of our challenge is how to motivate these new students generation to the fundamental courses. Moreover, even if simulations tools like SIMULINK are helpful and "funny to use", they do not fit perfectly the behaviour of a true circuit. The use of an intuitive and practical approach seems to be more efficient than traditional courses for these students. The job we present here is a try to create a didactical link between theoretical course and practical lesson. The example of a hand made low cost BPSK modulator/demodulator is used to illustrate this approach.

This kit is used by students during practical lessons without necessity of expensive and sophisticated test equipment. The schematic diagram and pictures are given and explained in the next paragraph.

2 Digital modulations background

2.1 Generalities

A complete digital radio link is a complex system [1], [2], [6], [7] which consist of several main blocks as indicated on the figure 1. The subset which interests us here is the modulator/demodulator on intermediate frequency. Among all the possible numerical modulations, we chose to start with the students, by simplest ie BPSK modulation.
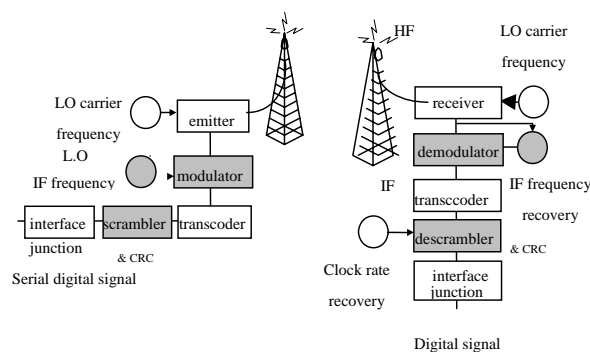

Fig 1 : Digital transmission block diagram

2.2 BPSK modulation principle [3]

Modulation BPSK (Binary Phase Keying Shift) consists of a phase modulation with 2 possible states of the intermediate frequency by a serialized numerical signal. Like there is, neither relation of phase nor of frequency between the Intermediate Frequency and the modulating signal, one synchronizes this one on the IF by a simple D latch. After a translation of level (centred on 0V), the synchronized modulating signal and the FI, is applied to an analogue multiplier. (Fig 2)
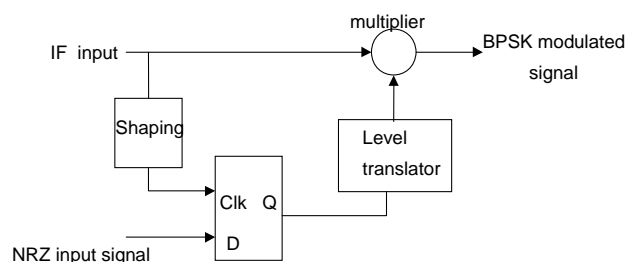

Fig.2 : Modulator principle

This allows obtaining a modulated signal with two states of phase 0° and π. The phase shift then occurs when the IF modulated signal crosses zero. Without the preliminary synchronization of signal NRZ, the phase shifts would happen in a random way compared to the carrying signal and would have a harmful effect on the spectrum (more marked transitions).
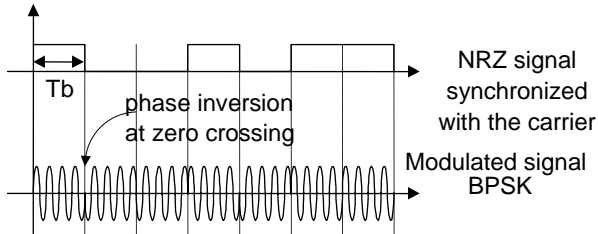

Fig 3 : Modulation BPSK

The shape of the modulated signal spectrum looks like a classical cardinal sinus $A.\left(\dfrac{\sin(\pi f.Tb)}{\pi f.Tb}\right)$ centred on IF frequency as indicated in figure 4.
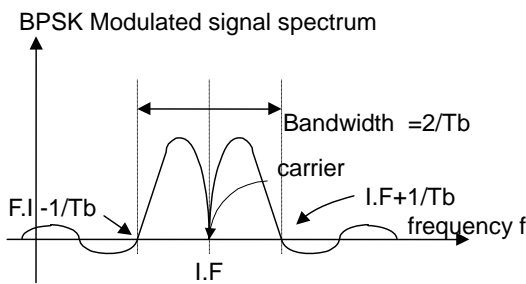

Fig 4 : BPSK modulated signal spectrum

Around 90% of the total energy is contained in the main lobe.

2.3 BPSK demodulation principle

The demodulation is known as coherent when that one has with the reception a local oscillator synchronized in frequency and phase with the emitted frequency.
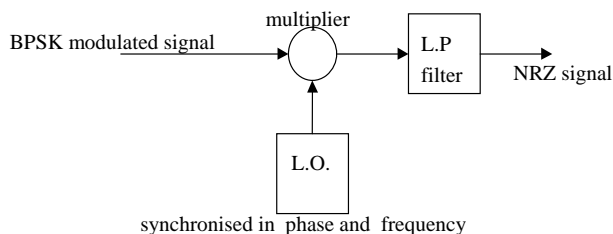

Fig. 5 : Demodulator principle

One can point out shortly the operation of the demodulator. The output voltage of the LO is written:

$$V_{ol} = A.\cos \omega t \quad (1)$$

The received signal is:

$$B.\cos \omega t \text{ or } B.\cos (\omega t + \pi) \ (2)$$

The signal delivered by the multiplier is:

$$A.B.\cos \omega t .\cos \omega t \text{ or } A.B. \cos \omega t .\cos (\omega t + \pi) \ (3)$$

From trigonometrically formulas:

$$\cos a. \cos b = 1/2.(\cos (a+b)+\cos (a-b)) \ (4)$$

it yields :

$$1/2 \ A.B. \ ((\cos 2\omega t) +1)) \text{ or}$$
$$1/2 \ A.B \ ((\cos 2\omega t) -1)) \ (5)$$

The low pass filter suppresses the harmonic 2ω.

We obtain then at the output a two level signal: 1/2 AB and -1/2A.B corresponding to the two level of the NRZ emitted code.

To demodulate the signal, it is obviously necessary to reconstitute locally the carrier wave one not presents in the emitted spectrum. That can be carried out according to two principles: rise squared in carrying or Costas loop [10]: we chose to use the first, simpler of approach, the Costas loop being approached in a more complete handling on modulation QPSK. The signal modulated received BPSK is applied simultaneously to the 2 entries of a multiplier. At the output, one finds the product:

$$\text{Cos}^2\omega t \text{ or } \text{Cos}^2 (\omega t + \pi), \text{ depending on carrier phase.}$$

As $\text{Cos}^2 a = (1+\cos 2a)/2$, it results from it a DC voltage and a signal at frequency 2ω without phasing. A simple filtering and a division by 2 are enough to restore locally the carrier wave in phase with the emitted IF carrier.

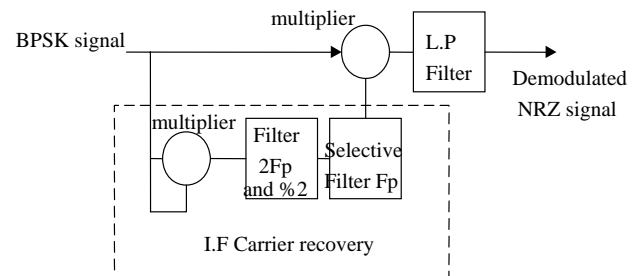The corresponding block diagram is given in figure 6.

Fig.6 : IF carrier recovery principle

2.4 Practical design

To simplify the design and to reduce the costs of realization, we chose to work at the standard frequency of 455 Khz, with an adjustable binary rate from 10 to 20 kBits/s. The use of integrated circuits of

the trade traditional easy to supply ensures the perennially of our models and an easy maintenance service.

2.5 General schematic diagram
The board consists of a pseudo random pulse train generator which can (or not) be integrated in a FPGA. This generator drives the IF 455 kHz modulator whose essential component is an analogical multiplier AD 835.

The 455kHz carrier wave is generated by a sinusoidal integrated oscillator MAX038 which can be possibly replaced by an oscillator with door and with ceramic resonator 3,64 MHz, a divider by 8 with D latches and one ceramic filter narrowband, tuned on 455 Khz, for more stability.

The modulator is directly connected to the demodulator primarily made up of a multiplier AD835. The recovery of carrier frequency is it also based on multiplier AD835 wired as a squared associated with a divider by 2 and one filter ceramic SFZ 455 A. The demodulated signal is given in form by a fast comparator AD790 then a simple logical gate.
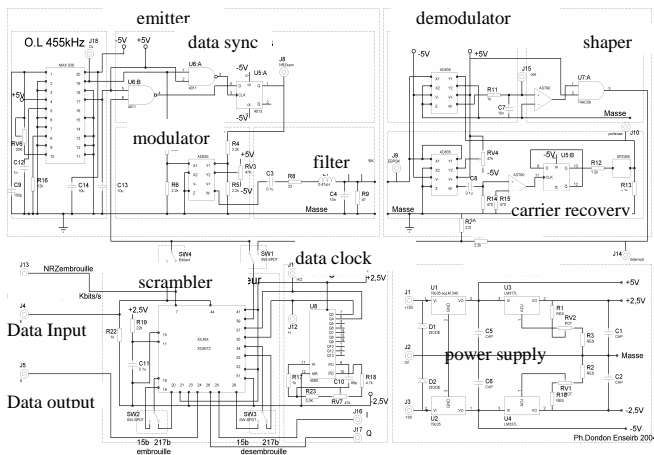
Fig 7 : Schematic diagram

Because of the differences in power supply voltages between circuits, a voltage level adaptation is necessary between Xilinx and the other circuits.

In the two following paragraphs, we detail the constitution of the blocks integrated in a CPLD.

2.6 Pseudo random pulse train generator
In order to observe the characteristics of the modulated signal, we included in the design, a digital pulse train generator [4] which simulates the data to be transmitted, based on the following diagram of figure 8.
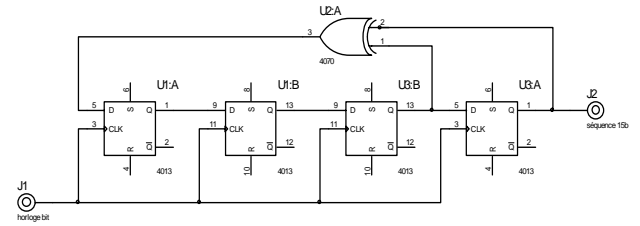
Fig 8 : Pseudo random generator principle

The more important the number of D latches used is, the longer the random pseudo sequence will be and the spectrum observed nearer to reality. In our case, we used 8 D latches and a sequence of 219 bits was selected. Its length is sufficient to obtain a "quasi" continuous spectral concentration. The generator can be designed starting from discrete D latches or integrated in a small standard XILINX XC 9572 programmed under "HDL designer" for example.

2.7 Scrambler /Descrambler
To better match the reality of a modulation system, we integrated a scrambler/descrambler whose role is double: to code information and to increase the number of transitions in the signal to facilitate the recovery of the binary rate in the receiver.
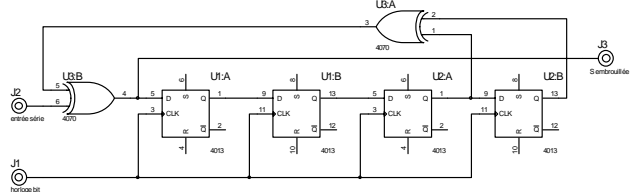
Fig 9. : Scrambler and generator

On the example of figure 9, the equation of the muddled exit M after the nth period of clock H (D latches numbered from 1 to 4, from left to right) is given by:

$$M(n)= E(n) \oplus [Q3(n) \oplus Q4(n)] \ (6)$$

or :

$$M(n) = E(n) \oplus [Q2(n-1) \oplus Q3(n-1) \ (7)]$$

Then :

$$M(n) = E(n) \oplus [Q1(n-2) \oplus Q2(n-2)] \ (8)$$

And finally :

$$M(n) = E(n) \oplus [M(n-3) \oplus Q1(n-3)] \ (9)$$

Where E is the input and Qn, are the outputs of the different latches.

It yields:

$$M(n)=E(n)\oplus [M(n-3)\oplus M(n-4)] \quad (10)$$

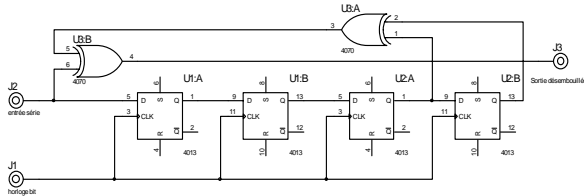The descrambler looks almost like the scrambler (figure 10).

Fig 10 : Descrambler

With M applied to the input of the descrambler, we can write the logical equation at the nth period of clock between the output S and the input :

$$S(n)=M(n)\oplus [M(n-3)\oplus M(n-4)] \quad (11)$$

If we associate the two circuit scrambler/descrambler, we obtain the logical equation:

$$S(n)=M(n)\oplus [M(n-3)\oplus M(n-4)] \quad (12)$$

With:

$$M(n)=E(n)\oplus [M(n-3)\oplus M(n-4)] \quad (13)$$

And it comes:

$$S(n)= E(n)\oplus [M(n-3)\oplus M(n-4)] \oplus [M(n-3)\oplus M(n-4)] \quad (14)$$

Finally :

$$S(n)= E(n) \quad (15)$$

The descrambler-scrambler system is known as auto synchronizing: After a maximum of n period, (with n = a number of latches stages, here 4), the system is locked and the exit of the descrambler restores the signal accurately. The unit must be correctly initialized with the powering to avoid any blocking of the D latches.

2.8 Gaussian filtering
The Gaussian filtering of the numerical train before modulation normally requires a DSP and a sophisticated algorithm. For reasons of cost, one can advantageously replace this filtering by an integrated filter for example of the 8th order, called of "improved Bessel" [8] to which the effect will be very close on the spectrum to the transmitted signal. For teaching questions and of facility of provisioning of the components, we propose also a simple filter RC which will already make it possible to the pupils to include/understand and compare the effect of these filters on the signal and the obstruction spectral. The selection of one or other filter is done by a simple switch.

2.9 Main components
For information, we give the list of the principal components and their suppliers:

AD835   multiplier Analog Devices
SFZ 455 A   ceramic Filter Murata
MAX038   oscillator Maxim
XC 9572   Xilinx
AD790   comparators Analogue Devices
LT 1164-7 (linear phase filter) Linear Technology
CD 4060, CD 4013, 4011 latches and gates
LM 7805, 7505, 337 et 317 power supply regulator

3 Experimental
The experimental results that we give here are those which the students can do during the practical lesson, on our BPSK board. A simple oscilloscope equipped with FFT function, or an oscilloscope and an analyzer of spectrum are enough for the practical observations of Work. Figure 11 shows the chronograms raised with an oscilloscope Agilent "Megazoom" mixed analogical numerical, in run/stop mode synchronized on the data flow. The phase shift is well observed in the passing to zero of frequency FI.
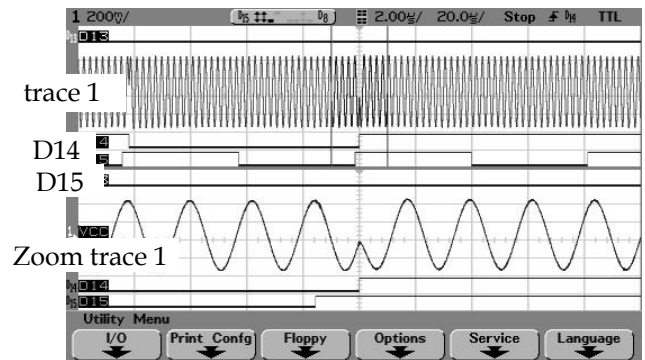

Fig 11 : BPSK modulated signal BPSK

Trace 1 : IF 455 kHz modulated
D14 :   random pulse train 11Kbits/s ,
D15 :   bits clock 11 KHz
Zoom Trace 1 : phase shift with D14 changes

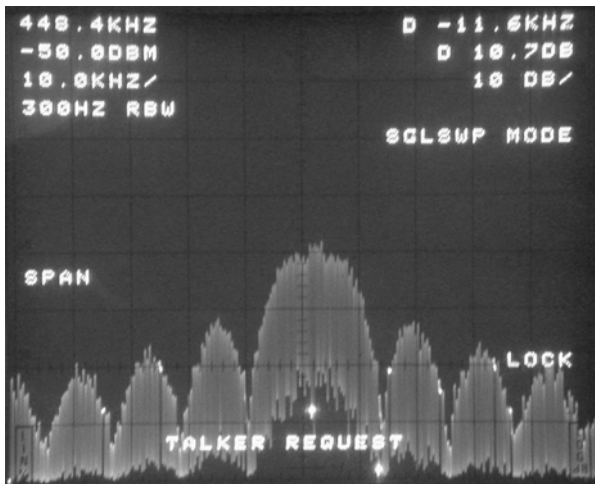The spectrum of the modulated carrier is given in figure 12.

Fig 12 : Modulated signal spectrum (Tek 2712)
Horizontal scale : 10kHz/div

One checks on figure 13, the widening of the principal lobe proportionally to the increase in the baud rate [9].

Fig 13 : BPSK spectrum with a 24Kbits/s baud rate and IF 445 kHz (Horizontal scale : 20kHz /div)

Then, one checks by bringing into service a simple R,C filter, on the bit stream 24Kbit/s (figure 14), the reduction of the secondary lobes. This observation has only a pedagogical goal, that to show the impact of filtering on the spectrum width of the modulated signal.
As already indicated this filtering is naturally far from sophisticated Gaussian numerical filtering really used but is sufficient from a teaching point of view.

A filtering closer to reality can, at this step, be introduced on the electronic board by "switching on" the improved Bessel 8 th order filter LT 1164-7.

Fig 13 : Spectrum with a simple R ,C filter

The modulating signal then takes the form given on figure 14 (run/stop mode, infinite persistence), and the lobes secondary become almost non-existent.
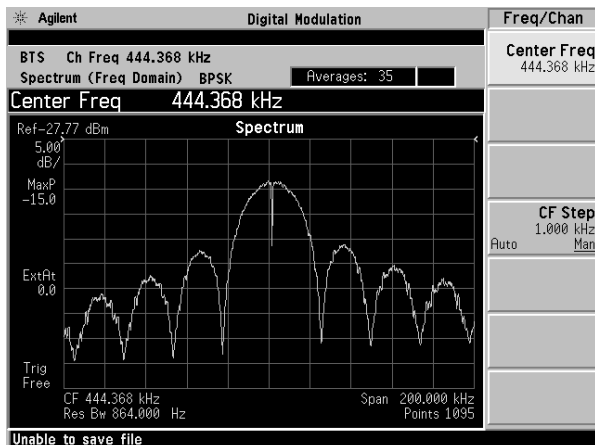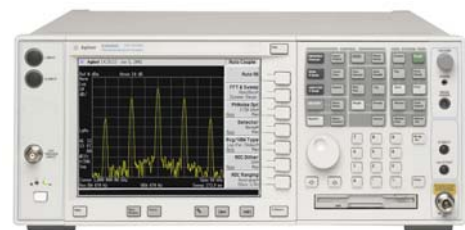

Figure 14 : Digital signal after   8th order Bessel filtering (cutoff frequency tuned at 9kHz)

Lastly, if an expensive test equipment such as vector signal analyzer (Agilent E4443 for example [5]) is available, one can visualize, the phase diagram, and the eye diagram (figure 15, 16,)

Figure 15 : Analyser E4443

The "widening" of points 0° and π testifies of phase vibration on modulating signal NRZ due to the electronic circuits.
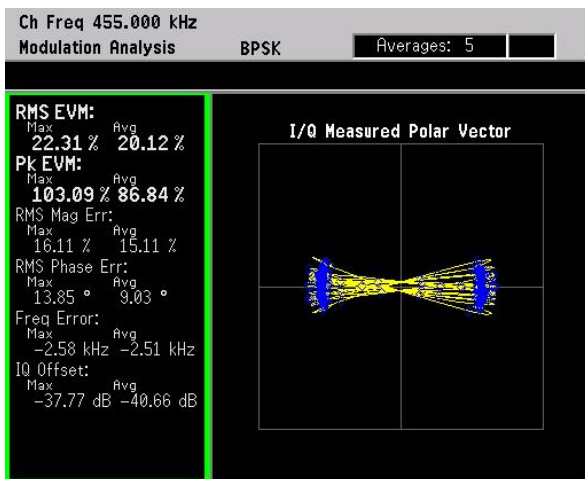
Figure 16 : BPSK vector analysis

According to the operating mode of the analyzer, one can visualize (figure 17) the eye diagram (to be compared with figure 14), the constellation and the parameters of amplitude and phase errors in the same window.
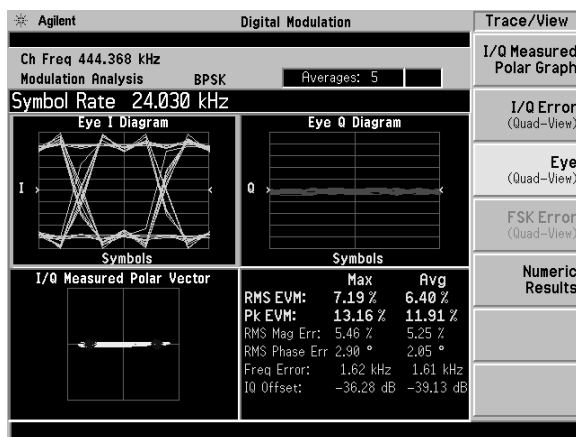

Fig. 17 : Eye diagram

In the opposite case (no vector analyser available), the constellation can also be observed on a simple oscilloscope in X,Y mode.

4. Possible improvements

The design and the use of these low cost models , (cf photograph of figure 18) constitute above all, an initiation with the numerical modulation and a practical complement with the theoretical lesson: the reaction of the receiver in the presence of a noisy transmission channel, the measurement of error rate and the oscillators jitter, the extraction of the binary rate (clock recovery) in reception are currently not presented on the model, but that can constitute an evolution or a later possible extension.

5. Conclusion

We showed that with reasonable techniques and financial tools 1 (as well in the field of the components as the equipment measurements), it is possible to create a very cheap practical lesson which illustrates perfectly the modern concepts of digital transmission of information. In complement of the traditional courses and work on standard simulator MATLAB which makes it possible to simulate complete connections, Our models complete the "often difficult transition" between abstract and concrete with which our students are confronted during their schooling.

After this experiment, we are introducing, and on the same way, "hand made" board for QPSK modulation/demodulation with Costas loop, and soon FSK which will supplement the "numerical communications" lessons given in ENSEIRB.
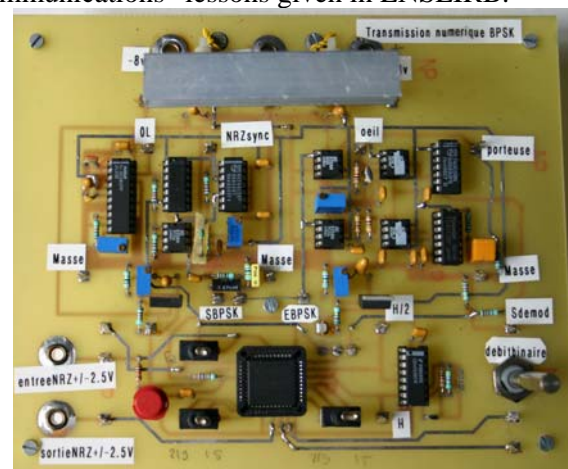

Figure 18 : BPSK board view

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