Low Glitch Current-Steering DAC with Split Input Code

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Abstract: - In this paper we will offer a solution for a current-steering DAC in standard CMOS technology which presents an important innovation as the voltage reference does not represent a distinct block, but it overlaps the functional diagram of the converter. The splitting in two equal parts of the digital input code applied to the converter will drastically diminish the number of large dimension transistors used in the current sources of the converter. By forcing the same potential to the complementary output of the converter as to its main output, we efficiently reduce the glitches that appear during the switching.

Keywords: current-steering DAC, sub-bandgap voltage reference, split input code, glitches.

1 Introduction

The natural tendency in portable equipments manufacturing is that their supply voltages become lower and lower. Furthermore, in the field of analog and mixed integrated circuits one of the most accessible technological processes in terms of price is the standard CMOS process.

Taking into consideration these two aspects, the majority of the works which deal with the subject of Nyquist frequency DAC-s design suggest the use of a reference voltage source which must be able to work at these low supply voltages. Thus, CMOS sub-bandgap reference voltage sources have been developed [8], [10], [11] and obviously they provide an output voltage lower than 1.2V.

The most widespread types of Nyquist frequency DAC-s are current-steering DAC-s, a statement sustained by recent works, such as [1], [2], [4], [5]. For these types of converters, exact theoretical models have been elaborated and they allowed an easy evaluation of their static and dynamic performances [5], [6]. Here, the bandgap voltage source is attached to DAC either as a distinct integrated circuit or it is integrated in the same chip next to the converter as it is presented in [1], [2], [3], [4].

In section 2 of this paper we will show how the sub-bandgap source and the DAC can be joined in a single, inseparable circuit, as we suggested in [7], which will benefit of the qualities of both circuit types.

A 10-bit current-steering DAC overlapping a sub-bandgap voltage reference will be controlled by a split digital input code (2×5b) which will allow a drastic diminishing of the number of unit current sources used in his block diagram. Moreover, we will present a method for an efficient reducing of glitches that appear when a new control code is applied to the converter.

Section 3 will conclude the paper.

2 Current Steering DAC with Embedded Voltage Reference

2.1 Sub-Bandgap Voltage Reference

The sub-bandgap voltage reference used as starting point in our work was designed according to [9] and it is presented in fig.1. In our simulations we used PSPICE models of 0.35μm CMOS process and of course we used pnp-lateral transistors instead of npn transistors like in the BiCMOS design of [9].

The minimum input common-mode voltage of the operational amplifier must be less than one V_{EB} and, as it was explained in [10], the input stage can't be built with nMOS transistors because, especially at high temperatures, the necessary condition $V_{EB(ON)}>$ $>V_{thn}+2V_{DS(sat)}$ can no longer be accomplished in any CMOS technology (V_{thn} is the threshold voltage of an input nMOS transistor and $V_{DS(sat)}$ is the minimum

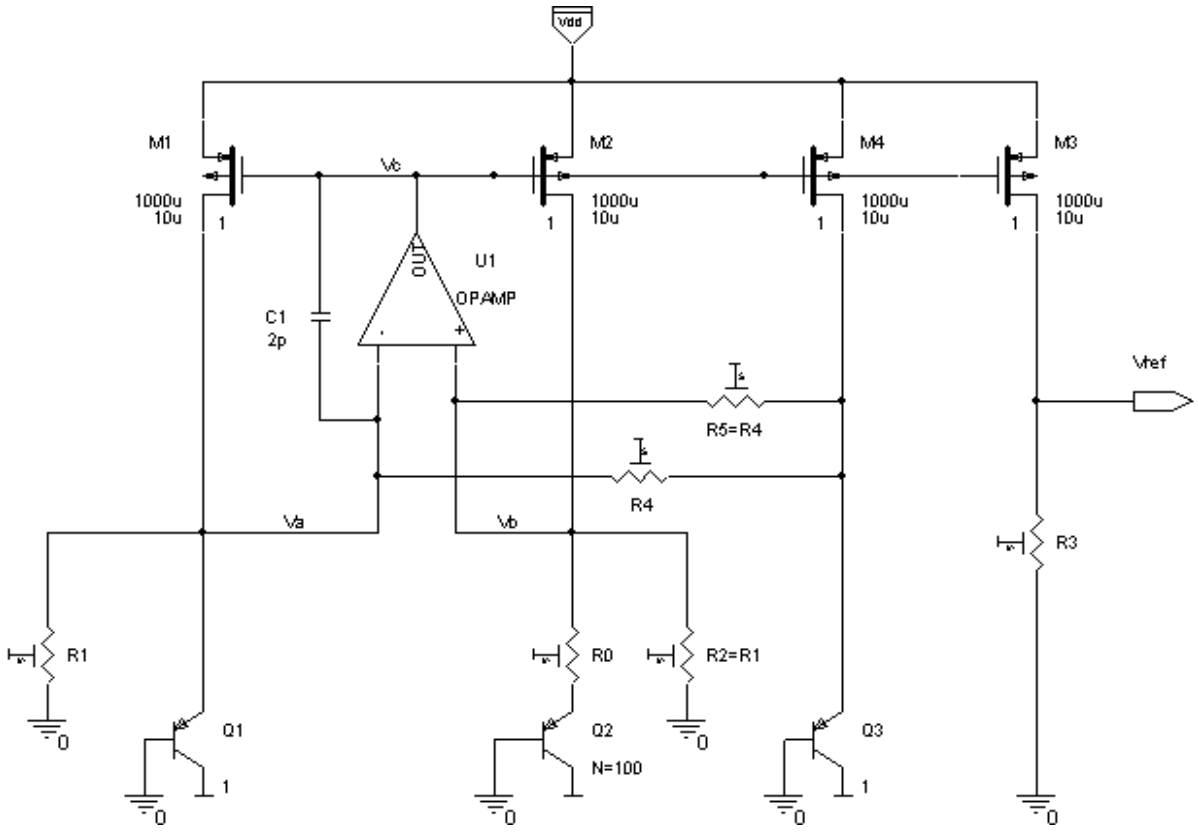

Fig.1 Sub-bandgap voltage reference with curvature compensation

voltage across the current source connected in the common sources of input transistors).

In this case we must use pMOS input transistors in the differential stage of the operational amplifier and the minimum supply voltage will be $V_{DDmin} \geq \geq V_{EB(ON)}+|V_{thp}|+2|V_{DS(sat)}|$. Unfortunately this means that $V_{DDmin} \geq 1.5V$ (i.e. 0.5V grater than in [9]).

The output voltage of the circuit shown in fig.1 presents a curvature compensation of the V_{EB} temperature dependence and is given by the equation (1):

$$V_{out} = \frac{R_3}{R_1}\left[V_{EBQ1} + \frac{R_1 \ln(N_E)}{R_0} V_T + \frac{R_1}{R_4} V_T \ln\frac{T}{T_0}\right] = \frac{R_3}{R_1} V_{BG} \quad (1)$$

where $N_E = 100$ is the ratio of emitter junction areas of Q_2 and Q_1, V_T is the thermal voltage, $\frac{R_1 \ln(N_E)}{R_0} = 23$ and $R_4 = \frac{R_1}{\eta - 1}$, with η depending on the bipolar structure ($\eta \cong 3.5$ in our design); $T_0 = 300K$. In the square brackets the second term represents the first order compensation of temperature dependence of V_{EB} and the third term represents the nonlinear compensation. As we can see from (1), the bandgap voltage of 1.2V can be weighted by the ratio R_3/R_1 and if R_3 is small enough, very low reference voltage values can be obtained.

In fact this circuit produces currents proportional with V_{EB}, V_T and with the nonlinear term from V_{EB} temperature dependence, that are weighted, summed up and injected in the resistor R_3.

For example, imposing the value of the output voltage $V_{out}=(2^{10}-1)\times 0.5mV=511.5mV$, and adopting $N_E=100$, $R_1=R_2=80k\Omega$, $R_0=18.13k\Omega$, $R_3=35.11k\Omega$ and $R_4=R_5=32.5\ k\Omega$ we obtained by simulation the output voltage of the circuit as a function of temperature which is presented in fig.2. As we can see, the variation of the output voltage is only 0.5mV when the temperature changes from -30^0C to 100^0C (curvature compensation). This variation is 1mV for a first order compensation only (in the absence of resistors R_4 and R_5).

2.2 Block diagram of proposed DAC

As it was shown in subsection 2.1, the sub-bandgap reference taken into consideration allows us to obtain a current independent of temperature which is mirrored in the last branch of the circuit and injected in the resistor R_3 (see fig.1).

As we presented in [7], a way to obtain a programmable output voltage is to mirror the output current of the reference in more branches through which the currents are switched or not towards the resistor R_3 of constant value. Instead of the last

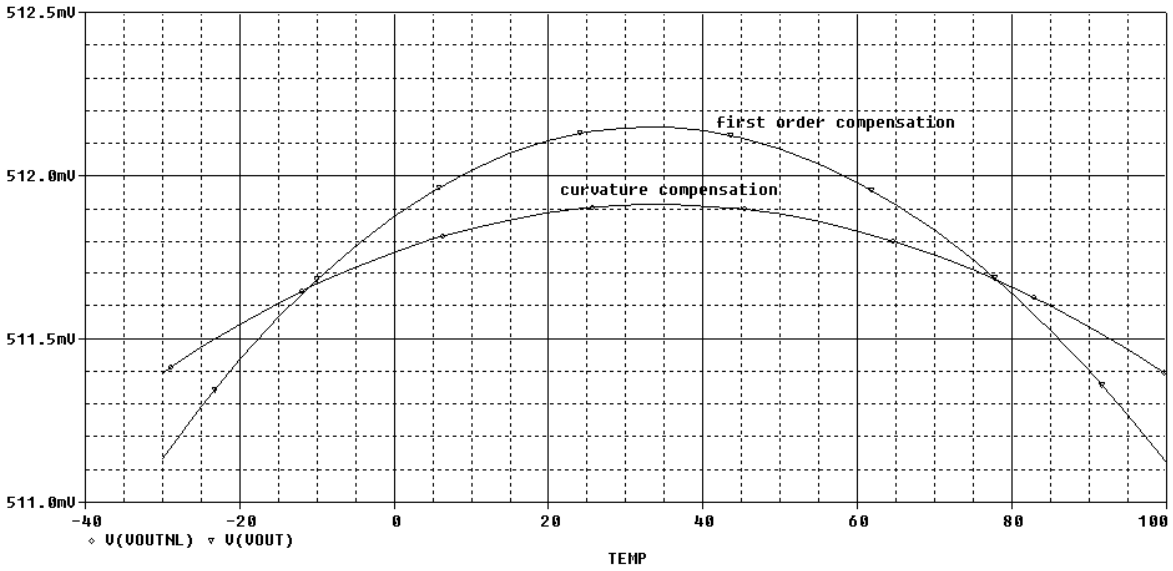

Fig.2 Simulated sub-bandgap voltage as a function of temperature with first order compensation and with curvature compensation

branch M_3 from fig.1 we add 2^N-1 unit current sources controlled by N switches in such a way that the LSB will control a single unit current source, the next will control two unit current sources, while the MSB will control 2^{N-1} unit current sources.

In order to avoid a sudden current step on the switched current sources we must ensure dual, complementary current outputs. Thus, the currents corresponding to the digital input code as well as those which will not contribute to the output voltage manufacturing will be summed up in two distinct nodes and will be led through equal value resistors R_3 towards the ground.

As both the current sources block and the resistor R_3 belong equally to the voltage reference and to the converter or, more precisely, because, in fact, the whole converter is included in the sub-bandgap mechanism, we obtained a single, inseparable circuit resulted from the overlapping of the two types of circuits.

The major disadvantage of this type of converter is that it uses a very large number of pMOS transistors. The number of the transistors which make up the unit current sources (which have to be of large dimensions in order to ensure a perfect equality of unit currents) is 2^N-1. For example, if N=10, we must use 1023 transistors.

Our solution implies the splitting into equal parts (for an even number of bits) of the digital input code applied to the converter. In these conditions, we will have two identical blocks. Each block will be controlled by N/2 bits and will contain $2^{N/2}$-1 unit current sources. In order to ensure the weighting of $2^{N/2}$:1 in the output voltage contribution, the nodes in which the currents of the two blocks will be summed up are connected as shown in fig.3. The ratio of resistor values R_8 and R_9 (which replace R_3), respectively R_{10} and R_{11} (for the complementary output) must be $2^{N/2}$-1. This will drastically diminish the number of large dimension transistors used in unit current sources. For example, if N=10, we must use only $2\times(2^5-1)=62$ transistors.

In fig.3, the delimitation between the blocks "Sub-BG" and "I_block" is purely formal and it was adopted for optimising and organising the block diagram of the converter on hierarchical blocks.

As follows, we note the equal currents through the two first branches of the block "Sub-BG", I_{BG}, (identical with those from fig.1) and the currents generated by the unit current sources I_u. The transfer function of the 10-b converter will be:

$$V_{out} = 1{,}2\frac{I_u}{I_{BG}}\left(\frac{R_8}{R_1}\sum_{i=0}^{4}A_i 2^i + \frac{R_8+R_9}{R_1}\sum_{i=0}^{4}A_{i+5}2^i\right) =$$

$$= 1{,}2\frac{I_u}{I_{BG}}\frac{R_8}{R_1}\sum_{i=0}^{9}A_i 2^i = 1{,}2\frac{I_u}{I_{BG}}\frac{R_8}{R_1}2^{10}\sum_{i=0}^{9}A_i 2^{i-10} \quad (2)$$

Imposing the resolution of the converter to be 0.5mV and $I_u/I_{BG}=1/10$ ($(W/L)_u/(W/L)_{BG}=1/10$) the resulting values of the resistors R_8, R_9, R_{10} and R_{11} are shown in fig.3. The maximum output voltage of the converter is $0.5\text{mV}\times1023=511.5\text{mV}$ and it presents a temperature behaviour similar with that shown in fig.2.

The problem which is still to be solved is the effect of parasitic capacitance switching of the

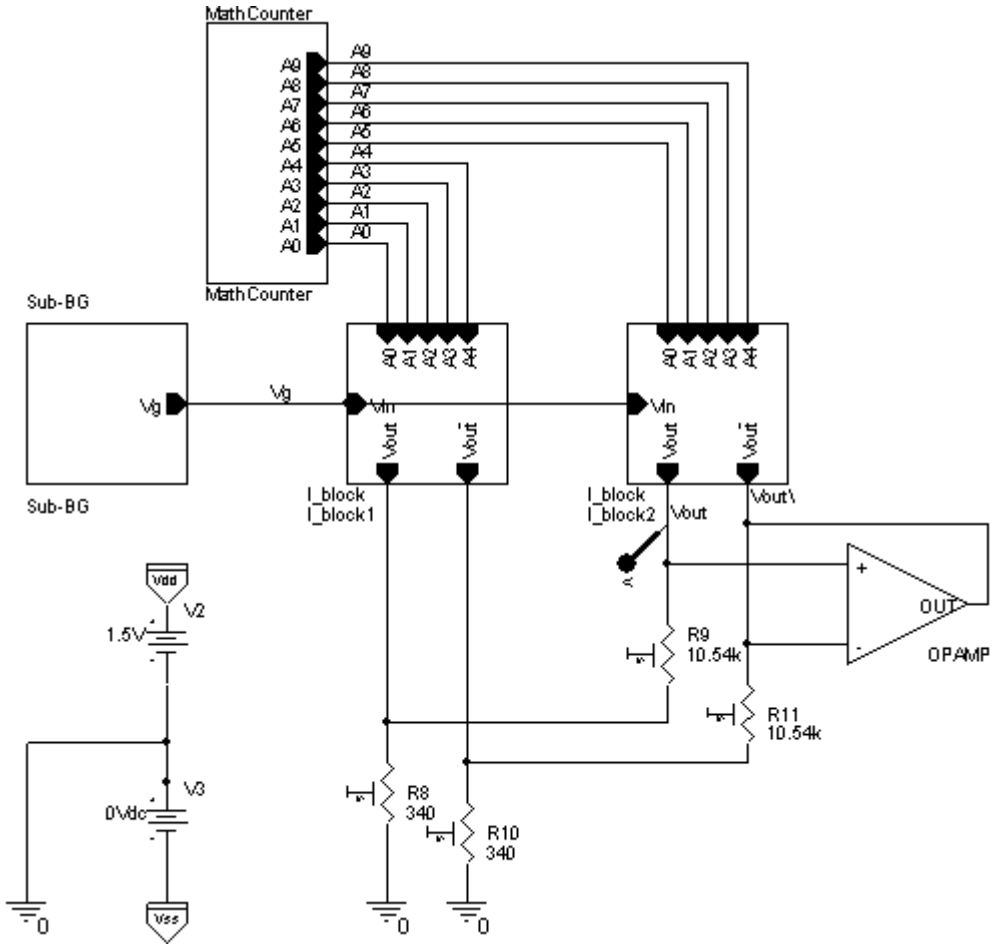

Fig.3 Block diagram of proposed DAC

current sources towards the nodes *Vout* anf *Vout* which don't have the same potential. For that, as we can see in fig.3, an operational amplifier was connected as follower with the inputs at the complementary outputs of the converter. This operational amplifier must be built with small dimension transistors because we need speed and because an input offset of 10mV, for example, leads to a non-critical voltage step during the parasitic capacitance switching.

The simulation results in the absence of the operational amplifier, respectively in its presence are presented in fig.4.a and fig.4.b. As we can see in fig.4.a the glitches are very big, especially when the counter changes from 2^k-1 to 2^k, with $5 \le k \le 9$. This happens because, in these cases, in "I_block2" 2^{k-5}-1 unit current sources are switched to *Vout* while other 2^{k-5} unit current sources are switched to *Vout* and their parasitic capacitance tries, for a very short time, to bring the previous potential Vout\ to the line *Vout*. We observe from fig.4.a that the amplitude of the glitches go to zero in the middle of the range of the digital input code. So, by forcing the same potential to the complementary output of the converter as to its main output, we efficiently reduce the glitches that appear during the switching, as we can see from fig.4.b. A detail of the biggest glitch as well as the settling time and the resolution of the converter can be observed in fig.4.c. The settling time is lower than 84ns in the middle of the range.

In our analysis we didn't take in consideration the mismatch error for the switch transistors and the influence of the bit skew (the timing errors have, usually, a standard deviation of approximately 5 percent [5]) so the energy of the glitch can be distributed for a longer period than in our case, but we can say that our converter works very well at 10MHz (a settling time of 100ns in the most unfavourable case).

3 Conclusion

In this paper we proposed a 10-bit current-steering DAC overlapping a sub-bandgap voltage reference. The converter is controlled by a split digital input code (2×5b) that allows a drastic diminishing of the number of unit current sources.

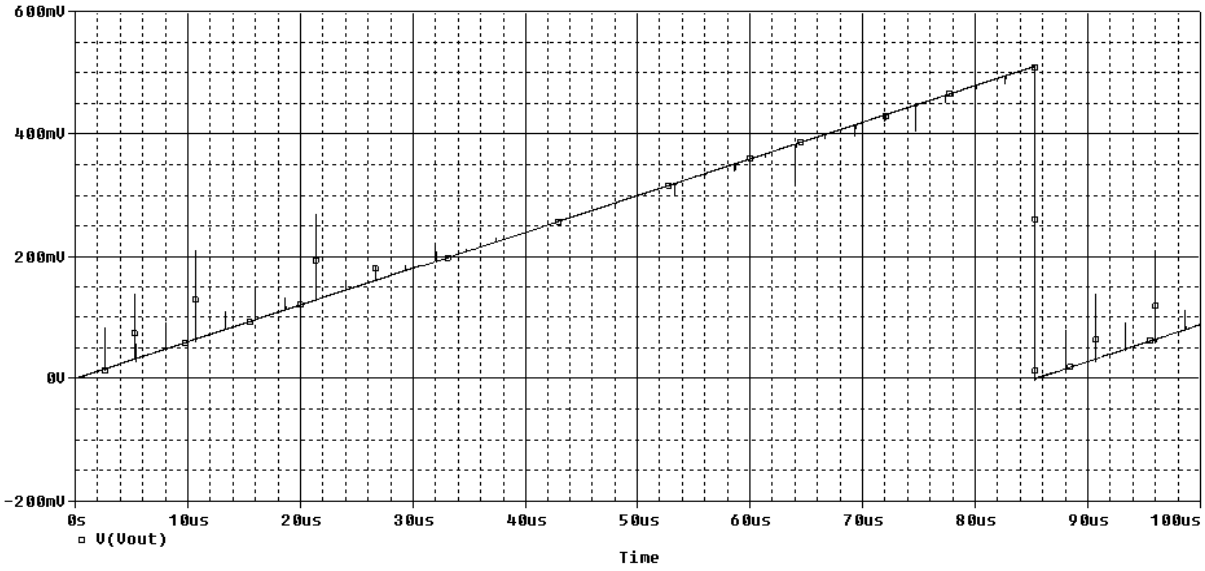

Fig.4.a Simulation results of DAC for all digital input combinations, without OpAmp

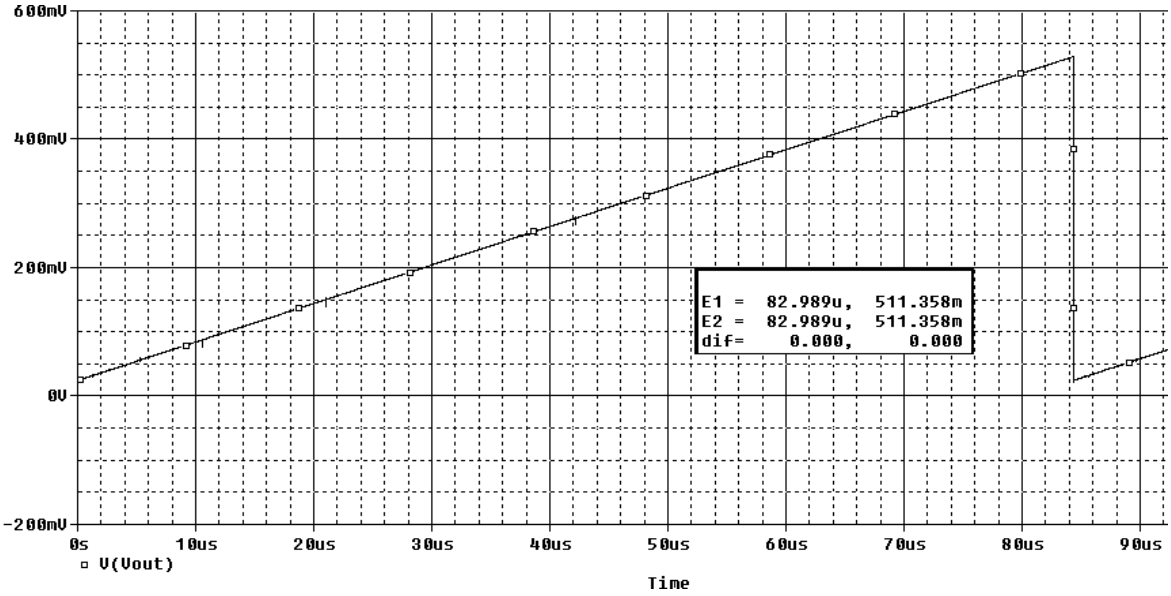

Fig.4.b Simulation results of DAC for all digital input combinations, with OpAmp

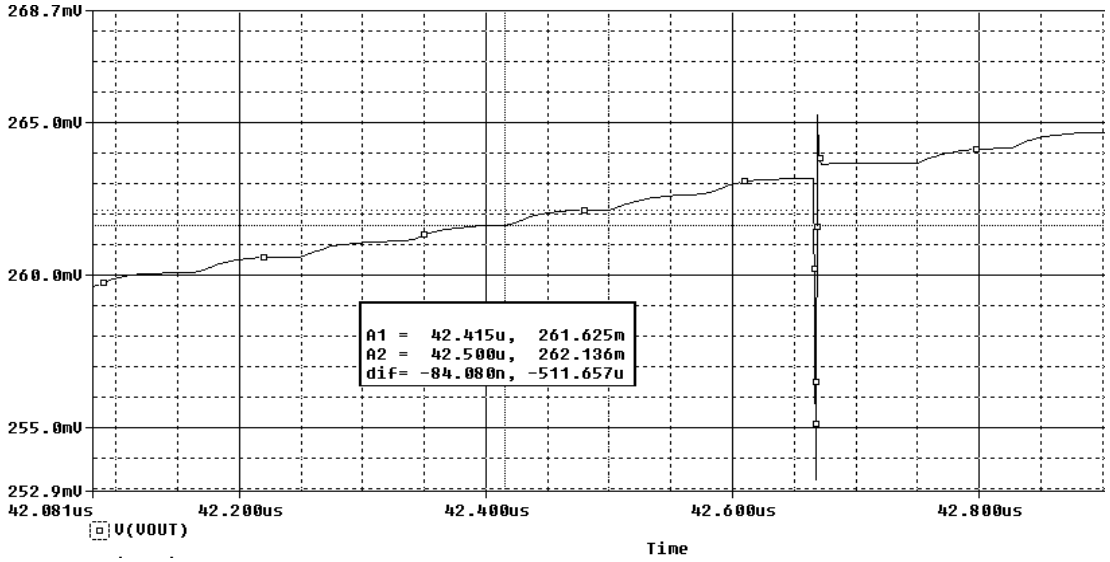

Fig.4.c Glitch detail of fig.4b; in window: settling time and resolution of the converter

Using an operational amplifier and forcing the same potential to the complementary output of the converter as to its main output, we efficiently reduced the glitches that appeared during the switching activity when a new digital input code is applied. We obtained by simulation a maximum settling time of 100ns for a supply voltage of 1.5V. The amplitude of the biggest glitch was 12mV.

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