

All-Optical Arithmetic Unit Based On The Hardlimiters

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Abstract:- The paper describes the design of all optical parallel adder and all optical arithmetic unit by using of a set of optical full adders and hard-limiters. The parallel adder and arithmetic unit are demonstrated via simulations and experiments. The optical Arithmetic unit can be used to perform a fast central processor unit using optical hardware components.

Key-Words:- Optical logic gate, Bragg grating, optical full adder, hard-limiters, optical processor, SOA.

1 Introduction

THE EMERGENCE of increasingly high speed, digital optical system, and optical processors demands an all optical arithmetic unit to performs a set of optical arithmetic micro-operations. The performing of signal processing operations entirely within the optical domain would exploit the speed and parallelism inherent to optics [1], [2].

Due to the lack of reliable optical logic devices, the signal processing technology used in current optical packet switched cross-connects and optical processor is based on a combination of electronic and optical technology. The all-optical arithmetic unit is carried out in electronics while the payload remains in the optical domain, where the over all operation is implemented using all-optical hardware components. .

All optical arithmetic units have many potential applications in optical communication systems and optical computing. All optical arithmetic unit can be realized by optical fiber delay lines, all optical full adders, and optical logic gates based on the hardlimiters.

In this paper we describe an all-optical circuit that performs parallel full addition of two binary optical words and could be used for applications such as packet header processing and used in the construction of optical central processor unit.

In general, this full binary adder function obviously adds to the range of digital optical processing capability that is required for optical computing [3].

The structure of the all-optical full adder is depicted in Figure 1 [1].

All optical Full adder logic circuit using three of limiters is shown in Fig. 1. It consists of three inputs (A, B, C) and Two outputs represent the Sum S and Carry out C_{out} [1].

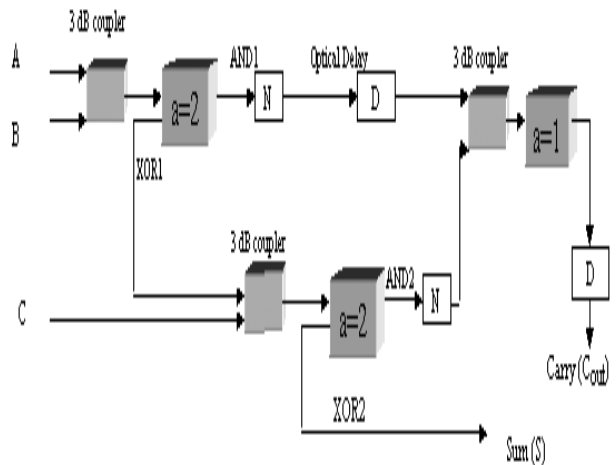


Fig. 1 All optical Full adder with three inputs(A, B, C) and two outputs (S, Cout)

Figure 2 illustrates the use of limiter in the construction of optical XOR and AND gates. Inputs A and B are first combined into a single beam. The transmitted intensity is defined as the O1 output and the reflected value as the O2. O1 yields the result of an AND operation and O2 the result of a digital XOR [1], [4].

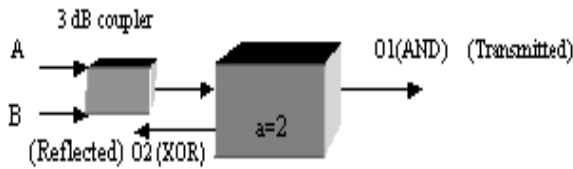


Fig.2. The structure of optical AND and XOR using optical limiter.

2 Operation Principle

The sum of two n -bit binary numbers can be generated in serial or parallel fashion. The serial addition method uses only one full adder and a storage device to hold the output carry [3], [5]. Each pair of bits is transferred one at a time through the single full adder to produce a string of output bits for the sum. The stored output carry from one pair of bits is used as an input carry for the next pair of bits [5].

The parallel method uses n full adders and all bits are applied simultaneously to produce the sum.

The paper introduces an 4 bit optical parallel adder. The all-optical parallel adder shown in figure 3 is implemented using four all optical full adder depicted in figure 1[1], and delay optical fiber to compensate the delay occurs by optical full adder in the next stages [1].

A binary optical parallel adder is an all-optical digital circuit that produces the arithmetic sum of two optical binary numbers in parallel. It consists of full adder circuits connected in cascade, with the output carry from one full adder connected to the input carry of the next full adder. The input carry to the parallel adder is C_0 and the output carry is C_4 .

The input carry in the least significant position is 0. Each optical full adder receives the corresponding optical bits of A and B and the input carry, and generates the sum bit for S and the output carry.

The output carry in each position is transferred to the input carry of the next-higher-order position. The output carry for each full adder is first fed to semiconductor amplifier (SOA) to be amplified and then fed to the next stage. The amplification by SOA ensures that the light injected to the next stage of full adder is sufficient to compensate the attenuation through the optical fiber.

Two 4 bits optical binary inputs A (A_3, A_2, A_1, A_0) and B (B_3, B_2, B_1, B_0) are applied to the all-optical parallel adder and the result of summation S (S_3, S_2, S_1, S_0) with output carry C_4 .

3 Results

The input pulses have a wavelength of 1552.9 nm and duration of 100 nanoseconds with optical peak power of 1 mW. Figure 4 shows the experimental waveforms of the optical binary input A (A_3, A_2, A_1, A_0). Figure 5 shows the experimental waveforms of the optical binary input B (B_3, B_2, B_1, B_0). The optical pulses to changes the state of parallel adder were injected every 100 nanosecond as shown in figure 4 and figure 5. The optical binary outputs S_3, S_2, S_1, S_0 , and C_4 are depicted in figure 6. All waveforms are scaled by arbitrary units and obtained using simulation computer aided design (CAD) of Beam PROP method version 5.0.

The optical outputs S_0, S_1 , and S_3 are delayed by optical delay element of 14.5 ns, 9.54 ns and 4.52 ns to compensate the full adder delays and obtain all optical summation outputs at the same instant.

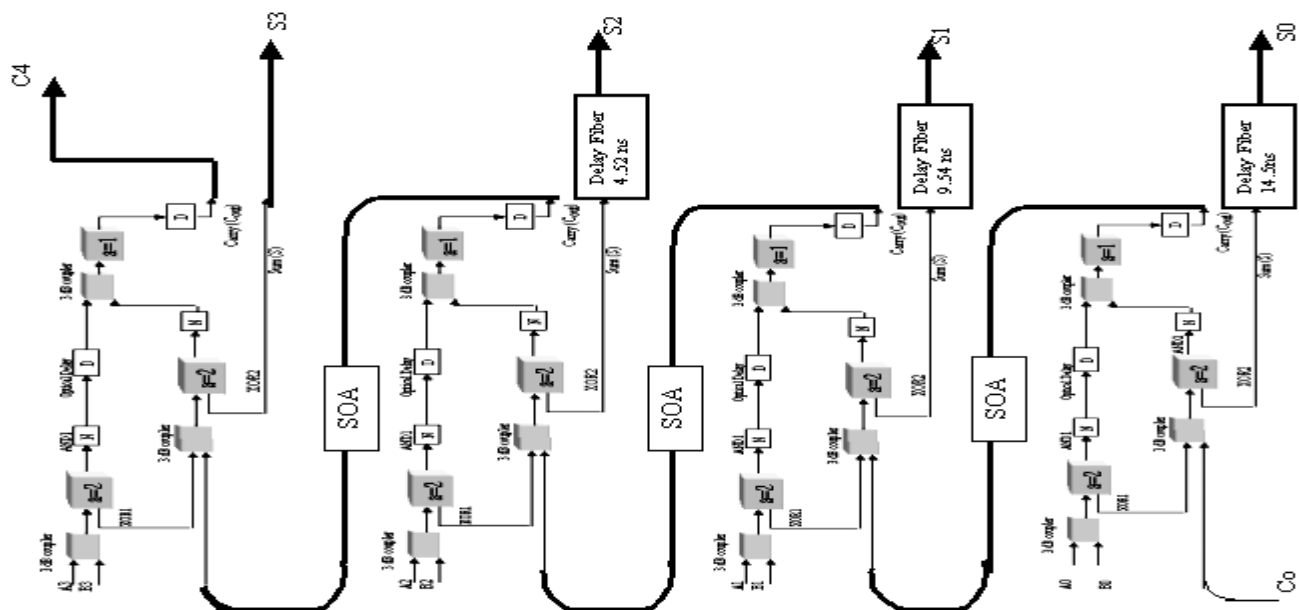


Fig 3 All-Optical 4 bit parallel adder using 4 all-optical full adders based on hardlimiters.

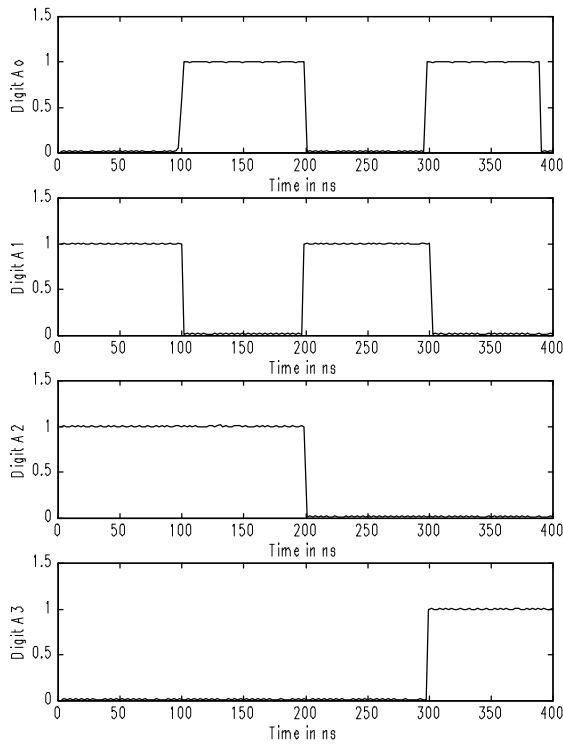


Fig4. Optical waveforms of input binary digits A_0 , A_1 , A_2 , and A_3

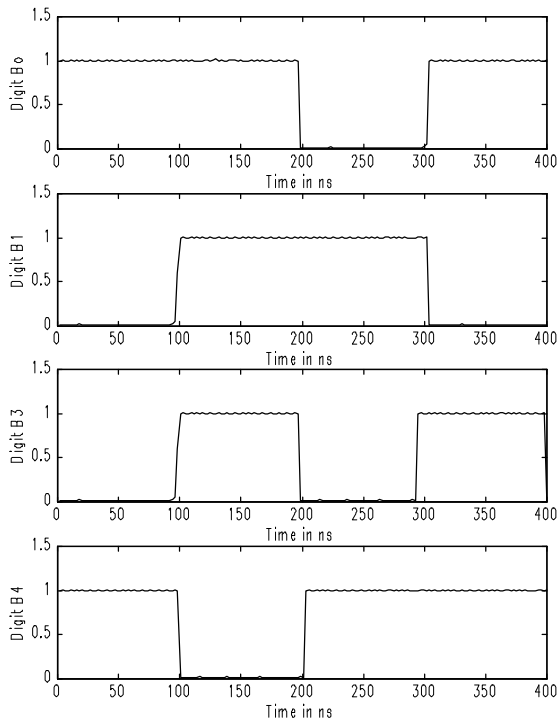


Fig5. Optical waveforms of input binary digits B_0 , B_1 , B_2 , and B_3

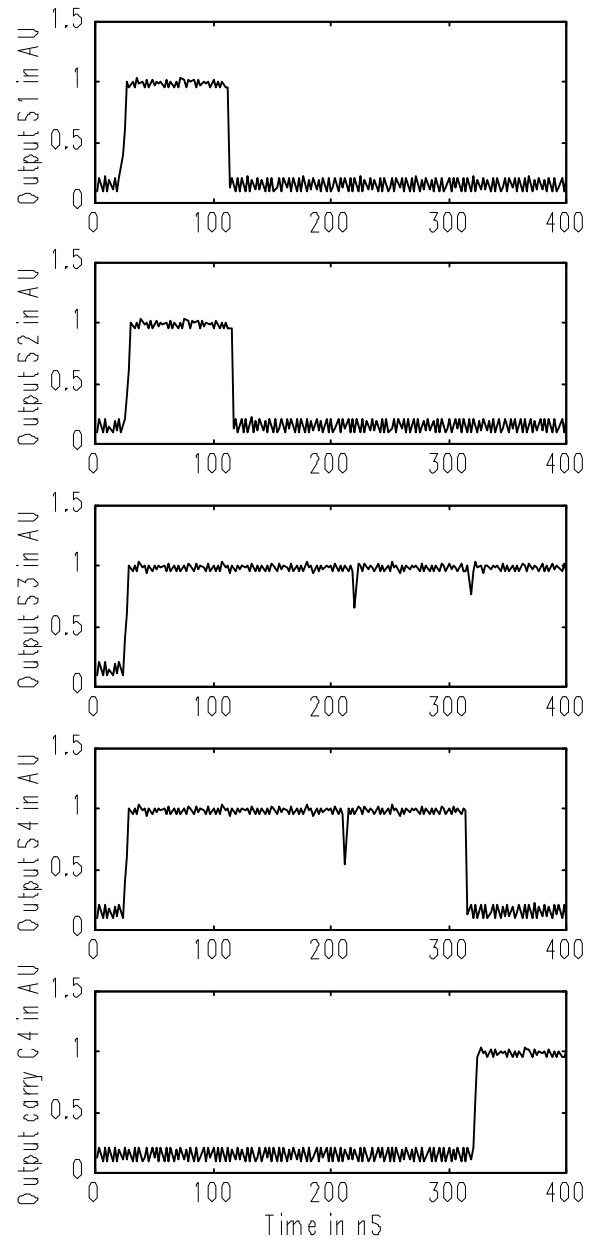


Fig 6. The output optical waveform of all-optical parallel adder S_0 , S_1 , S_2 , S_3 , and C_4 .

The basic component of an arithmetic circuit is the parallel adder. By controlling the data inputs to the parallel adder, it is possible to obtain different types of arithmetic operations. The block diagram of figure 7 demonstrates a possible configuration of 8 bit arithmetic unit, where one set of inputs to the parallel adder is controlled by two selection lines X_4 , and X_3 by using 3dB couplers and all optical AND gates. All optical AND gate is constructed using hardlimiter with limiting value equal $a=2$.

The optical control lines X2, and X1 are applied to all optical XOR gates (2^{nd} level of hardlimiters of limit value $a=2$) [1,4] with 3 dB couplers to control on the arithmetic operation with selection line X0, where X0 represents the input carry of the full adder circuit in the least significant bit position [5].

4 Conclusion

An all-optical optical parallel adder and all-optical arithmetic based on cascaded optical all-optical full adders and all-optical logic gates are designed and experimentally demonstrated with simulation (Beam Prop V.5) at an operation of 10 MHz. All-optical system computation eliminates the conversion from optical to electrical and vice versa. Accordingly, the latency is smaller than that using electrical digital computation. The time taken by each all-optical digital device and full adder could be reduced to sub nanoseconds by building integrated bragg gratings and optical fibers on SOI ridge waveguides [6].

The operation speed may increase to perform a fast optical central processor unit by using the photonic integration, which would decrease the dimensions of the building blocks [7].

Finally, the presented all-optical arithmetic unit based on optical parallel adder could be used with all-optical Multiplexer in [1] and optical gates in [1,4] to form an all-optical arithmetic and logic unit (ALU).

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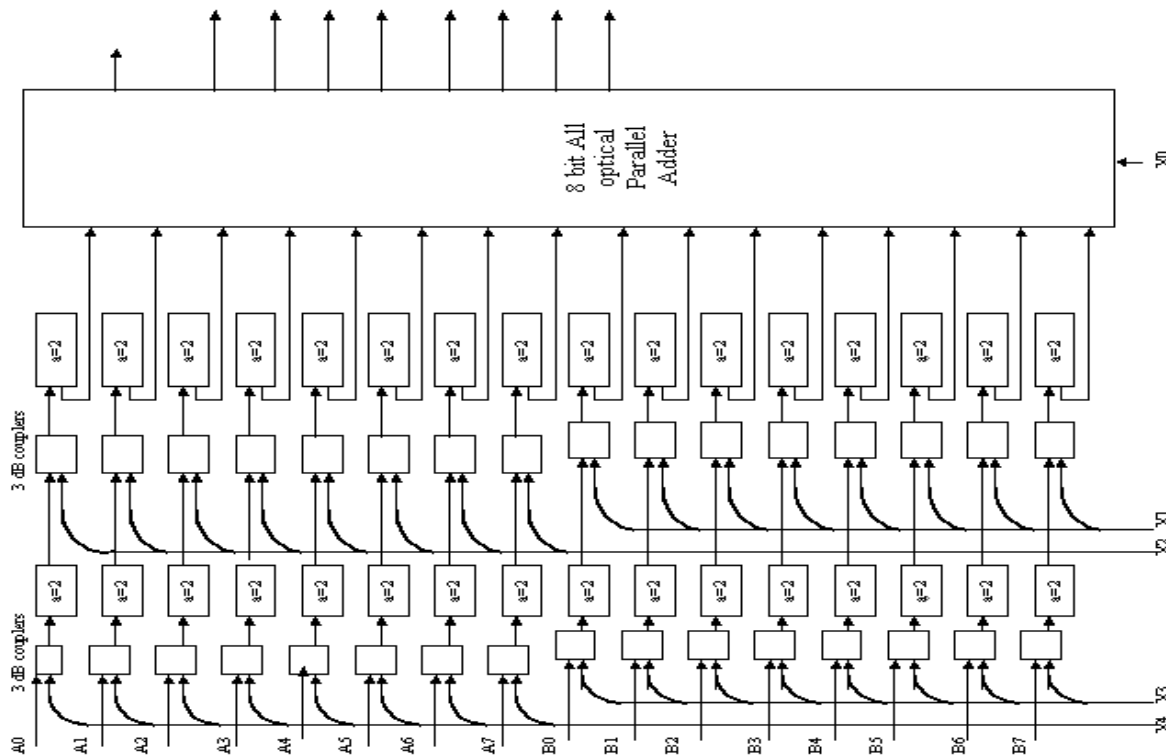


Fig.7.All-optical arithmetic unit based on all-optical parallel adder and optical logic gate.