Impact of MOSFET parameters on its parasitic capacitances

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Abstract: The aim of this paper is to calculate the MOSFET parasitic capacitances, and then based on the results obtained we can further see the impact of MOSFET physical parameters on these parasitic capacitances. These capacitances have a direct impact in the speed of operation of MOSFET circuits. Therefore, in order to increase the speed of operation, it is necessary that the parasitic capacitances are reduced to a minimum possible level that the technological process allows. We have analyzed the gate capacitance effect and junction capacitances as a function of the MOSFET dimensions.

Key words: MOSFET parameters, Parasitic capacitances, Gate capacitive effect, Junction capacitances, Speed of operation, Worst case conditions.

1 Introduction

When we analyze MOSFET in its transitive work regime (AC) we should have in mind the parasitic capacitances which influence the speed of operation of the MOSFET device and the MOSFET digital circuits. Considering the MOSFET's structure, these capacitances are distributed and their exact calculation is quite complex. But, by using simple approximation, we can obtain the value of parasitic capacitances which can be used for analyzing the main characteristics of MOSFET-s in AC. The Fig.1 shows the cross-section view and the top view (mask view) of typical n-channel MOSFET (enhancement-type).

Because the gate (L_M) has an extension over the source and drain regions (see Fig. 1), indicated with L_D, the effective channel length is [1, 4, 5]:

$$L = L_M - 2L_D \quad (1)$$

Note that the source and drain overlap region lengths are usually equal to each other because of the symmetry of the MOSFET structure. Typical values of L_D are from $0.05L$ to $0.1L$. Drain and source diffusion regions have a width denoted with W, length is denoted by Y and depth is denoted with x_j. Both drain and source regions are surrounded by p^+ in three sides with the purpose of preventing the formation of any unwanted channels between two neighboring n^+ diffusion regions (as in the case of integrated circuits).

Based on physical structure of MOSFET, its parasitic capacitances can be classified into two major groups:

– the gate capacitive effect (indicated by C_{ox}) and
– junction capacitances *drain-body* and *source-body*.

These two capacitive effects can be modeled by including capacitances in the MOSFET model between its four terminals, G, D, S, and B as shown in Fig.2. There will be five capacitances: C_{gs}, C_{gd}, C_{gb}, C_{sb} and C_{db} where the subscripts indicate the terminals [2, 3, 5, 6].

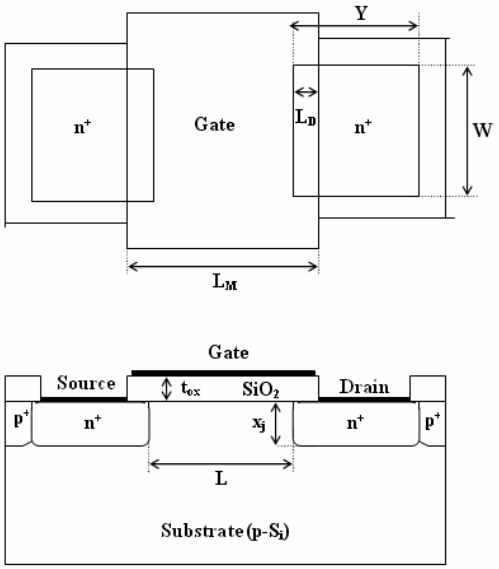

Fig.1 Cross-section view and the top view of typical n-channel MOSFET.

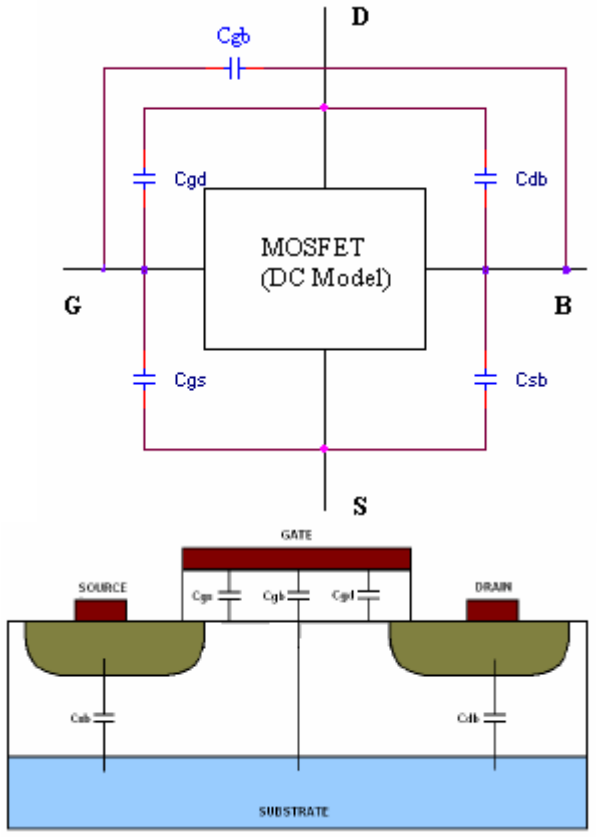

Fig. 2 Lumped representation of the parasitic MOSFET capacitances.

2 Calculation of parasitic capacitances: Results and discussion

2.1 The gate capacitive effect

The gate capacitive effect can be modeled by overlapping capacitances C_{GSov}, C_{GDov} and capacitances which are result of interaction between electrodes C_{gs}, C_{gd} and C_{gb} when MOSFET is operating in different work regions [2, 3, 5, 6].

Assuming that both the source and the drain diffusion regions are identically, the overlap capacitances can be calculated as:

$$C_{GSov} = C_{ox}WL_D \quad (2)$$

$$C_{GDov} = C_{ox}WL_D \quad (3)$$

where C_{ox} indicates the value per unit gate area:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (4)$$

ε_{ox} – dielectric constant of S_iO_2, where $\varepsilon_{ox} = 3.97\ \varepsilon_o$ (ε_o – dielectric constant of vacuum), and t_{ox} – thickness of oxide layer.

Overlapping parasitic capacitances do not depend on the bias conditions (they are voltage-independent). Overlapping capacitances gate-body will not be considered because their values are very small; to compensate this we assume that effective width of channel is W.

Parasitic capacitances C_{gs}, C_{gd}, C_{gb} depend on bias conditions (they are voltage-dependent) as:

– when MOSFET is operating in triode region, channel is considered to be uniform from the source to the drain. Therefore, in this case the gate-channel capacitance will be WLC_{0x} and can be modeled:

$$C_{gs} = C_{gd} = \frac{1}{2}WLC_{ox} \quad \text{and} \quad C_{gb} \approx 0 \quad (5)$$

– when MOSFET is operating in saturation mode, the channel has tapered shape and is pinched off at or near the drain end, thus the channel will not be uniform. In this case the gate-channel capacitance will be approximately $2/3 \cdot WLC_{0x}$ and can be modeled as:

$$C_{gs} \approx \frac{2}{3}WLC_{ox}, \ C_{gd} = 0, \text{ and } C_{gb} = 0 \quad (6)$$

– when **MOSFET** is in cut-off mode, channel is not inducted, thus in this case capacitive effect can be modeled as:

$$C_{gs} = C_{gd} = 0 \ \text{ and } \ C_{gb} = WLC_{ox} \quad (7)$$

As we can see from what we said above, the sum of three parasitic capacitances is dependent of gate voltage. This sum has maximal value $C_{ox}WL$ (in the cut-off and triode region) and minimal value is $0.66 \cdot C_{0x}WL$ (in saturation mode).

Gate capacitive effects in three operating regions of MOSFET including overlapping capacitances are presented as in table 1.

Tabele 1.

Capa-citance	Cut-off	Linear	Saturation
C_{gbt} C_{gdt} C_{gst}	$C_{ox}WL$ $C_{ox}WL_D$ $C_{ox}WL_D$	0 $1/2C_{ox}WL+C_{ox}WL_D$ $1/2C_{ox}WL+C_{ox}WL_D$	0 $C_{ox}WL_D$ $2/3C_{ox}WL+C_{ox}WL_D$

In Fig. 3 is shown the dependence of gate capacitive effect in the so-called "worst case" conditions on area S (product between width and length channel), for parametric values of thickness of oxide layers. With the so-called "worst case" we understand the case when gate capacitive effect reaches its maximal value.

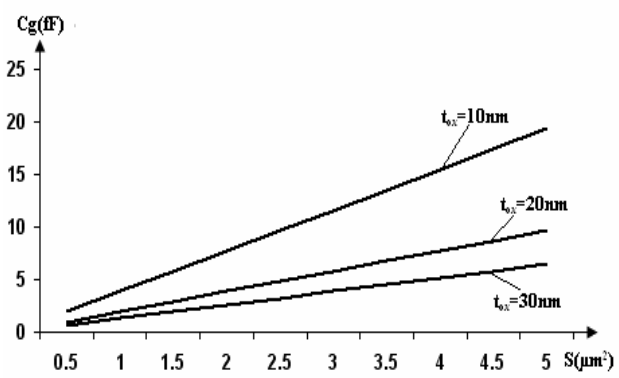

Fig.3 The dependence of gate capacitive effect on area S for the different values of parameter t_{ox}.

From fig.3, based on acquired values, we can conclude that gate capacitive effect is in direct proportion with the size of the area *S* but in indirect proportion with thickness of oxide layer. Therefore, minimal capacitive values are gained when *S* (*W*L)* is lower and thickness gains higher values (but, thickness has effect in threshold voltage).

2.2 Junction capacitances

Parasitic capacitances formed between the source-body and drain-body regions, as a result of reversed polarization during normal operating region of MOSFET, will be in function with reversed polarization voltage. Three dimensional shape of n^+ will form five planer pn-junctions with the surrounding p-type substrate indicated with numbers from 1 to 5. In advanced MOSFET-s these parasitic capacitances are calculated separately according to their specific junctions and lumped together in the end. Fig.4 shows a simpler geometrical shape of MOSFET, focusing n^+ diffusion regions (source) inside body (substrate).

In order to simplify calculation of parasitic capacitances assume that n^+ is rectangular box with dimensions: width *W*, length *Y*, depth x_j. Abrupt (step) pn-junction profiles will be assumed for all junctions for simplicity. In table 2 are shown types and region junctions from Fig. 4.

In the sidewalls 2, 3 and 4 p^+ regions we usually have density about $10N_A$. In practice the actual region shape is quite complicated and impurity concentration is not uniform.

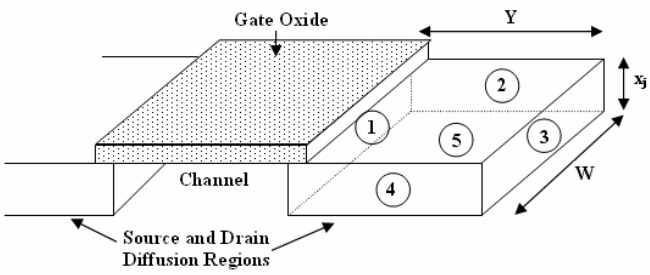

Fig.4 Three-dimensional view of the n^+ diffusion regions within the p-type substrate.

Table 2. Types and areas of the pn-junctions

Junction	Area	Type
1	W*x_j	n^+/p
2	Y*x_j	n^+/p^+
3	W*x_j	n^+/p^+
4	Y*x_j	n^+/p^+
5	W*Y	n^+/p

To calculate the depletion capacitance of a reverse-biased abrupt pn-junction, firstly we consider the depletion region thickness, which is x_d. Assuming that the n-type and p-type doping densities are given by N_D and N_A, respectively, and that reverse bias voltage is given by *V* (negative), the depletion region thickness can be calculated as [3, 5]:

$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{q} \cdot \frac{N_A + N_D}{N_A N_D} \cdot (\phi_0 - V)} \qquad (8)$$

where the built-in junction potential is calculated as:

$$\phi_0 = \frac{kT}{q} \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) \qquad (9)$$

k – Boltzmann's constant, *T* – temperature in Kelvin, *q* – electron charge and n_i – intrinsic carrier concentration in Si.

In normal operating region *pn*-junctions are reverse-biased, therefore amount of electric charge which is stored in depletion region is found by:

$$Q_j = A \cdot q \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D}\right) \cdot x_d = A\sqrt{2\varepsilon_{Si} \cdot q \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D}\right) \cdot (\phi_0 - V)} \qquad (10)$$

A – indicates junction area.

The junction capacitances associated with the depletion region are defined as:

$$C_j = \left| \frac{dQ_j}{dV} \right| \tag{11}$$

After differentiating (10) by voltage V, we can obtain the expression for pn-junction capacitances:

$$C_j(V) = A \cdot \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D} \right) \cdot \frac{1}{\sqrt{\phi_0 - V}}} \tag{12}$$

This expression can be rewritten in general form by considering the junction grading.

$$C_j(V) = \frac{A \cdot C_{j0}}{\left(1 - \frac{V}{\phi_0} \right)^m} \tag{13}$$

The parameter m in expression (13) is called the grading coefficient. Its value is equal to 1/2 for a step (abrupt) junction profile and 1/3 for a linearly graded junction profile. The zero-bias junction capacitance per unit area C_{j0} is defined as:

$$C_{j0} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D} \right) \cdot \frac{1}{\phi_0}} \tag{14}$$

From expression (13) it is obvious that junction capacitance value C_j depends from the external voltage which operates in *pn*-junction. Since the terminal voltage of a MOSFET will change during dynamic operation, exact calculation of junction capacitances under transient conditions is quite complicated. Calculation of junction capacitances by (13) is valid only in the case of small-signal operation. The problem of calculating the junction capacitances value under changing bias conditions can be simplified if we calculate a large-signal average junction capacitance as in the case of logic circuits. This equivalent large-signal capacitance can be defines as [3]:

$$\begin{aligned} C_{eq} &= \frac{\Delta Q}{\Delta V} = \frac{Q_j(V_2) - Q_j(V_1)}{V_2 - V_1} \\ &= \frac{1}{V_2 - V_1} \cdot \int_{V_1}^{V_2} C_j(V) dV \end{aligned} \tag{15}$$

The reverse bias voltage across the pn-junction is assumed to change from V_1 to V_2. The equivalent capacitance is obtained by substituting (13) into (15):

$$C_{eq} = -\frac{A \cdot C_{j0} \cdot \phi_0}{(V_2 - V_1) \cdot (1 - m)} \cdot \left[\left(1 - \frac{V_2}{\phi_0} \right)^{1-m} - \left(1 - \frac{V_1}{\phi_0} \right)^{1-m} \right] \tag{16}$$

In the case when m = 1/2 will have:

$$C_{eq} = -\frac{2 \cdot C_{j0} \cdot \phi_0}{(V_2 - V_1)} \left[\sqrt{1 - \frac{V_2}{V_0}} - \sqrt{1 - \frac{V_1}{V_0}} \right] \tag{17}$$

The equation (17) can be rewritten in simpler form by defining a dimensionless coefficient K_{eq}, as follows:

$$K_{eq} = -\frac{2\sqrt{\phi_0}}{V_2 - V_1} \cdot \left(\sqrt{\phi_0 - V_2} - \sqrt{\phi_0 - V_1} \right) \tag{18}$$

$$C_{eq} = A \cdot C_{j0} \cdot K_{eq} \tag{19}$$

K_{eq} – is called the voltage equivalence factor $(0 < K_{eq} < 1)$.

The accuracy of calculated values by expressions (18) and (19) is usually sufficient.

From fig.1 and fig.2 in three junction sidewalls (2, 3 and 4) of MOSFET, source and drain regions are surrounded by p^+ region, with higher doping density then substrate. Consequently, the sidewall zero-bias capacitance C_{j0sw}, as well as the sidewall voltage equivalence factor $K_{eq}(sw)$ will by different from those of the bottom junction (junction 5) and sidewall junction from channel (junction 1). Assuming that the sidewall doping density in p^+ is $N_A(sw)$, then we will have:

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A(sw) \cdot N_D}{N_A(sw) + N_D} \right) \cdot \frac{1}{\phi_{0sw}}} \tag{20}$$

where ϕ_{0sw} -is the build-in potential of the p^+ sidewall junctions with drain or source regions.

$$\phi_{0sw} = \frac{kT}{q} \cdot \ln\left(\frac{N_A(sw) \cdot N_D}{n_i^2} \right) \tag{21}$$

Since all sidewalls regions p^+ have approximately same depth of x_j, we can define a zero-bias sidewall junction capacitance per unit length.

$$C_{jsw} = C_{j0sw} \cdot x_j \tag{22}$$

The sidewall voltage factor for a voltage swing between V_1 and V_2 is defined as follows:

$$K_{eq}(sw) = -\frac{2\sqrt{\phi_{0sw}}}{V_2 - V_1} \cdot \left(\sqrt{\phi_{0sw} - V_2} - \sqrt{\phi_{0sw} - V_1} \right) \tag{23}$$

Combining the equation (20) through (22), the equivalent large-signal junction capacitance $C_{eq}(sw)$ for sidewall of length (perimeter) P can be calculated as:

$$C_{eq}(sw) = P \cdot C_{jsw} \cdot K_{eq}(sw) \tag{24}$$

Combining the equivalent junction capacitances we can find the equivalent junction capacitance of drain-body or source-body using expressions:

$$C_{db} = C_{sb} = A_t \cdot C_{j0} \cdot K_{eq} + P_t \cdot C_{jsw} \cdot K_{eq}(sw) \tag{25}$$

A_t – total area of the n^+/p junctions (sum of the bottom area and the sidewall area facing the channel region).

P_t – length of the n^+/p^+ junction perimeter (sum of three sides of the drain diffusion area).

Fig. 5 shows the dependence of equivalent capacitance C_{db} from the width of drain regions (W) for parametrical length value(Y) and depth value (x_j) of drain.

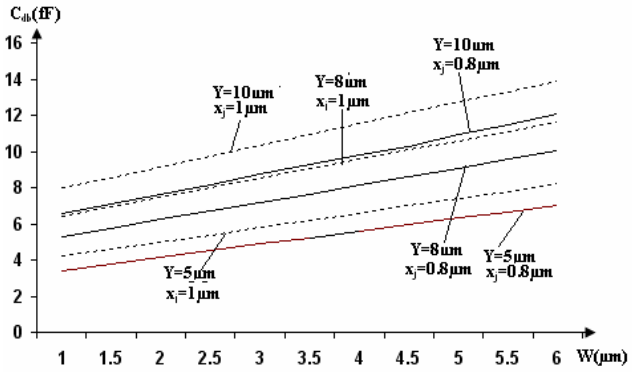

Fig.5. Dependence of junction capacitance drain-body C_{db} and W on parametrical values of Y and x_j of drain region, for: $N_A = 2 \cdot 10^{15}$ cm^{-3}, $N_D = 10^{19}$ cm^{-3}, N_A (*sw*) $= 4 \cdot 10^{16}$ cm^{-3}; $V_1 = 0$ V and $V_2 = -5$ V.

From Fig. 5 it is shown that parasitic capacitance values are related to the dimensional values of drain region. The higher dimensions of drain region (W or Y or x_j) will achieve higher values of parasitic junction capacitance C_{db} (or parasitic junction capacitance C_{sb}).

3 Conclusion

Based on results obtained, as shown in figures (3 and 5), we see the dependence of the gate capacitive effect and the junction parasitic capacitance on the MOSFET dimensions. Therefore, we can conclude that the value of the gate capacity effect can be reduced by smaller values of channel dimensions (W and L) as per technological process possibilities. Furthermore, the parasitic junction capacitances will be smaller if the dimensions of drain and source regions are smaller. To achieve the higher speed of operation, the dimensions of MOSFET device should be as smaller as possible.

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