ADAPTIVE BLOCK WATERMARKING AND ITS SOC IMPLEMENTATION BASED ON JPEG2000 DWT

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Abstract: - In this paper, we propose and verify an adaptive block watermarking algorithm based on JPEG2000 DWT, which determines watermarking for the original image by two scaling factors in order to overcome image degradation and blocking problem at the edge. Adaptive block watermarking algorithm uses 2 scaling factors, one is calculated by the ratio of present block average to the next block average, and the other is calculated by the ratio of total LL sub-band average to each block average. Signals of adaptive block watermark are obtained from an original image by itself and the strength of watermark is automatically controlled by image characters. Instead of conventional methods using identical intensity of a watermark, the proposed method uses adaptive watermark with different intensity controlled by each block. Thus, an adaptive block watermark improves the visuality of images by 4～14dB and it is robust against attacks such as filtering, JPEG2000 compression, resizing and cropping. Also we implemented the algorithm in ASIC using Hynix 0.25㎛ CMOS technology to integrate it in JPEG2000 codec chip.

Key-Words: - JPEG2000, Watermarking, DWT, SOC, ABW(Adaptive Block Watermarking)

1 Introduction

Most of data being processed in digital domain, however it is easy to copy, modify, and manipulate. Watermarking technology was proposed in order to protect the copyright of original data.

The watermarking in frequency domain usually was used with DCT(discrete cosine transform) and DWT(discrete wavelet transform)[1]. In case of still image, the DWT is replacing DCT to get better picture quality and lower bit rate in compression in JPEG2000. Therefore watermarking based on DWT have been proposed, but previous works use predefined watermarks to the image and they are known to decrease the image quality [2][3][4].

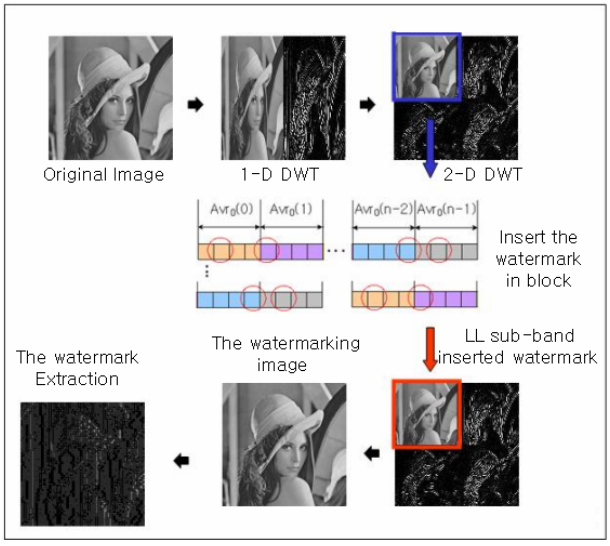


Figure 1. Proposed watermarking algorithm

In this paper, we propose an adaptive block watermarking method that can be used for the JPEG2000 and implemented in a chip with Hynix

0.25um technology. After decomposing an image to 1-level by using DWT of JPEG2000, all coefficients in LL sub-band are divided by block units and then operated watermarks within blocks. By using luminance correlation of an image, we generated two scaling factors and these determine watermark intensities. The watermarks with different intensities improve visuality and robustness of image and implemented hardware can be used in JPEG2000 codec chips [5].

We explain the adaptive watermarking algorithm in section II and we describe hardware implementation In Section III. In section Ⅳ, we compare performance of our method with others and describe ASIC implementing result, and the conclusion is in section Ⅴ.

2 Proposed Watermarking Algorithm

In this section, we briefly outline the adaptive block watermarking algorithm for hardware implementation. In JPEG2000 encoding process, discrete wavelet transform (DWT) is used to separate low frequencies from high frequencies. Low frequency domain contains more significant information of image than in high frequency domain. Selected high frequency coefficients are removed by the quantization process for lossy compression.

Therefore, watermark is embedded in low frequency domain called LL sub-band. The watermarked image is obtained by two scaling factors in DWT coefficient block. One is calculated by the ratio of the present block average to the next block average.

The other is calculated by the ratio of total LL sub-band average to the each block average. We call the factor alpha(α), beta(β) respectively. A block is group of 4 DWT coefficient s in each row. Figure 2 describes this algorithm..

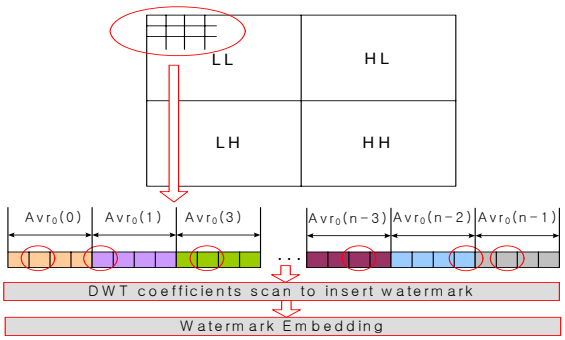


Figure 2. Adaptive block watermarking algorithm

Let $Arv_m(n)$ denote a block average of LLO sub-band, $\omega_m(n)$ denote initial watermark intensity. The algorithm is expressed as follows.

$$\alpha_m(n) = \frac{Arv_m(n)}{\sum_{m=0}^{LL}\sum_{n=0}^{M} Arv_m(n)} \quad (1)$$

$$\beta_m(n) = \frac{Arv_m(n+1)}{Arv_m(n)} \quad (2)$$

$$Y'_m(n) = Y_m(n)\cdot[1+\alpha_m(n)\cdot\omega_m(n)]\cdot[1+\beta_m(n)\cdot\omega_m(n)] \quad (3)$$

- $Arv_m(n)$ is calculated from n[th] block average of m-th row.
- We select the largest $Y_m(n)$ from $Arv_m(n) \le Y_m(n) < 255$
- If $Arv_m(n)$ is equal to 255, the n[th] block watermark of m[th] row is not inserted.
- If $Arv_m(n)$ is equal to 0, 1 is inserted in the 1[st] signal of the block as the n[th] block watermark of m[th] row, regardless of Eq.(3).

3 Implementation

We implemented the proposed algorithm in ASIC. The ASIC consists of a watermarking processing part and I/O interface.

Figure 3 shows the watermarking processing part. This part finds the signal which watermarking data is inserted through the 16-bit comparator from four coefficients and computes the average of a block. And it calculate ratio α from the block average and the total average of LL sub-band. It inserts watermarking according to Eq. (3).

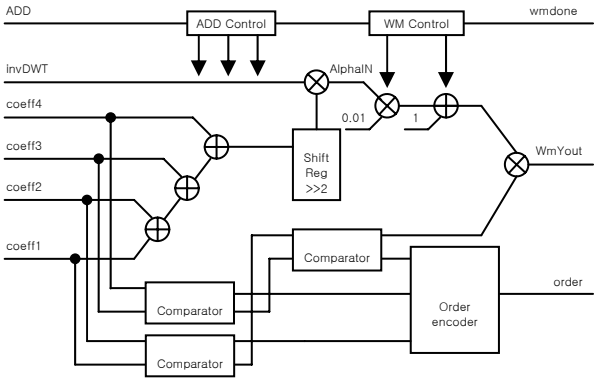


Figure 3. Hardware block diagram of watermarking

Watermarking hardware organized such that it takes 32-bit input. So proposed design can input two DWT coefficients per cycle. Figure 4 presents input interface. Firstly, the inverse of total average of LL sub-band is delivered, and then two coefficients are delivered according to the DIN signal.

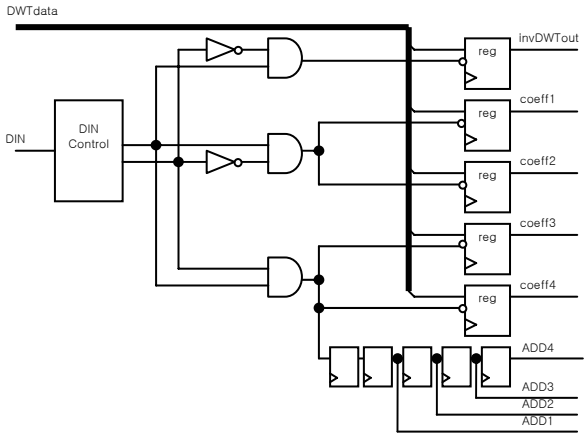


Figure 4. Input interface block diagram

Figure 5 presents the output interface that generate the coefficient of the block after watermark data is inserted. Watermarking coefficient is selected in data selector by sel1, sel2 signals which show where the coefficient is to the inserted. Because four coefficients are a total of 64 bits, coefficients are transferred starting from the first coefficient by OE signal

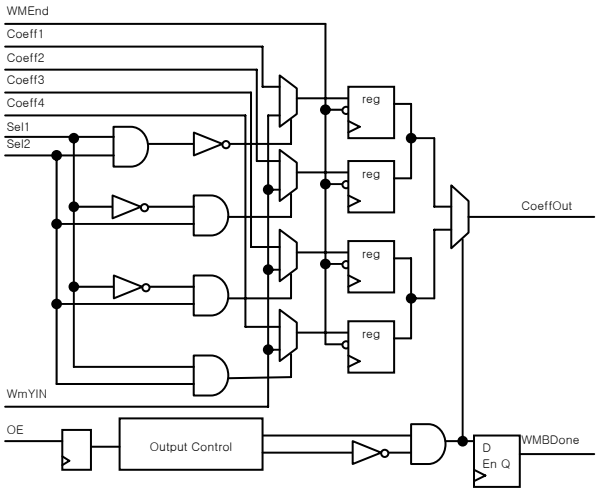


Figure 5. Output interface block diagram

4 Experimental Result

In this paper, we proposed and verified adaptive block watermarking algorithm. Test images are Lena, Goldhill and Baboon with 256 by 256 pixels. We inserted 4096 watermarks at the LL sub-band increase robustness and we also used two scaling factor and increased invisibility of images. The algorithm was verified in the test board with a chip designed and fabricated by Hynix 0.25㎛ CMOS process.

Table 1.The adaptive watermarking chip specification

Process Technology	Hynix 0.25um CMOS 1P4M
Gate count	7172 gates
Clock Frequency	125MHz
Supply Voltage	3.3V
Number of I/O pins	69

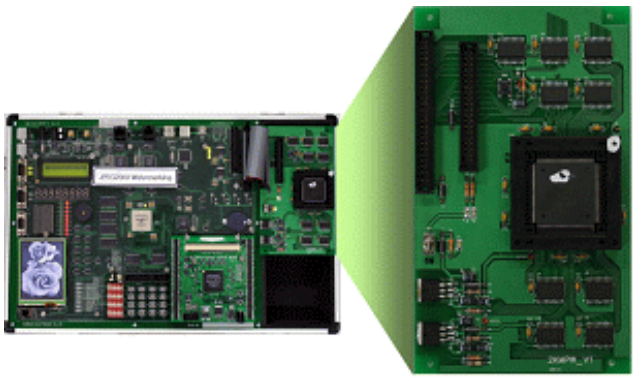


Figure 6. Verification of the chip by using test board & platform

We used Lena, Goldhill and Baboon to estimate proposed watermarking algorithm. We compared the test results with the existing algorithms. Figure 7 shows original test image and inserted watermark image. Table 2 and Table3 present the comparison of PSNR and robustness between proposed architecture and previous works. As a result, the performance of PSNR is increased by 4 ~ 10dB and the characteristic of invisibility is improved. In addition, proposed algorithm is more robust than existing algorithms against various watermarking attack.

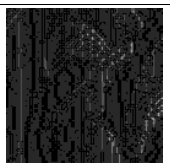
original Image	9/7 filter image inserted watermark	Inserted watermark
		
Lena	Lena	Lena

Figure 7. Comparison between original image and watermarking image

Table 2. The normalized similarity according to a series of attacks of Lena image

attack	Proposed method 9/7 filter	Proposed method 5/3 filter	Podilchuk 's method[2]	Dugad 's method[3]	Lumini 's method [4]
3 X 3 LPF	58.1	57.6	35.99	6.24	26.02
5 X 5 LPF	35.08	38.5	10.31	2.02	9.56
7 X 7 LPF	18.2	19.8	3.94	0.88	4.21
Scaling	35.78	36.6	34.99	5.90	6.01
Cropping	68.2	67.85	67.78	59.82	19.30
1% Random noise	89.8	90.4	89.20	23.62	4.54

Table 3. PSNR(dB) comparison with watermarking image

Image	Proposed method 9/7 filter	Proposed method 5/3 filter	Podilchuk 's Method[2]	Dugad's Method[3]	Lumini 's Method[4]
Lena	45.34	47.70	38.67	37.97	37.12
Baboon	39.20	41.37	35.53	35.28	34.72
Goldhill	45.14	47.50	36.64	37.60	33.72

5 Conclusion

In this paper, we proposed and implemented watermarking algorithm based JPEG2000 DWT to protect the copyright of digital data.

As a result of implementation with the ASIC, it has about 7K gate counts and the maximum operation frequency is 125MHz. Watermarking IP can be integrated with the JPEG2000 codec chip and we have verified superior invisibility and robustness when used with future printers, scanners and digital cameras.

References:

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