Acoustic Level Dynamic Compression Characteristics with FPGA Implementation

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Abstract: In this paper, we propose an FPGA design of an audio signal level compressor, based on an approximation algorithm using a polynomial. To implement a compression characteristic in a digital audio system, the gain calculation with fractional numbers is performed by using a polynomial expression to approximate the power operation, then the compressor can be designed with a number of additions, multiplications and a division. The arithmetic circuits were implemented in FPGA technology and the 16-bit compressor used 541 logic elements and 352 flip-flops of the hardware resource of EP20K200EFC484-2X from Altera. The proposed compressor can be applied as a functional unit in an on-chip audio system. The performance of the proposed compressor is evaluated by analysis and simulation.

Key–Words: Audio signal, Dynamic range control, Compression ratio, Gain, FPGA.

1 Introduction

Digital audio systems have advantages in audio signal transferring, recording and delay controlling over conventional analog systems. Various digital filters on digital signal processors(DSPs) for getting the frequency responses have been proposed[1]. It is desired that an audio system with a number of functional modules such as analog-to-digital and digital-to-analog converters, CPU, DSPs, memory and dynamic range controllers is implemented on a VLSI chip, called audio system on a chip[2, 3, 4]. Recently, FPGA (Field Programmable Gate Array) chips are often used to implement a digital system for shortening the development time to market, because high-performance FPGAs have been equipped with DSPs, memory and logic elements[5].

Dynamic range control of audio signal levels is a general requirement to get sound effects[3]. Compressors and limiters are such dynamic range controllers and may be also used to prevent peaks exceeding the maximum usable value in an audio system. As shown in Fig.1, a dynamic range controller performs the peak detection, gain calculation, attack time and release time control in the functional block, GAIN CONTROL, and then applys the gain to control the signal level. In a conventional dynamic range controller with analog circuits, a voltage-controlled amplifier (VCA) is used[4, 6] to control signal level.

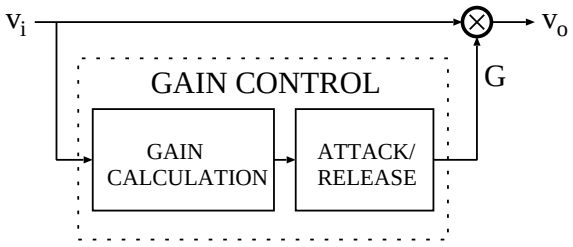


Figure 1: Dynamic range controller.

In general, the VCA circuit has the nonlinear input-output characteristics, which result in the harmonic distortion in the output signal.

Digital dynamic range controllers may implement the same functional blocks as the analog circuits. Thus, the harmonic distortion arisen by the VCA may be avoided by using the multiplication. However, the main problem is to perform the calculation for the power transformation, that is, how $x^y (0 < x, y < 1)$ is calculated efficiently with few operations and less hardware. In this paper, a polynomial expression is applied for the power transformation, so that the efficient hardware implementation in FPGA technology can be easily achieved by using a number of logic elements and flip-flops in an FPGA chip. To reduce the hardware resources, we propose an architecture with fewer multipliers, and the multipliers are designed by

using a shift-accumulation algorithm. The simulation results of 16-bit, 24-bit and 32-bit compressors designed using FPGA implementation technology show that the proposed compression characteristics are very close to the ideal ones.

2 Characteristics of Compressor

The audio signal levels are usually expressed by multiples of the reference voltage and are represented by decibels(dB). For a compressor, the input and output signal levels are denoted as V_i and V_o,respectively, and they have the following relationships:

$$V_i = 20\log_{10}(A_i), \quad (1)$$
$$A_i = |v_i|, \quad (2)$$
$$V_o = 20\log_{10}(A_o), \quad (3)$$
$$A_o = |v_o|, \quad (4)$$

where v_i and v_o are the input and output signals as shown in Fig.1, respectively. A_i and A_o have the values relative to the maximum magnitude of input signal which is the reference value in a digital audio system. Without loss of generality, we can suppose $-\infty \leq V_i, V_o \leq 0$(dB), then v_i and v_o are real numbers in [-1,1] and A_i, A_o are real numbers in [0,1].

The compression characteristics are defined in Fig.2, which are measured with the RMS(root mean square) values of the signal's magnitudes. When the audio level V_i of the input signal of a compressor is greater than a threshold level V_T, the signal level is compressed with a compression ratio p. That is, if $V_i > V_T$ then $\Delta V_i : \Delta V_o = p : 1$ ($p \geq 1$). When $p = \infty$, the compressor becomes a limiter. The relationship between the input and output levels is represented by the following equation:

$$V_o = \begin{cases} (1/p)(V_i - V_T) + V_T & (V_i > V_T) \\ V_i & (V_i \leq V_T) \end{cases}. \quad (5)$$

The attack time and release time control is a very important function to make the dynamic sound effects. In our approach, as shown in Fig.1, an ATTACK/RELEASE functional block is designed not only to make the sound effects but also to smooth the gain obtained in the GAIN CALCULATION block. Let the input and output of ATTACK/RELEASE block be G_i and G, respectively. G_I is the gain obtained from the GAIN CALCULATION block, where $0 < G_i \leq 1$. The attack time and release time are defined as follows:

Let $G = G_i = G_0$ initially. At the time $t = 0$, G_i changed and has a new value ($G_i \neq G_0$), then G is

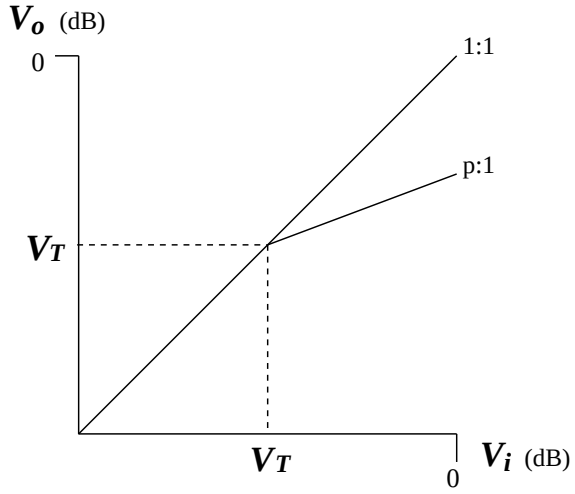


Figure 2: Compression characteristic.

changing from G_0 to G_i by the following equation,

$$G = G_i + (G_0 - G_i) \times exp(-t/T). \quad (6)$$

When $G_i < G$, $T_a = T$ is defined as the attack time, while $T_r = T$ is the release time when $G_i > G$. In general, $T_r \gg T_a$. From Eq.(6), we have

$$\Delta G/\Delta G_i = 1 - exp(-t/T), \quad (7)$$

where $\Delta G = G - G_0$ and $\Delta G_i = G_i - G_0$. Thus, the attack time and release time are the intervals, while the value changed on the output of ATTACK/RELEASE has become 63.2% of that changed on the input of the ATTACK/RELEASE block[**?**].

3 FPGA Design for the Gain Computation with a Polynomial Expression

3.1 Compression Characteristics with a Polynomial Expression

We begin the computation by considering the compression characteristics with a compression ratio $p(p \geq 1)$ as shown in Fig.2. From Eqs.(1),(3) and (5), we have the following relationship between the input and output signals of the compressor with a compression ratio p:

$$A_o = \begin{cases} v_t^{(p-1)/p} \cdot A_i^{1/p} & (A_i \geq v_t) \\ A_i & (A_i < v_t) \end{cases}, \quad (8)$$

where v_t is the signal threshold having a positive value with respect to the level threshold V_T satisfying $V_T =$

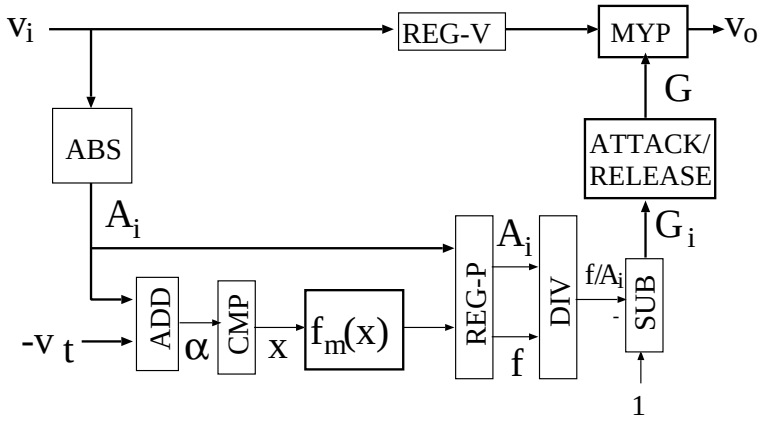


Figure 3: Architecture of the proposed compressor.

$20\log_{10}(v_t)$. The representation of the gain, G, may be obtained by

$$G = \begin{cases} (v_t/A_i)^{(p-1)/p} & (A_i \geq v_t) \\ 1 & (A_i < v_t) \end{cases}, \quad (9)$$

$$A_o = G \cdot A_i. \quad (10)$$

Because of the same signs of v_i and v_o shown in Fig.1, Eq.(11) is a general form of Eq.(10).

$$v_o = G \cdot v_i. \quad (11)$$

It is difficult to obtain the gain by Eq.(9) directly, which has the power calculation with fractional numbers. To simplify the power calculation, a polynomial expression is derived to approximate the compression characteristics. In the case of $A_i \geq v_t$, the gain may be represented by the following equation:

$$G = 1 - (1/A_i) \cdot f, \quad (12)$$

where,

$$f = A_i - v_t^{(p-1)/p} \cdot A_i^{1/p}. \quad (13)$$

Obviously, $0 \leq f < A_i$ and $0 < G \leq 1$.

Let $\alpha = A_i - v_t$, then Eq.(13) may be expressed by a polynomial of degree m of α to approximate the gain calculation as follows:

$$f_m(\alpha) = b_0 + b_1\alpha + b_2\alpha^2 + ... + b_m\alpha^m. \quad (14)$$

Since $f_m(0) = 0$, then $b_0 = 0$. Substituting the polynomial expression and a two-value variable $\delta \in \{0, 1\}$ into Eq.(9),

$$\delta = \begin{cases} 1 & (\alpha > 0) \\ 0 & (\alpha \leq 0) \end{cases}, \quad (15)$$

and let

$$x = \delta \cdot \alpha, \quad (16)$$

then the gain can be expressed as follows:

$$\begin{aligned} G &= 1 - (\delta/A_i) \cdot f_m(\alpha) \\ &= 1 - f_m(x)/A_i. \end{aligned} \quad (17)$$

Thus the power calculation with fractional numbers for getting compression characteristics is equivalent to the calculation of a division and the polynomial expression with parameters $(b_1, b_2, ..., b_m)$, which is easily performed by using arithmetic circuits such as adder, multiplier and divider as shown in Fig.3. If the parameters are set to $b_1 = 1$ and $b_i = 0 (i = 2, ...m)$, for $\alpha > 0$

$$G = 1 - \alpha/A_i = v_t/A_i$$

and

$$A_o = G \cdot A_i = v_t.$$

Thus a limiter characteristic, $p = \infty$, is obtained. Obviously, the larger the degree of the polynomial expression, m, the closer to the ideal the approximation characteristic is. The least aquares method may be used to calculate the parameters $(b_1, b_2, ..., b_m)$ for a given compression characteristics. To obtain the paramenters in a short time, an interpolating method may be used for $m \geq 7$[8].

3.2 Architecture of the Proposed Compressor

We suppose that the input and output audio signals of the proposed compressor are represented in a fixed-point binary number representation, called the two's complement representation, as follows,

$$x = x_0.x_1x_2 \cdots x_{n-1}, \quad (18)$$

where $x_i \in \{0, 1\}$ for $i = 0, 1, 2, \cdots, n-1$, and x_0 expresses the sign of x. The value of x is obtained by using the following equation,

$$x = -x_0 + \sum_{i=1}^{n-1} x_i 2^{-i}. \tag{19}$$

Obviously, x has a value range of $[-1, 1)$. the number representation is also applied to the inner arithmetic circuits of the proposed compressor. A pipeline-type architecture of the compressor is shown in Fig.3, in which REG-P and REG-V are two pipeline registers. The block CMP implements (13) and (14), and the main arithmetic circuits are the multipliers for computing the polynomial expression and implementing the attack/release function and the divider.

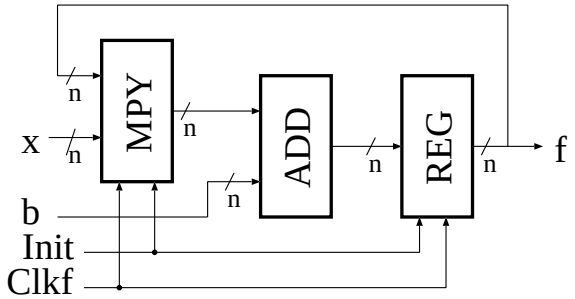


Figure 4: Arithmetic circuit for computing a polynomial expression.

We consider the polynomial expression of degree m given in (17), which can be calculated by performing $2m$ times of multiplications and m times of additions. We can use the Honner's rule to calculate the polynomail as follows:

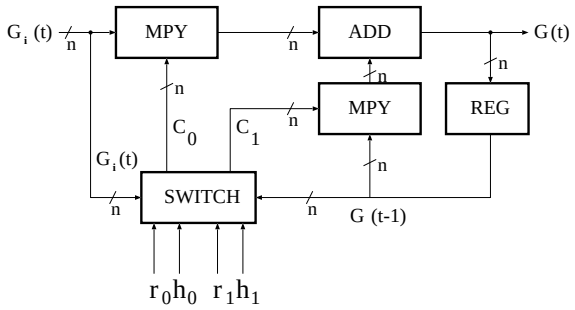
$$\begin{aligned} f_m(x) &= b_1 x + b_2 x^2 + ... + b_m x^m \\ &= ((\cdots((b_m x + b_{m-1})x \cdots + b_2)x + b_1)x. \end{aligned}$$

Therefore, the above calculation can be implemented by performing the following product-sum operation repeatedly m times,

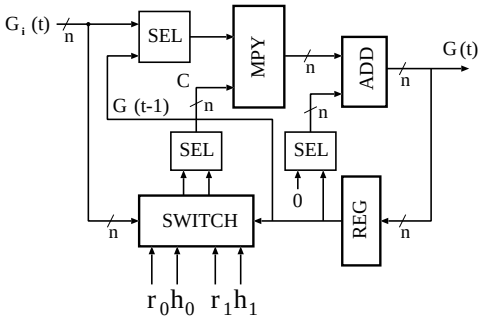
$$\begin{cases} f_i = f_{i-1} \cdot x + b_{m-i} \\ f_0 = b_m \end{cases}, \tag{20}$$

and the arithmetic circuit for the polynomial expression is designed as shown in Fig. 4.

Figure 5(a) shows an attack/release circuit performing two multiplications and one addition for the gain data from each signal sample. The circuit SWITCH switches parameters (C_0, C_1), by comparing $G(t-1)$ with $G_I(t)$, between (h_0, h_1) for the



(a) Original circuit



(b) Modified circuit

Figure 5: Attack/release circuit.

attack time control and (r_0, r_1) for the release time control, respectively.

$$(C_0, C_1) = \begin{cases} (h_0, h_1) & (G_i(t) > G(t-1)) \\ (r_0, r_1) & (G_i(t) \le G(t-1)) \end{cases}, \tag{21}$$

where t denotes a sampling time. The parameters, (h_0, h_1) and (r_0, r_1), are obtained by the following equations.

$$h_1 = exp(-1/(f_s \cdot T_a + 1)), \tag{22}$$
$$h_0 = 1 - h_1, \tag{23}$$
$$r_1 = exp(-1/(f_s \cdot T_r + 1)), \tag{24}$$
$$r_0 = 1 - r_1, \tag{25}$$

where f_s is the sampling frequency of a digital audio system. In the circuit,

$$G(t) = C_1 \times G(t-1) + C_0 \times G_i(t), \tag{26}$$

is calculated using two multipliers, one adder and a register. To reduce the hardware resources, we perform the calculation in two steps as follows:
[Attack/release time control]

step 1 $REG := C_1 \times G(t-1)$;

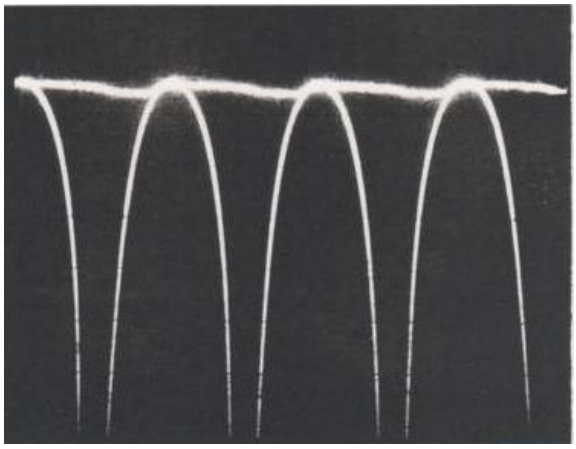


Figure 6: The gain smoothed by attack/release circuit.

step 2 $G(t) := C_0 \times G_i(t) + REG.$

Thus, the attack/release function can be implemented by using one multiplier and some selectors as shown in Fig.5(b). The attech/release circuit is designed not only to make the sound effects but also to smooth the gain $G_i(t)$. Fig.6 illustrates the smoothed gain when the input is a sine wave.

3.3 FPGA design for the arithmetic circuits

For the implementation of the proposed compressor, we use a field programmable gate array(FPGA) chip, EP20K200EFC484-2X from Altera, as the target device. In the FPGA chip, there are 8,320 logic elements (LEs) with the 0.22μ VLSI process. One LE can implement a four-input combinational logic and one register. Carry-chains are equipped for fast carry propagations between LEs during additions. We use a hardware description language, VHDL, to describe the arithmetic circuits of the compressor. Then the circuits are synthesized by using FPGA library of Altera and mapped into the FPGA chip EP20K200EFC484-2X.

As mentioned above, the multiplication and division circuits are most complicated parts in the proposed compressor. To realize a compact FPGA design, we implemented the multiplier and the divider using a shift-accumulation algorithm and restoring division algorithm, respectively. An n-bit multiplier is designed with an n-bit adder, one $2n$-bit and one n-bit register, and the output is the MSB-side n bits of the multiplication result. The divider has a similar structure with the multiplier.

The resulting amounts of hardware resources used in the compressor and the clock frequencies for 16-bit, 24-bit and 32-bit compressors are summaried in Table 1 and Table 2.

Table 1: Resource used in main circuits of the 16-bit compressor.

Elements	MPY	DIV	TOTAL
LEs	48	65	531
Registers	31	32	301

Table 2: Resource used in compressors.

Wordlength	16-bit	24-bit	32-bit
LEs	560	761	982
Pins	176	103	139
Registers	301	470	579
Clock Freq.(MHz)	100.17	80.36	56.08

4 Experiments and error analysis

Figure 4 shows the compression characteristics using polynomial of degree seven, in which the threshold level is set to -40 dB and the compression ratios are set to 1, 1.4, 2, 4, 6, 10, respectively. The parameters of the polynomials were obtained by using the interpalating method. and the characteristics are close to the ideal ones.

We calculate the mean error between the approximation characteristics and the ideal ones for the performance evaluation of the presented design method by the following equations,

$$\Delta_k = V_o(V_k) - V_{oM}(V_k), \quad (27)$$

$$\sigma^2 = \frac{{\Delta_1}^2 + {\Delta_2}^2 + \cdots + {\Delta_n}^2}{n} = \frac{\sum {\Delta_i}^2}{n} \quad (28)$$

$$\sigma = \sqrt{\frac{\sum {\Delta_i}^2}{n}}, \quad (29)$$

where n is the number of the input-output signal level samples, and $V_o(V_k)$ and $V_{oM}(V_k)$ are the output level values on the ideal characteristic and the approximation one, respectively.

Table 3: The mean error(dB)

$V_T = -40(dB), p = 2$			
degree	16bits	24bits	32bits
$m = 3$	0.710865	0.710425	0.710396
$m = 7$	0.330453	0.330448	0.330442

Table 2 shows the mean error for the implementation with the polynomial expressions of degree three

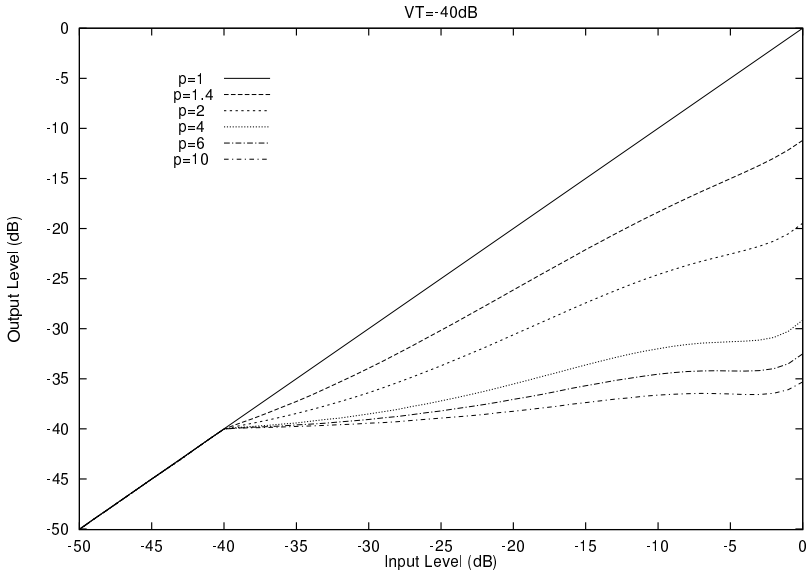


Figure 7: The compression characteristics by VHDL simulation.

and degree seven, respectively. For $V_T = -40dB$ and $p = 2$, the mean errors for 16-bit, 24-bit and 32-bit compressions have almost the same values. However, when $V_T = -50dB$, for example, the larger wordlength makes better compression characteristics.

5 Conclusions

An FPGA implementation method of a dynamic range controller, compressor, has been presented, by using a polynomial expression. Thus, the power transformation for getting the compression characteristic is converted into the calculations of additions and multiplications, which could be easily implemented by arithmetic circuits.

To evaluate the performance of the preposed compressor, compressors with 16-bit, 24-bit and 32-bit wordlengths, respectively, have been designed and simulated by using a hardware description language, VHDL. The design and simulation results show that the ideal input-output characteristic can be achieved by using a polynomial of degree three or a higher degree. The implemented compressor may be integrated into an audio system on an FPGA chip for practical use.

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