Target Identification Method by Adaptive GO-CFAR Processor and DSP Implementation for Radar System

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Abstract: - This paper presents a Greatest Of CFAR (GO-CFAR) detection scheme based on Censored Video Integration (CVI) that is increased detection probability of useful targets in noise environment and describes the Digital Signal Processor (DSP; ADSP-21160) implementation of adaptive GO-CFAR for radar system. Many signal processing algorithms are required high performance in real-time applications but it often means a high computational load for many conventional processors. This paper is proposed to appropriate hardware architecture for signal processing that target detection based on adaptive GO-CFAR processor in noise environment. The architecture has been designed with four DSP and has been implemented on four DSP processors with a good performance improvement over software implementations. Results are presented that the proposed hardware system could perform the real-time adaptive GO-CFAR processor and display of real-radar video.

Key-Words: - DSP Implementation, Radar, Signal Processing, Adaptive GO-CFAR, CVI

1 Introduction

In a real-radar system, the major problem is to detect useful targets in noise environment [1]. The decision of useful target is made according to the criterion by using a detection threshold [2]. CFAR have been widely used to extract targets from the background under noisy environments in application areas such as image processing, medical engineering, power quality analysis, surveillance system and among others [3][4].

The threshold of CFAR algorithm has problems that decrease the detection performance and increase of false alarm rate. To solve these CFAR problems, we propose a design method for adaptive GO-CFAR processor that based on CVI and GO-CFAR [5][6].

To implement adaptive GO-CFAR processor processing of radar video signal in real-time, it is necessar to have enough processing power to process a huge amount of radar data in a very short time. For this purpose, a radar extractor realized in a multiprocessor environment has been developed. ADSP-21160 is optimized for high performance. The performance of DSP that is includes an 80MHz core and has a 12.5ns instruction cycle time.

In this paper, According to the computer simulation of adaptive GO-CFAR processor, confirmed the detection probability of useful targets. The signal generator used for radar signal of computer simulation. In order to apply the adaptive GO-CFAR processor to DSP, real-radar signal is used. By the experimentation with DSP and real-radar signal, confirm the performance of adaptive GO-CFAR processor.

2 Analysis of Proposed Method

2.1 Analysis of CVI

Non -Coherent Integration (NCI) [7] is method to use the amplitude of signal to integration, and CVI is one of the NCI. CVI is carried out the pulse integration about the effectively a compromise between video integration and order statistics integrations. The output of CVI is given by equation (1).

$$y = (N-K)\cdot x_K + \sum_{j=1}^{K} x_j \quad \cdots\cdots (1)$$

And detection probability for CVI is given by equation (2).

$$P_D = \exp(-T\cdot D)\sum_{r=0}^{K-1}\frac{(T\cdot D)^r}{r!} \quad \cdots\cdots (2)$$

Where, T is threshold, $D = 1/(1+SNR)$ and N is number of integrated pulse. Figure 1 shows the block diagram of CVI.

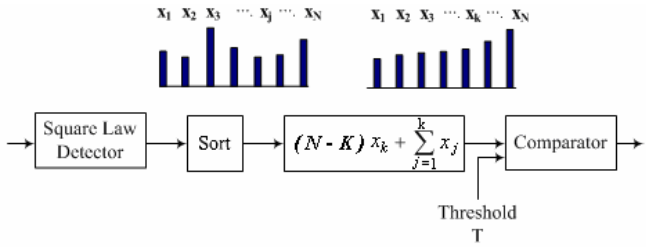

Figure 1. Block Diagram of CVI

2.2 Analysis of GO-CFAR Processor

GO-CFAR is called maximum mean-level detector and keeps CFAR state without excessive false alarm in clutter edge. According to analysis of GO-CFAR processor, we can calculate the false alarm, threshold and detection probability. Figure 2 shows the block diagram of GO-CFAR processor.

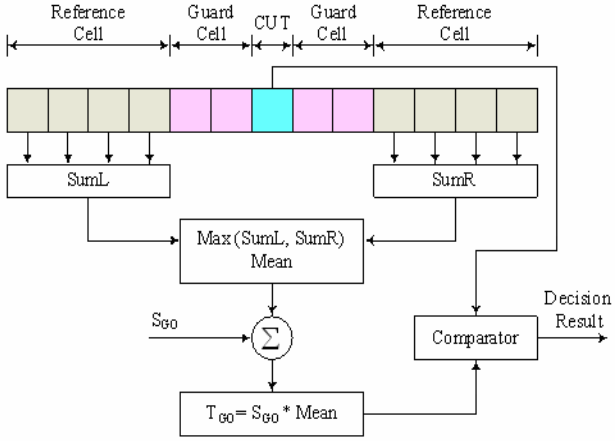

Figure 2. Block Diagram of GO-CFAR

The threshold T_{GO} of the GO-CFAR processor is given by equation (3).

$$T_{GO} = \max(Y1, Y2) \cdots\cdots (3)$$

Where, $Y_1 = \sum_{i=1}^{n} x_i$, $Y_1 = \sum_{i=n+1}^{2n} x_i$ and n is window size.

The probability distribution function of T_{GO} defined in equation (4)

$$f(x) = f_1(x)F_2(x) + f_2(x)F_1(x) \cdots\cdots (4)$$

Where, f_1 and F_1 are the probability distribution function and cumulative distribution function, respectively of the random variable Y_i, for $i = 1, 2$.

The false alarm probability is given by equation (5).

$$P_{fa} = E_X(P_r(Y \rangle XT \setminus H_0)) = M_X(-\frac{T}{u}) \cdots\cdots (5)$$

Where, $E_X()$ represents the mean over X and $M_X()$ represents the moment generating function of X. From the equation (3) and moment generating function of S_{GO}, the false alarm probability is obtained by equation (6).

$$P_{FA} = 2(1+S_{GO})^{-n} - 2\sum_{i=0}^{n-1}\binom{2n}{2}+i-1 \times (2+S_{GO})^{-(n+i)} \cdots (6)$$

Where, n is window size, P_{FA} is false alarm probability for GO-CFAR, S_{GO} is threshold multiplier of GO-CFAR.

The equations of threshold about GO-CFAR processor is as follows.

$$T_{GO} = S_{GO} \bullet \frac{MAX\left[\sum_{i=1}^{n} x_i, \sum_{i=n+1}^{2n} x_i\right]}{2n} \cdots\cdots (7)$$

2.3 Adaptive GO-CFAR Processor

In order to design of adaptive GO-CFAR processor, the threshold is established by calculation about equation (7).

The threshold that is established in GO-CFAR processor becomes feedback to comparator in CVI and improves the performance of detection probability about equation (2). By improved detection probability, maximum mean level is changed and the performance of threshold is improved in GO-CFAR processor.

Figure 3 shows the construction of adaptive GO-CFAR processor.

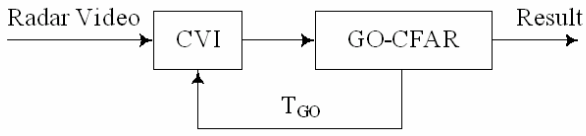

Figure 3. Construction of Adaptive GO-CFAR Processor

The performance of adaptive GO-CFAR processor was evaluated by simulation

3 Computer Simulation of Adaptive GO-CFAR Processor

The performance of the proposed adaptive GO-CFAR processor is analyzed in the section using simulated data. These data were selected in such a way that the performance of CVI and GO-CFAR processor can be demonstrated in the presence of multiple targets or target near a clutter edge. Table 1 shows the parameters of radar and adaptive GO-CFAR.

Table 1. Parameters of Radar and GO-CFAR Processor

Parameter	Value
Transmit Power	25KW
Antenna Gain	35dB
Radar Loss	0.37dB
PRF	4.8KHz
SNR	6.5dB
Sample Rate	60MHz
Window Length	16
Guard Cell	8
False Alarm	10^{-6}
Threshold Multiplier	0.983

Figure 4 shows generated signal by signal generator

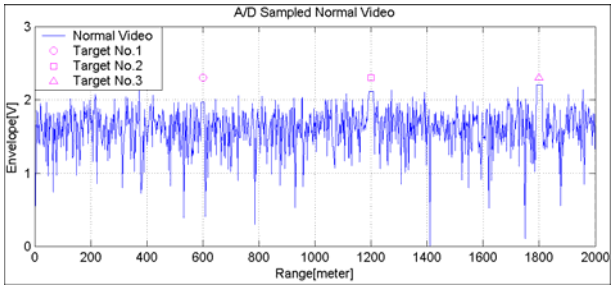

Figure 4. Generated Signal by Signal Generator

Generated signal has three targets in noise environment. Figure 5 shows simulation results by GO-CFAR processor.

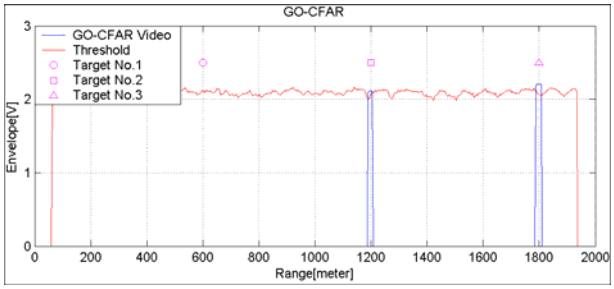

Figure 5. Simulation Result about GO-CFAR

As shown in Figure 5, GO-CFAR processor misses the target lying near the edges of the clutter and in the lower side of them. This is due to the extension of the clutter region on each side and threshold level is not matched about the radar specification. As a result, only two targets are detected. Figure 6 shows simulation results by adaptive GO-CFAR processor.

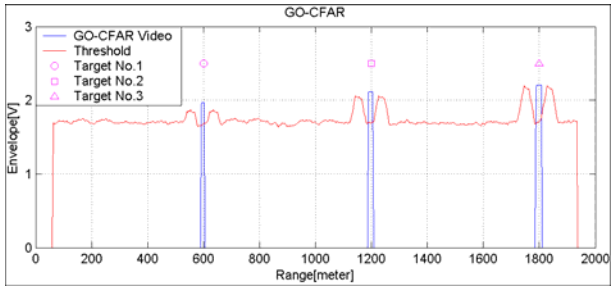

Figure 6. Simulation Result about Adaptive GO-CFAR

As shown in Figure 6, the most suitable threshold level is identified by adaptive GO-CFAR processor. It is worth mentioning that the clutter region is not enlarged so that targets are easily detected

4 DSP Hardware Implementation Method

A digital signal processor's data format determines its ability to handle signals of differing precision, dynamic range, and signal-to-noise ratios. Because floating-point DSP math reduces the need for scaling and probability of overflow, using a floating-point DSP can ease algorithm and software development. The extent to which this is true depends on the floating-point processor's architecture.

ADSP-21160 is a high-performance 32-bit DSP for medical imaging, communications, military, audio, test equipment, 3D graphics, speech recognition, motor control, imaging, and other applications. This DSP architecture balances a high performance processor core with high performance buses.

4.1 Hardware Description of DSP and DSP Board

Adaptive GO-CFAR processor is applied DSP board with four DSPs (ADSP-21160; Analog Device). And DSP board has SharcFIN ASIC, a 512MB bank of

SDRAM, 2MB bank of flash RAM and a PMC+ site. Figure 7 shows the block diagram of DSP board.

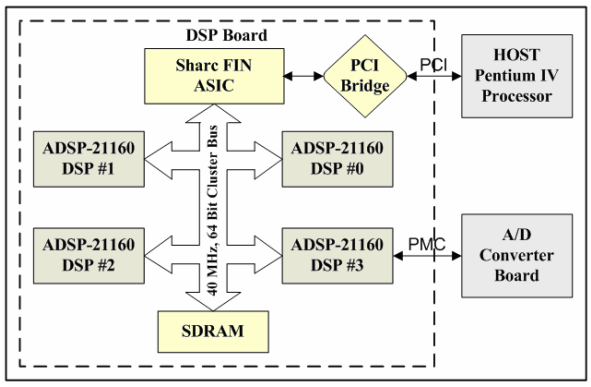

Figure 7. Block Diagram of DSP Board

4.2 Implementation Method of Adaptive GO-CFAR Processor

To develop the application code in DSP, using VisualDSP Target which is a software plug in for VisualDSP that allows the VisualDSP++ debugger to communicate directly with DSP board. Also use a hardware in-circuit emulator, such as the ICE emulators from Analog Devices, to debug application code.

The DSP21K-SF Toolkit provides host interface tools. The DSP21k-SF Toolkit is a complete software development kit that allows development of application code and integration of four DSPs into DSP board.

Figure 8 shows block diagram of A/D conversion and DSP implementation method of signal processing algorithms in DSP board.

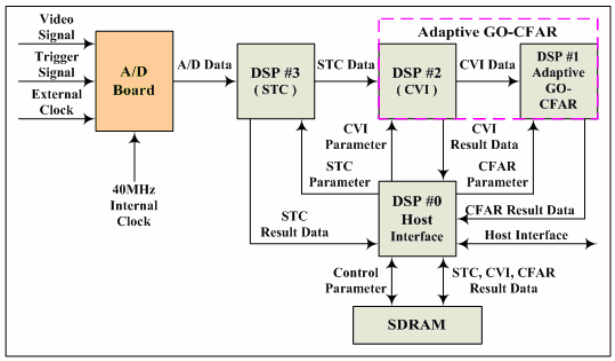

Figure 8. DSP Implementation Method of Signal Processing Algorithms in DSP Board

For DSP implementation of adaptive GO-CFAR processor, analog radar signals were converted to digital data with using A/D converter board.

DSP #3 achieves the pre-processing that is called STC.

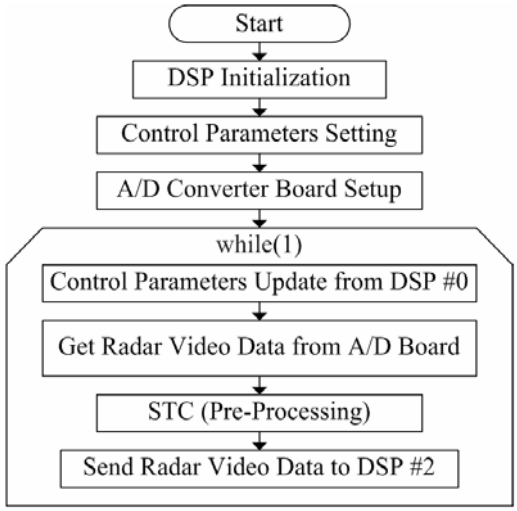

Figure 9. Operation of DSP #3

DSP #2 is achieves the CVI processing for adaptive GO-CFAR processor.

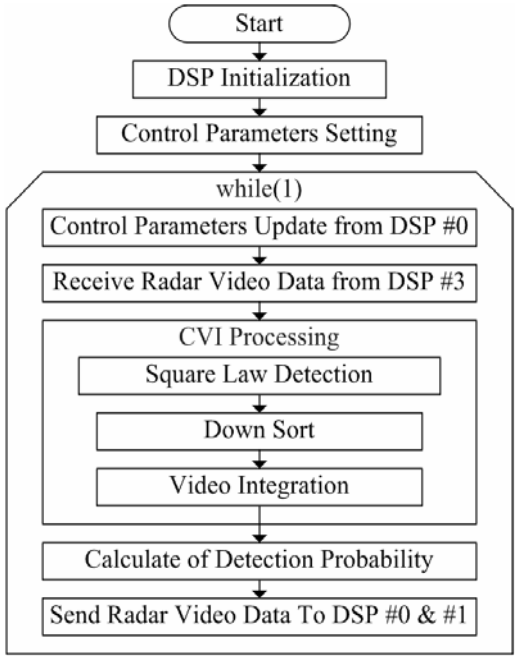

Figure 10. Operation of DSP #2

DSP #1 achieves the adaptive GO-CFAR processor.

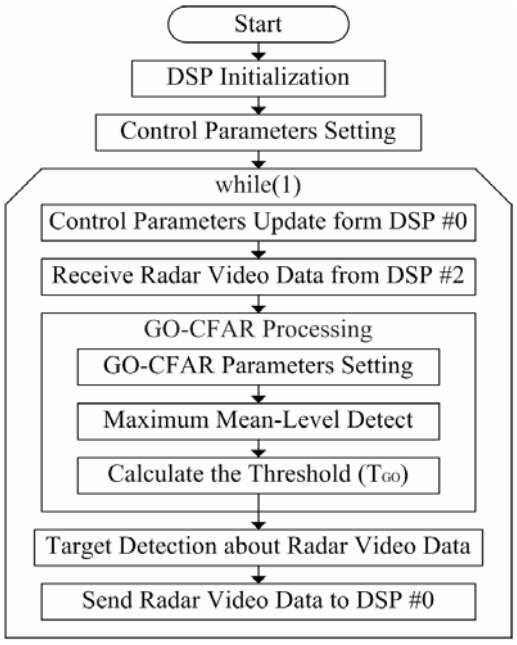

Figure 11. Operation of DSP #1

Also DSP #0 achieves the control of other DSPs and host interface.

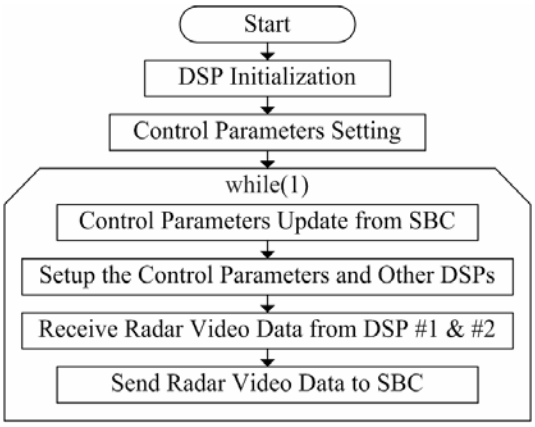

Figure 12. Operation of DSP #0

5 Conclusion

To confirm the performance of adaptive GO-CFAR processor, the experimentation is carried out in radar system. Table 2 shows the radar specification for experimentation.

Table 2. The specification of radar system

Transmit Power	25KW
Transmit Frequency	9410MHz (X-Band)
Antenna Type	Slotted Array
RPM / PRF	25RPM / 2.4KHz
Beam Width	Horizontal(1.2° ± 0.2°) Vertical(22°)
Range Resolution	Within 25m
Range Accuracy	MAX 0.9% of Range Scale
Bearing Resolution	1.8°
Bearing Accuracy	1° or less
SNR	6.5dB or less
Sample Rate	60MHz

We have proposed the adaptive GO-CFAR processor that is applied DSP. For the performance of the proposed processor, we will compare the proposed processor with GO-CFAR processor.
Figure 13 shows the experimental result that didn't achieve the CFAR processor in radar system.

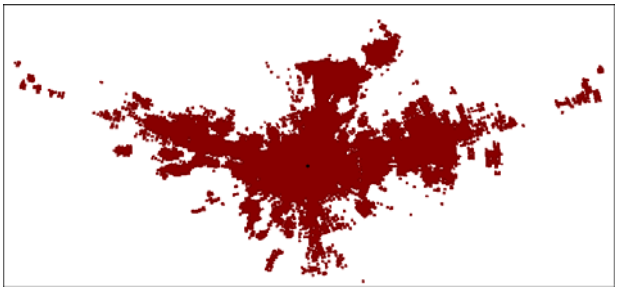

Figure 13. Radar Display without CFAR Processor

Figure 14 and Figure 15 show the experimental result that achieve the GO-CFAR processor and proposed adaptive GO-CFAR processor.

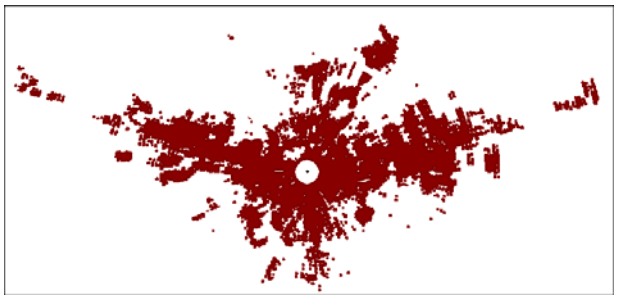

Figure 14. Radar Display by GO-CFAR

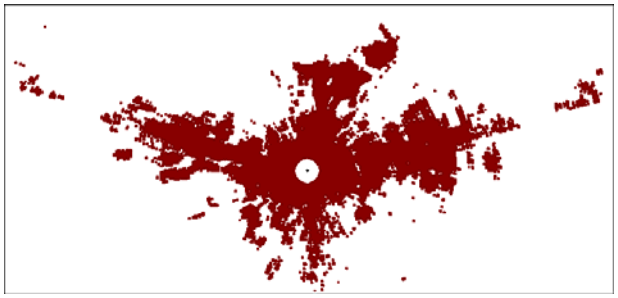

Figure 15. Radar Display by Adaptive GO-CFAR

As shown in Figure 14 and Figure 15, two processors reduce the edge clutter and display the more definite target from radar video. But the proposed processor has better optimal performance than GO-CFAR.
Table 3 shows the experimental result about threshold multiplier about CFAR processors.

Table 3. Threshold Multiplier of CFAR Processors

Processor	Threshold Multiplier
GO-CFAR	1.157
Adaptive GO-CFAR	0.983

As shown in Table 3, proposed processor has most suitable threshold multiplier that is identified by adaptive GO-CFAR processor.
This paper proposed the adaptive GO-CFAR processor that based on CVI and GO-CFAR processor. The proposed processor is identified the threshold multiplier about GO-CFAR processor and applied DSP board to display radar video signal.
The results of proposed processor are as follows:
1. The performance of the CFAR processor was studied by means of computer simulation.
2. When applied suitable threshold multiplier by proposed processor, the experimental results showed that exactly detection of useful target in noise environment.
3. The proposed hardware system could perform the real-time adaptive GO-CFAR processor and display of real-radar video.

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