Implementation of Flight Control Computer Hardware Using the C6701 Processor

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Abstract: Flying Test Bed (FTB) program is to establish the in-house capability of digital flight control computer (DFLCC) development which will be installed on the existing Korean Supersonic Aircraft (KSA). A hardware manufacturing technology of DFLCC mainly lies in constitution and layout of central processing unit (CPU), and input output processor (IOP) board which includes core processor, with those of other boards. The FTB DFLCC has triplex digital redundancy architecture. We use to DFLCC rapid prototyping (RP) to help the participants perform design review and function analysis easily. In this paper, we present the establishment and implementation of FTB DFLCC hardware using the SMJ320C6701 processor and RP. Also, channel valid logic and cross channel data link (CCDL) are described for redundancy management.

Key-Words: Digital Flight Control Computer (DFLCC), SMJ320C6701, Flying Test Bed (FTB), Korean Supersonic Aircraft (KSA), Flight Control System (FCS). Central Processing Unit (CPU), Input Output Processor (IOP), Rapid Prototyping (RP).

1 Introduction

The Korean Supersonic Aircraft (KSA) is to prepare future pilots for current and next-generation fighters such as F-15, F-16s, the F/A-22, F-35 and the Euro-fighter. The aircraft is powered by a single General Electric turbofan engine, type F404-GE-102, with Full Authority Digital Electronic Control (FADEC). The primary flight control surfaces are composed of Left Horizontal Tail (LHT), Right Horizontal Tail (RHT), Left Flaperon (LF), Right Flaperon (RF), and Rudder, and the secondary surface is a Leading Edge Flap (LEF). The KSA, which is flying test bed (FTB) aircraft, will be used to teat and evaluate domestic developmental digital flight control computer (DFLCC). Flight controllability and stability is controlled by DFLCC to drive actuator for moving control surfaces. The hardware and software development of DFLCC is the core technology to maximize not only aircraft controllability and stability but also maneuvering and flight performance. The Fly-By-Wire (FBW) system utilizes triplex redundant pilot-operated force transducers to produce flight control command signals. The control commands are combined with aerodynamic data and gyro rate and acceleration data by a three-channel flight control computer. The computer produces three channel electrical commands for operation of the Direct Drive Valves (DDVs) that control the motion of the flight control surface hydraulic actuators [1]. The FTB DFLCC hardware is composed of central processing units (CPUs), input output processor (IOP) boards, analog discrete input output (ADIO) boards, actuator control servo (ACS) boards, discrete output (DOUT) boards, power supply (PS) boards, and housing. The digital signal processor (DSP) of the FTB DFLCC is SMJ320C6701 from Texas Instruments (TI™). In this paper, the design and implementation of triple redundancy DFLCC hardware based on the C6701 processor is described. Also, we present the technology of redundancy management. The rest of this paper is organized as follows: In section 2, we briefly review the flying test bed flight control system overview. Section 3 describes the hardware design and implementation. Section 4 gives and discusses the redundancy management for increasing survivability and reliability. Section 5 provides the conclusion of this paper.

2 FTB FCS Overview

The DFLCC, which is core in flight control system (FCS), is to enhance flight stability and to improve maneuvering according to pilot control command, and to increase aircraft survivability and reliability. This

also commands to drive actuators for implement control laws from air data sensor, aircraft motion sensor, and mission computer, etc. The functions of DFLCC are as the following

- to provide primary flight control,
- to operate triple redundancy sensor input,
- to provide +28VDC and Battery Backup,
- to receive pilot control command, aircraft motion sensors, air data sensor,
- to provide 1553B MUX signal and RS422 interface, and
- to provide actuator drive command signal : Left Horizontal Tail (LHT), Right Horizontal Tail (RHT), Left Flaperon (LF), Right Flaperon (RF), Rudder, Leading Edge Flap (LEF)

The FCS major components of the FTB aircraft are shown in Fig. 1. Fig. 2 shows the block diagram of the FCS.

The FTB FCS has been designed to provide satisfactory aircraft handling qualities and to ensure an acceptable level of performance achievement. To provide the KSA with enhanced operational capability, the airframe is being designed with relaxed static stability (RSS). In order to maintain control of an aircraft designed with RSS, electronic augmentation in the form of a digital FCS being utilized. The architecture for the FTB FCS is comprised of redundant sensors, redundant DFLCC hardware executing real-time command and control software, and multiple surface actuators.

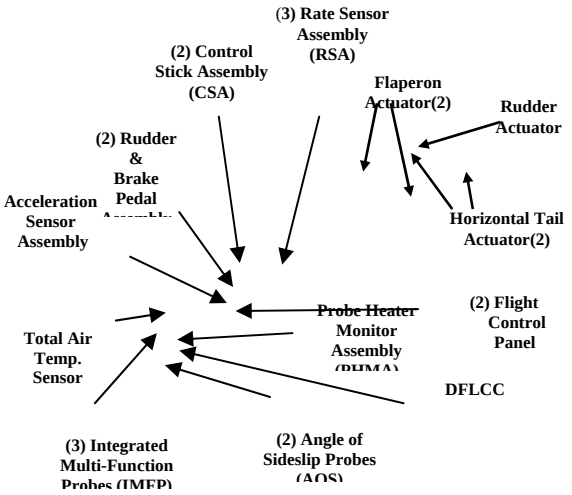

Fig. 1. The FTB FCS major components

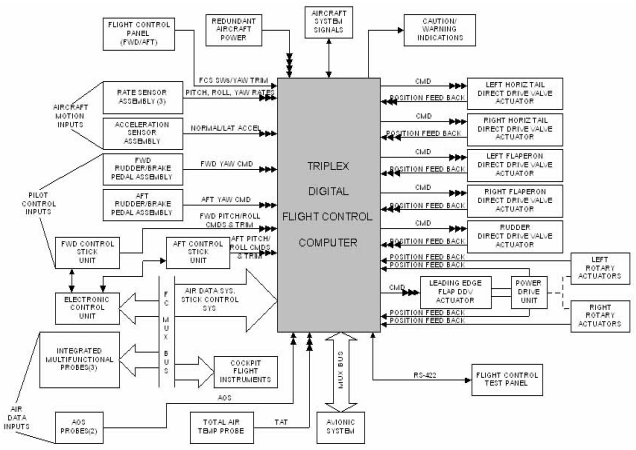

Fig. 2. Block Diagram of the FTB FCS.

The DFLCC includes the digital electronics to store and process the software and the hardware to handle all the input and output functions between DFLCC and other systems on the aircraft (sensors, avionics subsystems, surface actuators, etc.). The software is referred to as the operational flight program (OFP) and it contains all the computations or algorithms necessary to process the sensor information, to calculate the appropriate surface commands, to detect and isolate component failures, and to maintain a record of failures for the pilot(s) or maintenance personnel. The DFLCC is accomplished by performing the digital computations on the triple redundant sensor inputs. These sensors are responsible for measuring the aircraft motion, the pilot's control inputs, and the atmospheric conditions. The outputs of the DFLCC are control signals used to drive the five primary control surfaces and the one secondary surface through DDV actuators/PDU. In addition to providing stability and command augmentation, the FLCC will, when loaded with the OFP software, monitor interfacing subsystem signals, manage redundant functions, isolate interfacing subsystem failures that affect flight safety or degrade the performance of the primary flight controls, and validate non-redundant data. Cross-channel voting will be used by the OFP to perform pre-flight and in-flight assessments on the health of the triplex system.

3 Rapid Prototyping

Development of DFLCC hardware requires integration of various of technologies. So, the stakeholders should share the same idea through the entire development life cycle and efficient

communication shall ensure the successful development. Model based design concept is popular now in the hardware and software design[2, 3, 4]. We use to methodology of RP to design systematically. The main idea is to develop virtual environment where engineers can systematically review the design information like signal flow diagram, logic diagram, function block diagram, control block diagram, circuit diagram, circuit card assembly drawing, circuit elements information, etc. and verify the function and operation of the DFLCC by simulation. Design issues is solved insert thermal layer inside printed circuit board (PCB) to conduct cooling, relocate component layout in PCB, etc. using RP technology.

4 Hardware Design and Implementation

The FTB DFLCC is implemented using the present-generation SMJ320C6701 processor from TI™ for CPU and SMJ320C6203 for IOP. DFLCC is composed of three CPU/IOP cards, three ADIO cards, six ACS cards, three DOUT cards, three sets (9 cards) of PS board, an EMI filter, a chassis, and a motherboard. The configuration of the FTB DFLCC hardware is shown in Fig. 3.

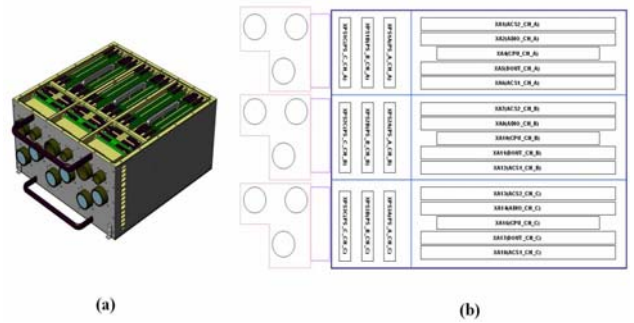

Fig. 3. Configuration of the FTB DFLCC Hardware: (a) Layout and (b) Motherboard.

4.1 SMJ320C6701 DSP Architecture

The SMJ320C6701 is the floating point processor that uses the high-performance advanced very-long-instruction-word (VLIW) architecture developed by TI™. As shown in Fig. 4. the SMJ320C6701 core is divided into two data paths (A, B), each with the same set of four independent functional units, a register file with sixteen 32-bit general-purpose registers, and paths for addressing and moving data between memory and registers[5,6]. All four functional units in each data path support integer operations. With three floating point units per data path, the SMJ320C6701 is capable of up to six floating point operations or two multiply-accumulates (MACs), per clock cycle, for a total of a giga floating-point operations per second (GFLOPS) or 334 million MACs, at clock rate of 167MHz.

The C6701 has 128 Kbytes of on-chip memory, evenly divided between program and data space. The on-chip program memory has a dedicated 256-bit path to the CPU core, allowing it to fetch a 256-bit VLIW instruction packet with eight 32-word instructions, one per functional unit, every clock cycle. In contrast, all off-chip memory access, whether it is a program or data fetch (or store), occurs through the 32-bit external-memory-interface (EMIF) bus, thus requiring at least eight cycles to fetch the same VLIW packet. Since the off-chip access rate is at least one cycle per 32-bit word, the C6701 must execute using on-chip program memory for good performance.

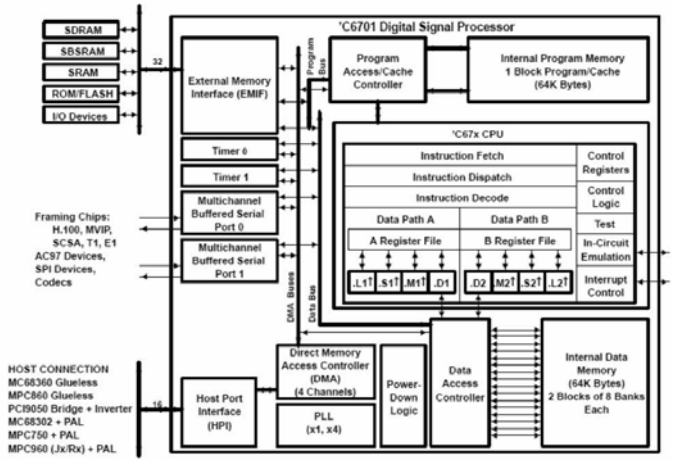

Fig. 4. SMJ320C6701 Functional and CPU Block Diagram. Courtesy of Texas Instruments, Inc.

4.2 CPU/IOP Board

The CPU/IOP board is divided into CPU part and IOP part[7]. While the CPU part provides C6701 processor to execute OFP and to compute flight control algorithm, the IOP part achieves the management of analog input/output and discrete-time input/output using command received from CPU through dual port random memory access (DPRAM). The major components of CPU part are CPU (SMJ320C6701), flash memory, synchronous static RAM (SSRAM), static RAM (SRAM), non volatile RAM (NOVRAM), DPRAM, 1553 MUX controller, universal asynchronous receiver and transmitter (UART), complex programmable logic device (CPLD), etc. The

inside of CPLD is composed of address decoder, parity generator/checker, clocks, DIN, DOUT, DIO bus, interrupt encoder, channel valid logic, etc. The components of IOP part are CPU (SMJ320C6203), flash memory, DPRAM, analog to digital converter (ADC), digital to analog converter (DAC), analog MUX, 8bit DIO bus, CPLD, etc. The block diagram of the CPU/IOP board is shown in Fig. 5.

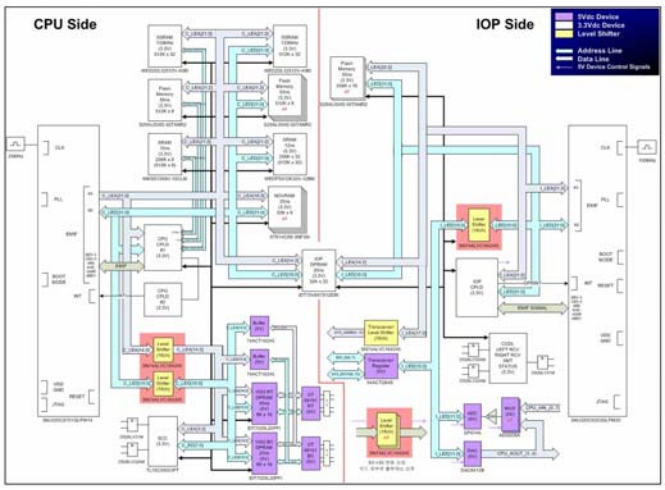

Fig. 5. Block diagram of the CPU/IOP board.

4.3 ADIO Board

The ADIO board accomplishes the input/output function of analog and discrete-time signal. ADIO board creates analog built-in test (BIT) stimulation (STIM), discrete-time BIT STIM, ACS BIT STIM, pulse width modulation (PWM) BIT STIM, acceleration sensor assembly (ASA) torque test signal, etc. The block diagram of the ADIO board is shown in Fig. 6.

4.4 ACS Board

The ACS board receives the analog-type control command signal from CPU/IOP board. It also receives the ram and actuator valve position signal from actuator and performs PWM control to drive actuators. The ACS board consists of two cards per channel. The ACS1 board controls RHT, RF, RUD surface and the ACS2 board controls LHT, LF, LEF. The block diagram of the ACS board is shown in Fig. 7.

4.5 DOUT Board

The DOUT board fulfills discrete-time signal input/output. It is a user-interface to a pilot to inform warning/caution signal and status signal of other equipment. The block diagram of the DOUT board is shown in Fig. 8.

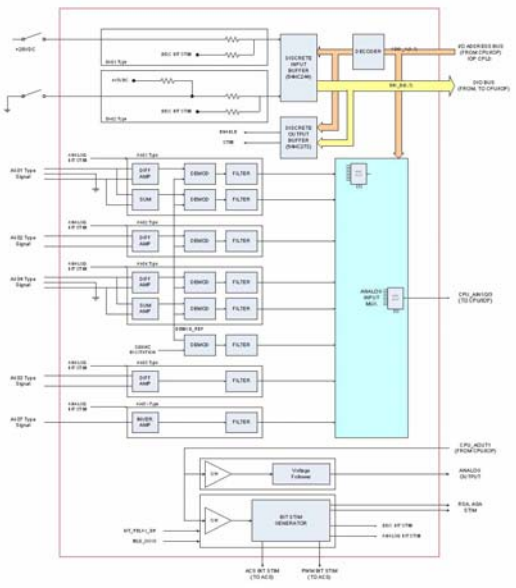

Fig. 6. Block diagram of the ADIO board.

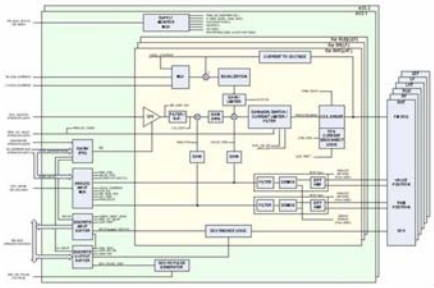

Fig. 7. Block diagram of the ACS board.

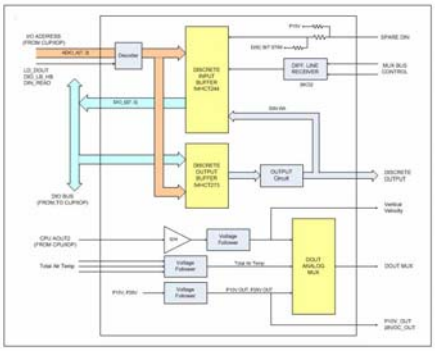

Fig. 8. Block diagram of the DOUT board.

4.6 PS Board

The PS board provides +3.3Vdc, +3.3VNVM, +5Vdc, +15Vdc, and -15Vdc to CPU/IOP board, and +5Vdc, +15Vdc, -15Vdc, and +28Vdc-select to DOUT and ACS board. It also provides +5Vdc, +15Vdc, -15Vdc, +28Vdc-select, 7VAC 3200Hz, 7VAC 3200Hz Buffer to ADIO board, and 7VAC 3200Hz, and 7VAC 3200Hz Buffer , +10V_SOV(shut off valve), +15Vdc, and -15Vdc to external equipments. The block diagram of the PS board is shown in Fig. 9.

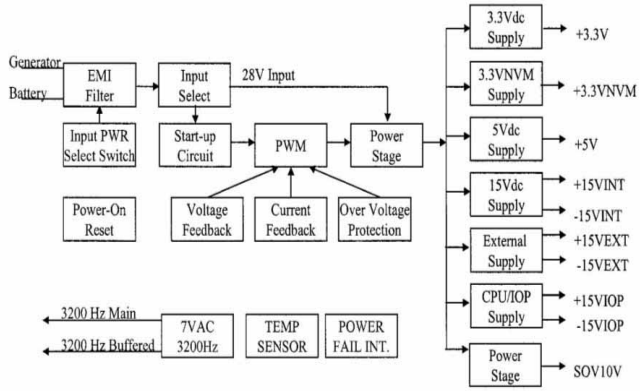

Fig. 9. Block diagram of the PS board.

5 Redundancy Management

The FTB DFLCC utilizes triplex digital redundancy architecture. It is designed to perform asynchronous operation. However, provisions are included to permit computational frame synchronization between DFLCC branches using the software. Inter-channel discrete-time signal directly readable by the CPU (i.e., without the need of the IOP) is provided. The CPU is interrupted by any transition of these discrete-time signals. Synchronization interrupts may be disabled by the CPU.

5.1 Channel Valid Logic

Each channel of the DFLCC contains the logic to prevent a failed processor from commanding the control surfaces. The channel fail logic is designed that logic state changes for a channel failure are prohibited. The block diagram of the channel valid logic is shown in Fig. 10

5.2 Cross Channel Data Link

The transmission of data from a channel to the other channels in DFLCC is provided via cross channel data link (CCDL). This data exchange is under control of the input/out controller (IOC). These CCDL are capable of transmission at a minimum rate of 1 Mbits/sec. Each IOC channel includes the circuitry to automatically receive data from the other channels, placing this data in memory without interventing of the channel's CPU. The IOC is designed to allow the software to command the starting address and the number of words (from 1 to 2048 words, inclusive) to be data-linked. A software flag indicating a data updated by the block is available to the receiving processor to permit data set consistency. A failure of any transmitter or receiver shall not affect an associated receiver or transmitter in any other channel. The CCDL has the capability of wraparounding transmission from a channel to the receivers in that channel. The block diagram of the CCDL interface is shown in Fig. 11.

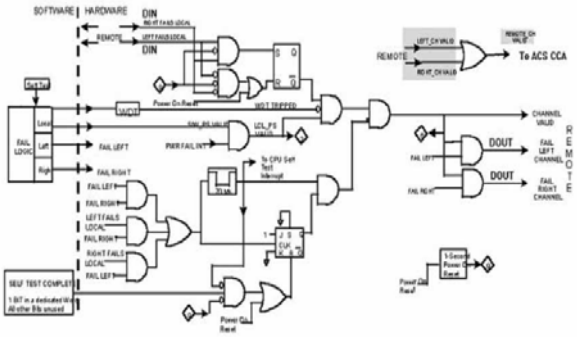

Fig. 10. Block diagram of the channel valid logic.

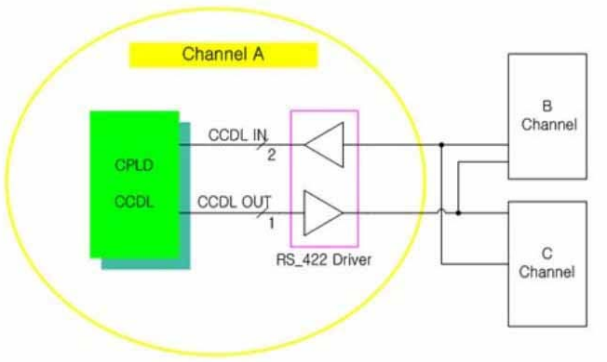

Fig. 11. Block diagram of the CCDL interface.

6 Conclusion

Development of DFLCC hardware requires the integration of various kinds of technologies. Among them, it is important to select the CPU processor and design procedure. This work has proposed and implemented FTB DFLCC hardware using the C6701

processor and RP. The FTB DFLCC hardware is composed of three CPU/IOP cards, three ADIO cards, six ACS cards, three DOUT cards, three-set (9 cards) PS board, an EMI filter, a chassis, and a motherboard. The design concepts of CPU/IOP board constituted using SMJ320C6701 and SMJ320C6203 processor are described and the functionality and block diagrams of ADIO, ACS, DOUT, and PS board are elucidated and illustrated. Also, the channel valid logic via CCDL for redundancy management is suggested and discussed.

References:

[1] Agency Defense for Development, "Prime Item Development Specification FTB Air Vehicle", D85PS0001, Jun., 2005

[2] Detlef Kochan et Al., "Rapid prototyping issues in the 21st century", *Computer in Industry* Vol. 39, 1999, pp. 3-10.

[3] D.M.C. Santos et al., "The development of 3D models through rapid prototyping concepts", *Journal of Materials Processing Technology*, Vol. 168, 2005, pp 270-272.

[4] V. K. Madisetti, M.A. Richards, "Advances in Rapid Prototyping of Digital Systems", *IEEE Guest Editor' Introduction*, Fall, 1996.

[5] Texas Instruments, Inc., "SMJ320C6701 Floating-Point Digital Signal Processor", Literature No. SGUS030B

[6] Texas Instruments, Inc., "TMS320C6000 Peripherals Reference Guide", Literature No. SPRU190D.

[7] Agency Defense for Development, "FTB DFLCC Performance Requirement", D85PS0002, Jan. 2006.