

A DVB-T/H Baseband Receiver for Mobile Environments

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Abstract: This paper presents an architecture design, FPGA implementation, and measurement results of a real-time baseband processor for DVB-T/H receiving. The proposed receiver supports 2K/4K/8K mode and all the GI ratios defined in standard with mode/ratio detection. To improve the performance in high mobile environment, the proposed channel estimation with linear prediction in pilot subcarriers and quadratic interpolation of non-pilot subcarriers provides a better estimation (at Doppler frequency 300 Hz). The FPGA implemented results give a low complexity of 139k gate counts working on 36.75 MHz clock rate.

Key-Words: DVB-T/H, OFDM, Synchronization, Channel Estimation, Baseband Transceiver, Mode Detection

1 Introduction

To provide more contents and better quality, digital TV is a trend. It can support more channels than analog systems and provide much better quality video resolution. There are several standards established for this requirement such as ATSC, ISDB-T, and DVB-T/H [1, 2, 3, 4]. DVB-T/H is now a popular (over 100 countries in the world) video broadcasting technology for the terrestrial and for handheld devices.

In DVB-T/H systems, there are no preamble, but are with plenty of pilots. To combat channel impairment, these pilots should all used for channel estimation. However, the pilots are not in all subcarriers, if the channel varies too fast, system performance will be degraded. Many researches work on how to use these pilots to against the fast time varying channel. In [5], with SIMO technologies, two dimensional (symbol index and subcarrier index) interpolation of channel response is adopted. However, this technique needs to buffer four OFDM symbols and two sets of pilots. This leads to a large hardware complexity. Some other method uses the prediction method [6]. Although the hardware cost is low, the performance is not good enough under the fast time-varying channel condition.

This paper will focus on how to estimate well the fast time-varying channel response while still maintaining the low hardware complexity. It is organized as follows. Section 2 will introduce briefly the important parameters of DVB-T/H system. Proposed transmitter and receiver architecture conforming to the standard and the related algorithms and techniques

will be discussed in Section 3. Section 4 provides the simulation results to prove the function and performance. For hardware implementation, Section 5 shows the implementation flow and implementation results. The proposed receiver compared with other related researches for performance and complexity is discussed in Section 6 and Section 7 comes to a conclusion.

2 System Description

To support high data rate and spectral efficiency, DVB-T/H standard adopts OFDM technology. Different modes (2K, 4K, and 8K) are defined for various operating ranges and Doppler tolerance. When more subcarriers are allocated in a system, the larger network it can be operated, but the tolerance for Doppler effect is less. In addition to the transmitted data in an OFDM symbol, there are several important subcarriers useful for the signal reception. The scattered pilot, continual pilot, and TPS pilot are useful for time synchronization, frequency synchronization, and channel estimation. Compared with 802.11 and 802.16 standards, there is no preamble in DVB-T/H systems. Therefore, these pilots are useful for synchronization and to combat frequency-select fading. The important system parameters for DVB-T/H is shown in Table 1.

3 Architecture Design

The proposed baseband processor deals with inner part of the transmitter and receiver. Besides com-

Table 1: Important parameters for DVB-T/H.

Constellation	QPSK, 16-QAM, 64-QAM		
# of FFT points	2K	4K	8K
# of used subcarriers	1705	3409	6817
# of continuous pilots	45	89	177
# of TPS pilots	17	34	68
# of scattered pilots	131	262	524
# of data subcarriers	1512	3024	6048
Guard interval ratio	1/32, 1/16, 1/8, 1/4		

mon OFDM processing unit, the proposed channel estimation and compensation block mentioned later can combat frequency-select fading in the high mobility environment.

3.1 Transmitter

The proposed transmitter receives the data from outer encoder and modulates the data to a QPSK/16-QAM/64-QAM symbol. After IFFT transformation and guard interval (GI) insertion, the data is sent to RF frontend for broadcasting. The frame adaption unit arranges the pilots, TPS pilots, and data subcarriers to fit the OFDM frame structure. The proposed transmitter architecture is shown in Figure 1 .

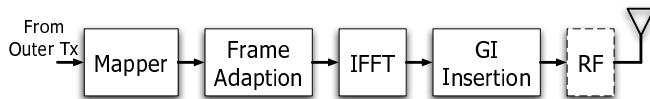


Figure 1: Proposed transmitter architecture.

3.2 Receiver

Figure 2 shows the proposed receiver architecture. The receiver consists of a signal detection unit, a carrier frequency offset (CFO) estimator/compensator, an FFT window controller, an FFT processor, a channel estimator/compensator, and a de-mapper. The first two units process time-domain signals while the last two process in the frequency-domain. In the following paragraphs, the important building blocks for the proposed receiver will be explained.

Signal Detection (Mode Detection)

Unless the signal detection unit detects the DVB-T/H signal, the other parts of the receiver will not be turned on for low power consumption consideration. Assume $r(n)$ is the receiver input signal for time n ,

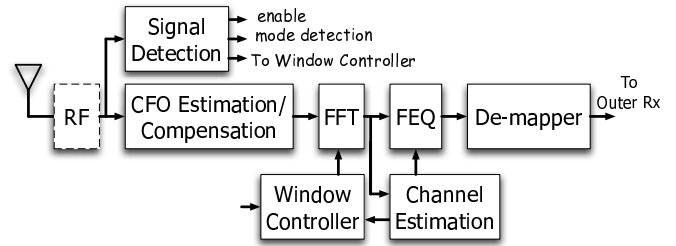


Figure 2: Proposed receiver architecture.

for the delay correlation equation below:

$$c(n) = \frac{\sum_{k=0}^{N_G-1} r(n-k-N_F)r^*(n-k)}{\sum_{k=0}^{N_G-1} r(n-k)^2}, \quad (1)$$

where N_G is the length of GI, and N_F is the length of FFT. We can scan N_F for 2K, 4K, and 8K, and scan N_G for 1/32, 1/16, 1/8, and 1/4. If there is any DVB-T/H signal, there will be a peak ($|c(n)| > 0.5$) periodically; otherwise, no peak detected. Therefore, the signal detection can be achieved. Also from the peaks' characteristics, the mode and GI ratio can be obtained.

Symbol Timing Synchronization

The signal detection unit also provide the function of symbol timing synchronization because $|c(n)|$'s peak is always at about the end of an OFDM symbol. However, the position is not the exact. So we can move the FFT window's beginning early by the amount of 1/4 of the smallest GI. This will not affect the performance and can reduce inter-symbol interference.

To maintain the FFT window boundary correctly, a simple windows controller can monitor the sample add/drop function.

Carrier Frequency Offset Compensation

Carrier frequency offset can be divided into fractional CFO and integer CFO. Delay correlation can only detect the CFO which is within one subcarrier spacing. However, during some operating modes, the CFO can exceeds multiple subcarrier spacing. Therefore, both fractional and integer CFO need to be estimated and compensated. The fractional CFO (FCFO) estimator in time domain still uses delay correlation to find the offset and compensates that before the received signal goes into FFT processor. When two

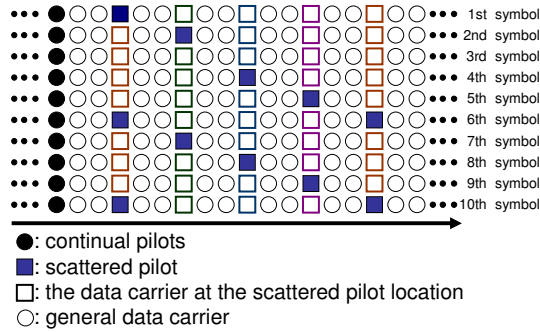


Figure 3: Continual pilots and scattered pilots.

neighboring peak values are detected, the phase difference between can be used to get the FCFO.

$$\text{FCFO} = -\frac{\angle c(n_b) F_s}{N_F 2\pi} (Hz), \quad (2)$$

where $c(n_b)$ is the phasor difference. Once the FCFO is obtained, the received signal can be compensated by a simple phase de-rotate circuit just before FFT unit.

As for integer CFO (ICFO) estimation, the property of pilot's power is larger than data's power can be used. The maximum CFO is no larger than 16 sub-carriers is defined in standard. So the ICFO can be obtained by the following equation:

$$\text{First subcarrier location} = \underset{-16 < k < 16}{\text{argmax}} \left(\sum_{p_c} R(p_c + k) \right), \quad (3)$$

where p_c is one of the location set of continual pilots.

Channel Estimation

Since the DVB-T/H standard does not have preamble, all the pilots should be used for channel estimation. Continual pilots and scattered pilots are used to provide enough information to track channel response for all data subcarriers for all times. Continual pilots always occupy the same sub-carriers. A scattered pilot occurs per twelve sub-carriers in an OFDM symbol, and shifts three sub-carriers to the next OFDM symbol. Figure 3 displays these pilots' arrangement. The proposed receiver adopts the general method to estimate the channel response where the pilots exist:

$$H(p_k) = \pm \frac{3 \times R(p_k)}{4}, \quad (4)$$

where p_k is one of the pilots set. For continual pilots in some subcarriers, the channel response can be estimated and updated every symbol time. However, in scattered pilots, the above equation can be used for only some discontinuous symbol time. Even for the

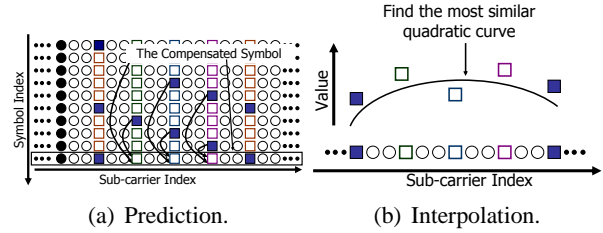


Figure 4: Steps of proposed compensation method: first, predict the channel response; second, use the regression for quadratic interpolation.

subcarriers without pilots (neither continual pilots nor scattered pilots), the channel response is also required for correct signal detection. Therefore, some methods should be used to get the channel response for each subcarrier. The proposed algorithm is as follows. First step, use linear interpolation to predict the channel response for the scattered-pilot subcarriers when the pilot transmission is off. This scenario is shown as Figure 4(a). The second step is to use the derived (sub-carrier with pilots) and the predicted (derived from the first step) channel responses for quadratic interpolation. This can derived the channel response of the subcarriers without pilots. This is shown in Figure 4(b).

In the first step, because the pilots are all in the same subcarrier, so the prediction is much more accurate than the pilots in different subcarriers. For reduction of complexity, linear prediction [6] is sufficient. This can be done with the following equations:

$$H_i(p_k - 9) = \frac{5}{4} \times H_{i-3}(p_k - 9) - \frac{1}{4} \times H_{i-7}(p_k - 9), \quad (5)$$

$$H_i(p_k - 6) = \frac{6}{4} \times H_{i-2}(p_k - 6) - \frac{2}{4} \times H_{i-6}(p_k - 6), \quad (6)$$

$$H_i(p_k - 3) = \frac{7}{4} \times H_{i-1}(p_k - 3) - \frac{3}{4} \times H_{i-5}(p_k - 3), \quad (7)$$

$$H_i(p_k) = H_i(p_k), \quad (8)$$

$p_k \in$ scattered previous pilots' location set. In a dynamic channel, especially in high mobility channel, the response varies dramatically with time (symbol index) and subcarriers. Therefore, linear interpolation can not be used. The second step in the proposed receiver adopts linear prediction of channel response with quadratic curve interpolation by considering the second-order regression results. Thus, for the equation:

$$H_i(p_k + 12n + m) = am^2 + bm + c. \quad (9)$$

use second-order regression to find the coefficient a,

b, c, the required channel response of the interpolation results can be obtained.

All the estimated channel response can be sent to the frequency-domain equalizer (FEQ) for channel compensation.

4 Simulation Results

To verify the system function and performance, a baseband channel equivalent model has been establish. It includes multipath fading (Jakes' model), Doppler effect, AWGN, CFO, and SFO. Also the multipath model F1 and P1 provided by [1] and typical urban 6 taps (TU6) multipath model [7] are included.

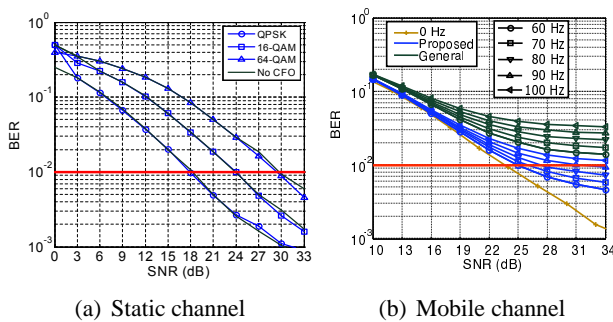
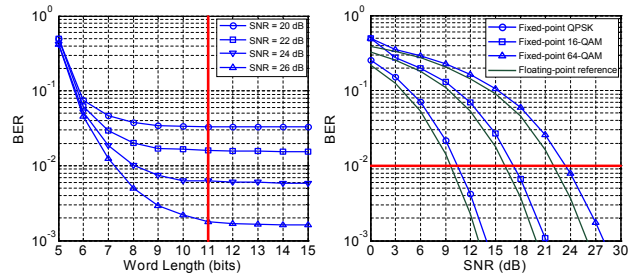


Figure 5: The performance in static and mobile channel.

Figure 5(a) shows the simulation under the condition of 2K size FFT, 1/32 GI ratio, 16 kHz CFO, 20 ppm SFO, P1 channel, and the sampling frequency is 64/7 MHz. The performance satisfies the standard requirement and presents the CFO has be compensated successfully. Figure 5(b) shows the simulation results under a mobile channel. The channel condition is the same as in Figure 5(a) except the P1 channel is replaced by TU6 channel. The results shows not only the performance satisfies the standard requirement but also with superior performance.

5 Hardware Implementation

Before hardware implementation, the word length of each signal in the building blocks have to be determined. One example is shown in Figure 6(a). If the word length is large enough, the performance will be saturated. The simulation is based on the condition of 64-QAM modulation, 2K mode, 1/32 GI ratio, and F1 channel parameters. After the word length of all signals is determined, the fixed-point system performance is shown to be about 2dB less than the floating-point system (Figure 6(b)).



(a) Word length determination. (b) Fixed-point performance.

Figure 6: Word length determination for hardware implementation. (a) Use ADC input as an example. (b) Performance comparison between floating-point simulation and fixed-point simulation.

The target system is implemented with an FPGA platform. The implemented result is shown in Table 2. The operating is 36.75 MHz. The power consumption is estimated 439 mW by FPGA utilities and is just for reference.

Table 2: Hardware Specification.

FFT mode	2K, 4K, 8K
GI ratio	1/32, 1/16, 1/8, 1/4
Clock frequency	36.75 MHz
Gate count	139 k
Power consumption	439 mW

6 Discussion

Figure 7 shows the performance comparison with other related works. Figure 7 compares the performance under mobile environment. The condition is 2K FFT, 193 Hz Doppler frequency, 1/4 GI ratio, QPSK data modulation, and TU6 channel. The proposed linear prediction with quadratic interpolation is shown to be superior to the 2D interpolation method [5]. Figure 7(b) compares the performance of ICI cancellation. The condition is 2K FFT, 1/8 GI ratio, QPSK data modulation, TU6 channel, and 300 Hz Doppler frequency. This compares the proposed architecture with some coding of the signal [8]. The proposed result is shown to be better.

Table 3 summaries the comparison mentioned above. According to the comparison, the performance and complexity is all the best.

7 Conclusion

In this paper, a DVB-T/H baseband receiver architecture design and hardware implementation is proposed.

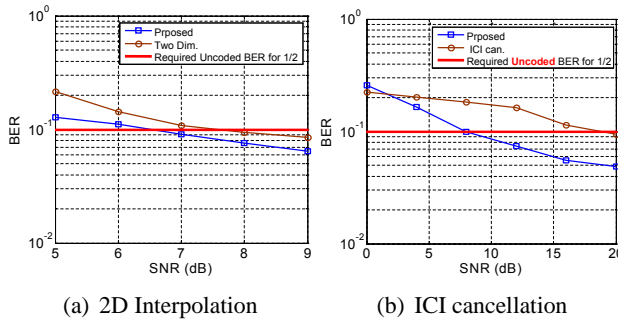


Figure 7: Performance comparison with related works. (a) 2D interpolation vs. proposed quadratic interpolation. (b) ICI cancellation with coded signal vs. proposed.

Table 3: Performance/Complexity comparison.

	[5]	[8]	Proposed
# of data buffers (6048 words)	3	1	0
# of pilot buffers (2096 words)	2	1	2
# of regular multiplier	2	1	0
# of constant multiplier	2	0	4
Hardware cost (rank)	3	2	1
Performance (rank)	3	2	1

The receiver includes a signal detector, a carrier frequency offset estimator and compensator, a symbol timing synchronization unit, a FFT processor, a channel estimator/compensator, and a de-mapper. The signal detector can not only detect the DVB-T/H signal's existence to save power but also can detect the mode (2K/4K/8K FFT) and GI ratio (1/32, 1/16, 1/8, 1/4) of the system. The proposed channel estimator adopts linear prediction for pilot subcarriers and quadratic interpolation for non-pilot subcarriers. The system performance and implementation results shows the proposed architecture not only a better performance (Doppler frequency 300 Hz and for about 1.7 dB gain) but also with low complexity (139k gate count).

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