DIFFERENTIAL CMOS CLASS-E RF POWER AMPLIFIER

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Abstract: - This paper presents a differential CMOS class-E power amplifier that exhibits high linearity. The amplifier operates at 900 MHz from ± 2.0-V, and delivers 1-W output power with 80% drain efficiency. Simulation results show that 3rd and 5th IMD products of the proposed PA are lower than that of the conventional class-E amplifier by 18 dB and 13dB respectively.

Key-Words: CMOS, Differential, Class-E, RF, Power Amplifier.

1 Introduction

Last few years have seen an increase in the popularity of the wireless communication systems. As a result, the demand for compact, low-cost, and low power portable transceivers has increased dramatically [1]. A proposed solution is single-chip radio transceiver realized in a low-cost CMOS, [2][3]. Since it is known that Radio Frequency (RF) power amplifier (PA) consumes most of the dissipated power within a transmitter, reducing its power consumption will improve the transceiver performance.

Due to its superior performance over the MOS transistors, Gallium Arsenide (GaAs) transistors have been used extensively to build high performance RF PA. GaAs based PAs have several drawbacks: costly to implement, require high level power supply, and have large size. On the other hand, CMOS power amplifier's has a limited performance because of its low breakdown voltage, low current drive, and lossy substrate. In spite of its limitation, sub-micron CMOS prove to be a good candidate process for RF PA implementation.

Recently, several RF power amplifiers have been implemented in a low-cost digital CMOS technology [4-7]. These PAs were designed for constant envelop modulation scheme which are employed by various systems such as European standard for mobile communications and Advanced mobile phone system (AMPS). The reported amplifiers utilized switching class amplifiers to achieve high efficiency and output power.

Designing a high efficiency PA for a linearly modulated RF signal such as that used in NADC is not an easy task. Traditionally, class A or AB amplifiers, which are backed off the compression point, are used in these systems. As a result, these PAs have low efficiency and low output power. Another approach is using high efficiency switching amplifiers with an additional linearization circuit [8-9]. This technique resulted in an amplifier that has good linearity, efficiency, and output power. However, the required linearization circuits usually tend to be very complex and chip's area and power consuming.

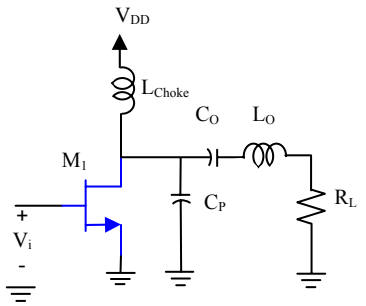

Figure.1 Single-ended Power Class-E Amplifier

The objective of this work is to design a high linearity differential CMOS class-E PA with one watt output power and high efficiency. Moreover, it should not require additional complex linearization circuit.

2 Class-E Amplifier

The conventional configuration of class-E is a single-transistor amplifier as shown in Fig. 1. Transistor M1 operates as a switch; M1 is on half cycle and off in the other half. A heavily overdriven transistor realizes switching behavior required for class-E operation. Moreover, an adequate load needs to be placed across the realized switch. The analysis of the class-E amplifiers has been reported in several papers [12-16]. Equation (1), which describes the required Z_L at the fundamental frequency, is obtained from [14]. Load at second and third harmonics need to be strong reactive load.

$$Z_L = \frac{0.28}{\omega_s \cdot C_s} \cdot e^{j49^o} \qquad (1)$$

The resonance frequency of the load is designed to be slightly higher than the fundamental frequency for two reasons: To force the fundamental current only to pass to the load and to provide the transistor with the required inductive load. In [10] and [11] the maximum class-E frequency operation (f_{max}) for a given device can be approximated as follows:
For high choke inductor [10],

$$f_{\max} = \frac{I_{\max}}{565 \cdot C_T \cdot V_{DD}} \qquad (2)$$

For finite choke inductor [11],

$$L_{choke} = \frac{0.7436}{(2\pi f_{\max})^2 \cdot C_T} \qquad (3)$$

I_{max} is the maximum current that the device can provide. C_T is the total capacitance across the transistor, which includes intrinsic capacitance, package effects and external capacitor C_P. Usually at radio frequency (RF) the intrinsic capacitance is adequate if not more than sufficient in some cases. Therefore, C_T puts a limit on the maximum operating frequency. As depicted in equation (3), f_{max} can be enhanced by using smaller choke inductor.

3 Proposed Typology

Figure 2 shows the proposed class-E output stage. Ideally, M1 and M2 act as switches; one-transistor switches on and the other off alternatively every half cycle. By proper selection of C_{p1} and C_{p2}, the resonance frequency will be the same in both half cycles, $w_o = 1/\sqrt{L_o(C_o + (C_o \cdot C_T)/(C_o + C_T)}$.
Therefore, low harmonic distortion is expected to be generated by the proposed class-E circuits. Although [13] share this feature, low harmonic distortion, it requires high driving voltage which is difficult to achieve especially with the limited supply voltage and the high linearity requirement. The LC networks at the transistors' gates are tuned to resonate the gate capacitances.

Because of its numerous advantages over single ended typology especially in integrated circuit (IC), a differential structure for class-E amplifier Fig. 2 is adopted as shown in Fig. 3. Balun is used here to convert the differential output voltage to a single ended voltage. However in the cases of differential antenna systems, there will be no need for the balun as the differential output voltage will be connected directly to the antenna through the matching networks. Among the important advantages of the differential architecture is its immunity to common-mode noise where substrate coupling is one of the main noise sources in IC. Moreover, it reduces the even harmonics generated by the switch non-linearity. As a result, this configuration is expected to achieve high linearity performance. Another merit, differential configuration gives double output power compared with the single-ended configuration yet at lower drain voltage swing.

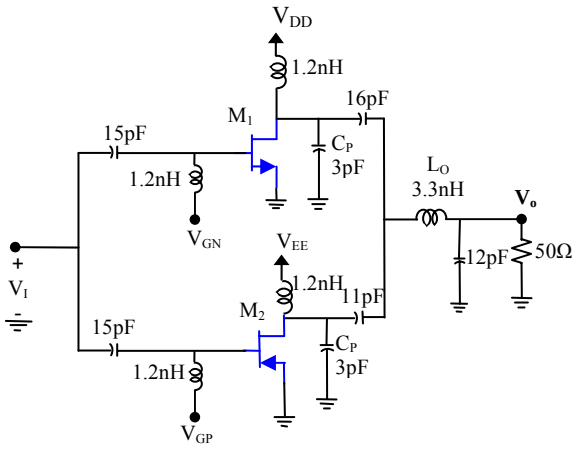

Fig. 2 Proposed Class-E Amplifier

4 Simulation

The proposed class-E circuit, Fig. 3, was simulated to study its performances. BSIM3 model were used to model the performance of the MOS transistors with HP 0.5-*u*m process model parameters, which are available in MOSIS' homepage. Fig. 4 shows the output power and drain efficiency versus frequency; about one watt output power and 80% drain

efficiency over wide range of frequency is achieved. Two-tone test is used to study the linearity of this circuit. Fig. 5 presents the third and fifth order intermodulation distortion (IMD) versus the two-tone frequencies spacing. The linearity of different class-E circuits was tested to compare their performance with other proposed circuits. Table 1 depicts that the proposed amplifier has the best linearity and comparable performance in terms of output power and efficiency. The 3rd and 5th IMD of the proposed PA are improved by 18 dB and 13 dB respectively compared to the conventional class-E.

ADS software (Advanced Design System) by Hewlett Packard is used to study the GSM response of the proposed PA. The maximum output power is normalized to compare the performance to the spectrum characteristics mask. The date rate is 270.83 Kbps, and the Gaussian filter bandwidth bit, BT, is 0.3. As shown in Fig. 6, no spectral regrowth is observed.

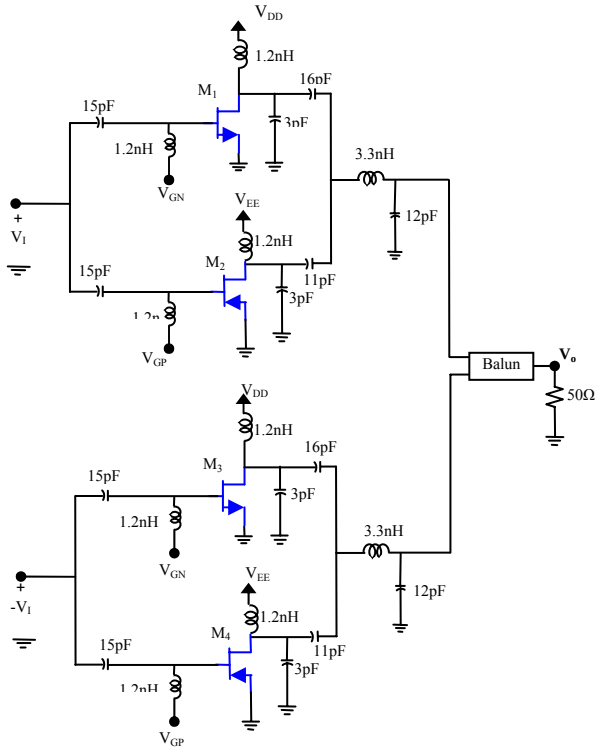

Fig. 3 Proposed Differential Class-E Amplifier

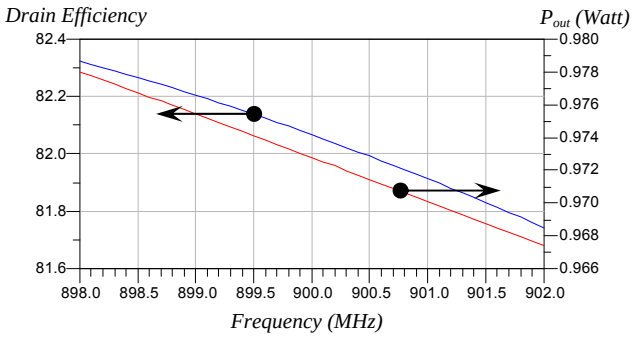

Fig. 4 Drain Efficiency and Output Power versus frequency

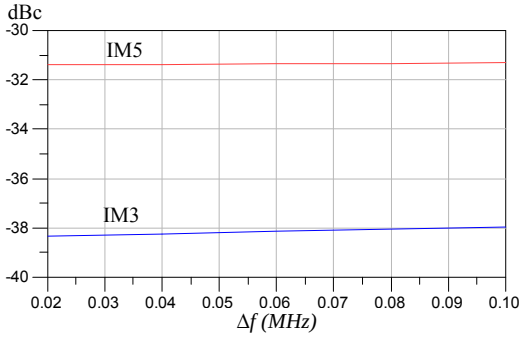

Fig. 5 Third and fifth IMD signals versus frequency spacing.

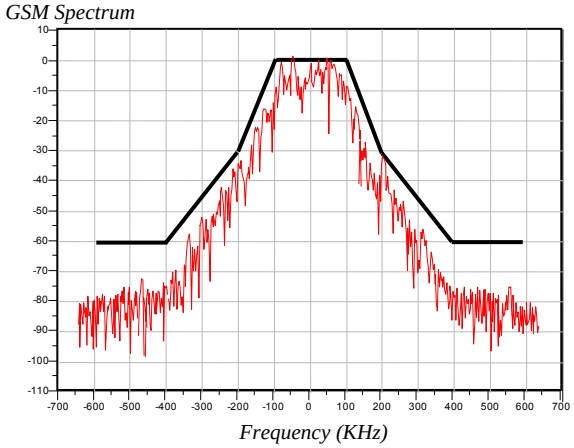

Fig. 6 GSM Spectral Emission for the proposed PA

Table 1: Performance of different class-E configurations at 900 MHz.

	Single-Tone Test		Double-Tons test	
	PAE	Pout Watt	IM3 dBc	IM5 dBc
Conventional class-E	76%	1	-13	-25
Class-E in [12]	75%	1	-21	-30
Class-E [13]	75%	1	-21	-32
Proposed Class-E	81%	1	-38	-32

5 Conclusion

A one Watt 900 MHz Differential CMOS class-E power amplifier with 80% drain efficiency has been designed using a standard digital 0.5-*u*m CMOS process. It is shown that 3rd and 5th IMD products of the proposed PA are lower than that of the conventional class-E amplifier by 18 dB and 13dB respectively.

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