Electronic phase sensitive receiver for railway signalling technology

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Abstract: This article deals with a design of a replacement of an electro mechanic phase sensitive relay type DSS-12. These relays are used by the Czech Railways for detecting the presence of railway vehicles at the rail circuit. The replacement of electro-mechanical phase sensitive relay leads to the design of a special digital signal processing (DSP) system. The input signals must be converted from an analogue signal to a digital representation by A/D converters and further processed by digital signal processing methods. Discrete Fourier transform, an iterative algorithm CORDIC and threshold was used for digital signal processing. The digital signal processing system was implemented in C language and then rewritten to the VHDL language to implement it in the FPGA (Field Programmable Gate Array) device.

Key-Words: phase sensitive relay, DSS-12, railway signalling technology, rail circuit

1 Introduction

At present time electro-mechanic relays are used as a railway signalling technology by the Czech Railways. These relays were developed in the 1960 and are used for detecting the presence of railway vehicles at the rail circuit.

2 Railway circuit

The railway circuit is shown in Figure 1. It consists of an isolated rail segment, a transformer, a source of signal with given frequency and a phase sensitive relay.

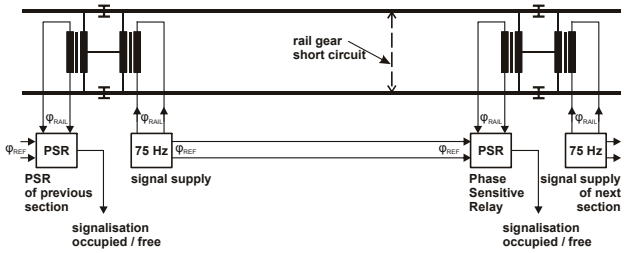

Fig. 1 Railway circuit

The railway circuit is modeled by an electrical circuit with RLC parameters spread along a rail. Thus when the moving rail gear makes a short circuit between rails then both amplitude and phase of the rail signal will change in time.

The source generates the sinusoidal signal with frequency 75 Hz or 275 Hz. The source of the signal has two outputs phase shifted by 90 degrees. One of them is connected to the transformer's primary winding. The secondary winding of the transformer is connected to the rail circuit. The second output is connected to the reference input of the phase sensitive relay. At the opposite end of the railway circuit is signal from the second transformer connected to the second input of the phase sensitive relay. The presence of the railway vehicle in the railway segment can be detected by changes in the amplitude and phase of the rail signal against the reference signal. The change of both the amplitude and phase is detected by the relay.

2.1 Phase sensitive relay DSS-12

The phase sensitive relay DSS-12 is shown in Figure 2. The functionality principle of the relay is well known as Ferraris motor.

Fig. 2 Phase sensitive relay DSS-12

The phase sensitive relay consists of two coils turned over 90 degrees. An aluminum plate is inserted between them and by a torque M acts on contacts. The torque M is proportional to the product of coils current magnitudes

in and function *sin φ* (Equation 1). Where the *φ* is phase angle between currents I_1 and I_2.

(1) $M = k\, I_1\, I_2 \sin\varphi$

The maximum moment happens when the phase angle *φ* is equal to 90°. The output of the relay depends on deviation of the plate.

Because these relays are present at the each segment of the railway (length 100 m to 1.5 km) and they have an expensive maintenance a new design of their electronic version is being developed.

3 Digital signal processing algorithm

The digital signal processing algorithm was suggested. The algorithm does computation analogous to the phase sensitive electro-mechanical relay DSS-12 (follow the Equation 1) and was designed with respect to easy implementation in the FPGA (Field Programmable Gate Array) device. At the beginning the signals (railway and reference) are converted from the analogue signal to digital representation by A/D converters.

3.1 Computation of amplitude and phase

The amplitude and phase of the digitalized signal can be computed by discrete Fourier transform (DFT) [1, 2].

(2) $$X_k = \sum_{i=0}^{N-1} x_i e^{-j(2\pi/N)ik} = \sum_{i=0}^{N-1} x_i W_N^{ik}, \quad k = 0,1,\ldots, N-1$$

As the result of the one point DFT computation at frequency 75 Hz or 275 Hz for the railway and reference digitalized signals, we get two complex vectors. For each complex vector we can compute its amplitude and phase by

(3) $$A = |X_k| = \sqrt{x_{k\,re}{}^2 + x_{k\,im}{}^2}, \quad \varphi = \arctan\left(\frac{x_{k\,im}}{x_{k\,re}}\right)$$

The direct realization of square root and arctan functions in the FPGA device is fairly complex and inefficient. The computation of the amplitude and phase of a given complex vector can be done by an iterative algorithm, e.g. CORDIC (COrdinate Rotation DIgital Computer) algorithm [3, 4]. The principle of the algorithm is a vector rotation in a plane by the series of micro rotations. The one micro rotation is defined as:

(4) $$\begin{aligned} x[j+1] &= x[j] - \sigma_j 2^{-j} y[j] \\ y[j+1] &= x[j] + \sigma_j 2^{-j} y[j] \\ z[j+1] &= z[j] - \sigma_j \tan^{-1}\left(2^{-j}\right), \quad \text{where } \sigma_j \in \{-1,1\}. \end{aligned}$$

Only three additions / subtractions, two shift operations and one pre-computed table with angles are required for the implementation of one micro rotation.

We assign to *x* real part and to *y* imaginary part of the vector. The computation of the amplitude and phase of the vector in Equation 4 is done with this assignment. We obtain an accumulated angle (initial value is 0) after several micro rotations in *z*. The CORDIC algorithm multiplies the vector amplitude by a factor $K \approx 1.64676$.

3.2 Computation of torque *M*

We need to compute trigonometric function *sin* of the phase angle *φ* (phase difference of the vectors) to get the value of the torque *M*. The computation also can be done through the CORDIC algorithm. We assign $x = 1$, $y = 0$ and $z = \varphi$ at the beginning of the computation. The results are ready after several micro rotations. The result of the function *cos φ* is stored in *x*. The result of the function *sin φ* is stored in *y*. Now we have computed out all variables (I_1, I_2 and *sin φ*) and we can compute the torque *M* by the multiplication of them. The hardware multipliers which are commonly available in today's FPGA devices are used for the multiplication.

The computed torque *M* has to be compared to the preset thresholds. The two threshold values define the hysteresis. The hysteresis is necessary to avoid an oscillation of the output. The output of the comparator is logical signal which indicates whether the railway segment is free or occupied by a railway vehicle.

3.3 Delayed output

The electro-mechanic phase sensitive relay has some reaction time (pull time and drop time). The output signal timing must be realized even in the DSP algorithm. The programmable pull time and drop time were realized by a simple circuit.

The output of the threshold logic controls two counters – "False" counter and "True" counter. The "False" counter counts up when the output of the threshold logic is logical 0, and counts down when the output of the threshold logic is logical 1. The "True" counter counts vice versa. Each counter counts to the specified value and do not overflow or underflow. The output of the relay is logical 0 when the "False" counter reaches a specified value and logical 1 when the "True" counter reaches the specified value. The specified values are adjusted to pull and drop time of the real relay.

3.4 Verification of DSP algorithm

A model of the electronic phase sensitive relay [5] was built to verify the suggested digital signal processing algorithm. The model consists of the analogue-digital hardware module and the software that runs on a PC.

The analogue part of the module contains the over-voltage protection, an operational amplifiers network for

the adjustment of the input voltage range, successive approximation 16-bit A/D converters with serial output, 2.5 V voltage reference and 10 Mbps optocouplers for the galvanic isolation between the analogue and the digital part of the circuitry. The digital part of the module consists of a FPGA device only. It samples analogue signals and transfers the digitized samples to a PC. The analogue-digital module allows simultaneous sampling of two analogue channels at a sample rate of up to 100 kHz with a 16-bit resolution.

The software part was written into C language. It supports three simulation input data modes. First two modes do offline simulation with an interactively generated data or with a data stored in binary files. The third mode supports real-time simulation with the data acquisition from the hardware module (real data).

3.5 Implementation in the FPGA device

The whole system was rewritten into VHDL language after the successful verification of the DSP algorithm on the PC. The system consists of several modules. Block diagram of the realized system in the FPGA device is shown in Figure 3.

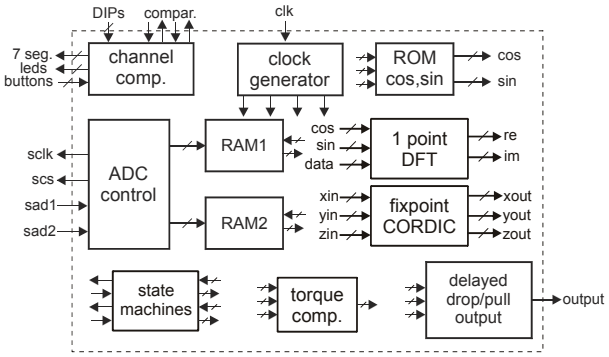

Fig. 3 Block diagram

The clock generator generates sample clock and master clock for serial A/D converters and clocks for finite state machines. The ADC control module controls a data acquisition by serial A/D converters. The next block is ROM with sin and cos coefficients for the computation of one point DFT. The Kaiser window with $\beta = 2$ was applied to the coefficients in order to suppress the influence of the buffers boundaries. The samples produced by ADC block are shifted to the sample buffers. A one point DFT is then computed over each buffer. The frequency resolution of the realized DFT is 5 Hz per point. The complex vectors are obtained for each buffer. The amplitude and phase of the vectors is then computed by the iterative CORDIC algorithm. After the rectangular to polar conversion, the algorithm continues to compute function sin of the phase difference again by the CORDIC algorithm. Finally the torque is computed by two multiplications, the threshold function is performed and delayed drop/pull output function is realized. All mentioned blocks are controlled by finite state machines.

Because the whole system must be safe, the reciprocal comparison (block channel comp. in Figure 3) was designed. The system consists of two identical channels. The results of their computations are compared. The amplitudes, the phases, the torque, the final outputs and the several internal states are compared.

The system was written in the VHDL language and successfully simulated in simulator by functional and finally by timing simulation. The simulated input data for serial A/D converters was read from binary files stored on disk.

4 Conclusion

The main goal of the design was to create and verify digital signal processing algorithm and its implementation to the VHDL language. This goal was satisfied and fully functional model was successfully finished. The system is realized in the FPGA device Altera EP2C8 and contains over 2000 LUTs (Look-Up Tables), 600 flip-flops and 6 kB of RAM memory. The computational power of the realized system is 22 MOPS. This type of a digital system implementation is called "System On Programmable Chip" (SOPC). Due to use of the digital signal processing, the electronic version of the relay has advantages. For example in the field of diagnostics of the railway circuit it can monitor the amplitude and phase of the free and occupied railway segment and store these values for diagnostics purposes.

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References:

[1] A. V. Oppenheim, R. W. Schafer, J. R. Buck, Discrete-Time Signal Processing, Prentice-Hall Inc., Upper Saddle River, New Jersey, USA, 1999, p. 870. ISBN 0-13-083443-2

[2] V. Cizek, Discrete Fourier transforms and their applications, Adam Hilger, Bristol, UK, 1986, p. 141. ISBN 0-85274-800-0

[3] J. E. Volder, The CORDIC Trigonometric Computing Technique, IRE Transactions on Electronic Computing, vol. EC-8, 1959, pp. 330-334

[4] M. D. Ercegovac, T. Lang, Digital Arithmetic, Morgan Kaufmann Publishers, San Francisco, USA, 2004, p. 709. ISBN 1-55860-798-6

[5] M. Poupa, Electronic Replacement of Electro-Mechanic Phase Sensitive Relay, Proceedings of the "IEEE International Conference on Computational Cybernetics ICCC 2003", Siofok, Hungary, 2003, pp. 385-387. ISBN 963-7154-17-5