Tolerance Analysis in MOSFET Analog Integrated Circuits

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Abstract: - The goal of the design and optimization phase in analog integrated circuits conception is to get the structure yielding the best system performance. The parameters of various components (resistance, capacitance, transistors, etc) of the circuit are set to the optimized nominal values, but no guarantee exists that these values will be conserved during the fabrication process. As a matter of fact, during fabrication the real values of the circuit parameters deviate from the nominal values and consequently the performance of each sample is affected in an unpredictable way. Manufacturers sometimes propose the upper and lower bonds of the acceptability interval, but generally they are obtained after performing measurement of an important number of samples. Furthermore, any circuit whose performance is outside the pre-established interval of acceptability is definitively rejected. When a tolerance analysis is included in the design process, the designer has the possibility to estimate, according to the tolerances imposed on each component, the maximum possible fluctuations of the performance before manufacturing the circuit. The first- and second-order sensitivities of the performance with respect to all circuit parameters must be previously computed. In MOS integrated circuits the designer has no direct access to electrical parameters, thus the tolerance analysis with respect to these parameters is insufficient. Our work consists in developing a procedure to compute the sensitivities of the performance of interest with respect to the geometrical parameters of MOSFETs, which are the only parameters under designer's control. A software package has been developed to link these sensitivities to those with respect to the electrical parameters, as in any traditional approach. From these results, and using the tolerances provided by the manufacturer on the geometrical and technological parameters of the MOSFETs, we can accede to the lower- and upper-bonds of performance fluctuations around its nominal value.

Key-Words: - Tolerances, Analog Integrated Circuits, Sensitivity, Modeling, MOSFET

1 Introduction

The goal of design and optimization process is to get the values of the circuit parameters, which yield the best performance. With the continuous scaling down of circuits, accurate control of every step of the fabrication process becomes more and more difficult and this results in non negligible difference between the computed and the fabricated values of the components parameters. As a result, the performance of the circuit is affected in an unpredictable way.

Furthermore, traditionally the optimization process is carried out on the electrical parameters (like resistance, capacitance, etc.). The link between the electrical parameters and the technological or geometrical parameters is missing, even if sometimes it is more or less intuitive. Rather than to perform a tolerance analysis with respect to electrical parameters, it is undoubtedly more interesting to perform this analysis with respect to the geometrical and technological parameters of the MOS transistors, which are under designer's control. In this way, the designer can estimate, before manufacturing, the maximum deviations of the performance of interest around its nominal value. This is expected to improve the fabrication yield.

This paper presents a novel method to compute the maximum and the minimum of a MOSFET analog circuit performance, with respect to the imposed tolerances of the geometrical parameters. This method uses first- and second- order sensitivities of the target performance with respect to all geometrical dimensions of the MOS components.

2 Sensitivities

Sensitivities computation is a decisive step in analog circuit design. Inspecting their values, we are able to establish a list of the most sensitive parameters i.e. those parameters whose deviations have the greatest impact on the target performance [1].
There are different types of sensitivities of a performance F, with respect to two circuit parameters denoted h_i and h_j:
- single first-order relative sensitivity :

$$S^{1}_{h_i} = \frac{h_i}{F} \cdot \frac{\partial F}{\partial h_i} \quad (1)$$

- single second-order relative sensitivity :

$$S^2_{h_i} = \frac{1}{2}.\frac{h_i^{\,2}}{F}.\frac{\partial^2 F}{\partial h_i^{\,2}} \quad (2)$$

- cross second-order relative sensitivity :

$$S^2_{h_i h_j} = \frac{h_i.h_j}{F}.\frac{\partial^2 F}{\partial h_i.\partial h_j} \quad (3)$$

The computation of second- and higher-order sensitivities is necessary because often the values of the first-order sensitivities are not enough to predict how strong is the impact of any of the circuit parameters. [1]

If the sensitivities values are available, by means of a truncated Taylor series development we can find a very close polynomial approximation of the performance F, versus the relative variations of the n parameters (denoted h_i or h_j) :

$$\frac{\Delta F}{F} = \sum_{i=1}^{n} S^1_{h_i}.\frac{\Delta h_i}{h_i} + \sum_{i=1}^{n} S^2_{h_i}.\left(\frac{\Delta h_i}{h_i}\right)^2 + \sum_{i=1}^{n} \frac{\Delta h_i}{h_i}.\left(\sum_{j=1}^{n} S^2_{h_i h_j}.\frac{\Delta h_j}{h_j}\right) \quad (4)$$

The values of the sensitivities with respect to electrical parameters are obtained by using a home-made software package called SAMI, intended to analog and microwave linear circuits sensitivity analysis [2].

3 The MOSFET parameters

The MOSFET, like any active linear component, has been implemented in SAMI and described by means of its small signal equivalent model. The NMOS structure is presented in Fig.1 (the PMOS structure being the complementary structure, with a P channel). The transistor is characterized by its dimensions (the length *L* and the width *W* of the gate, the overlap length L_d), and its technological parameters (the oxide capacitance C_{ox}, and the mobility of charge carriers in the channel denoted μ_n).

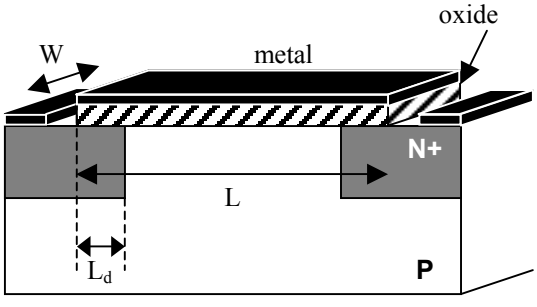

Fig. 1 3-D view of the NMOS structure

The simplified equivalent circuit of the MOSFET is presented in Fig.2. The influence of the bulk has been neglected and the threshold voltage V_T is considered constant.

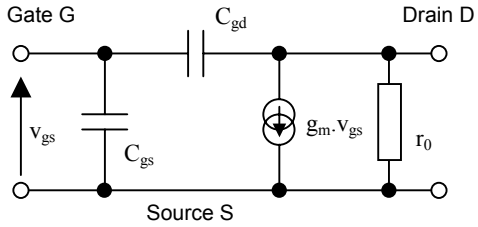

Fig. 2 The MOSFET small-signal equivalent circuit

SAMI can compute sensitivities with respect to the internal electrical parameters of the MOS components (capacitances C_{gs} and C_{gd}, output conductance r_0, and transconductance g_m). An additional module has been added, which provides the sensitivities with respect to the geometrical and technological parameters of the MOSFET (width *W*, channel length *L*, the overlap gate length L_d, and the oxide capacitance C_{ox}).

4 Tolerance Analysis

Let us consider an analog circuit.

- The target performance is noted F.
- Each of its n parameters, h_i, has a nominal value denoted by h_{i0}, and an actual value, resulting after manufacturing, $h_i = h_{i0} + \Delta h_i$.
- $F_0 = F(h_{10},h_{20}, ...,h_{n0})$ is the nominal value of the performance, and $F(h_1,h_2, ..,h_n) = F_0+\Delta F$ is its effective value.

The goal of tolerance analysis is to establish the upper- and lower-bond of F, denoted respectively by F_{max} and F_{min}.

The analysis starts with the computation of the first- and second-order sensitivities of F with respect to all the parameters h_i. These results are employed in the next step that is the tolerance analysis itself. The core of tolerance analysis is an optimization procedure, based on the gradient method.

However, the number of iterations may become important if the number of the parameters is high. That's why before using this method we have introduced a step to find the monotonic parameters (i.e., those whose variation in a monotonic way produces a monotonic variation of the performance). The optimization is run only on the set of non-monotonic parameters and

consequently the computation time is significantly shortened [3].

5 Results

Consider the elementary amplification cell shown in Fig.3; consisting of a NMOS common-source amplifier biased by a PMOS transistor that in turn has its gate maintained at a potential V_{BIAS} of 3.85V, and a W_P size of 30µm. Input potential V_s has a DC bias value of 1.05V. This circuit has an estimated magnitude of its voltage gain $\frac{V_{out}}{V_s}$ of 347.3 [4].

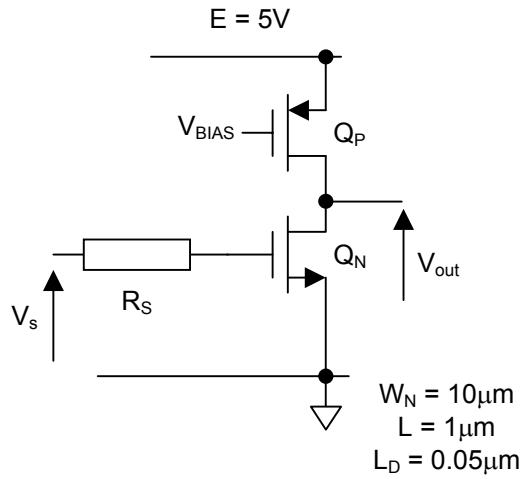

Fig. 3 Common-source amplifier

In Figure 4 are shown the first-order relative sensitivities with respect to the electrical parameters (C_{gs}, C_{gd}, r_0, and g_m) of both MOSFETs.

Figure 5 presents the first-order relative sensitivities with respect to the geometrical and technological parameters (L, W, L_d and C_{ox}) of each MOSFET (index N is for Q_N and index P is for Q_P).

Using both 1st and 2nd order sensitivities, a tolerance analysis has been performed. Considering ±5% tolerances of L, W, L_d and C_{ox} we have established that :

- the minimum value of the gain magnitude is **337.67**
- the maximum value of the gain magnitude is **356.33**

Therefore, any sample of this amplifier exhibits a gain whose value is comprised between -2.8% and +2.6% with respect to its nominal value.

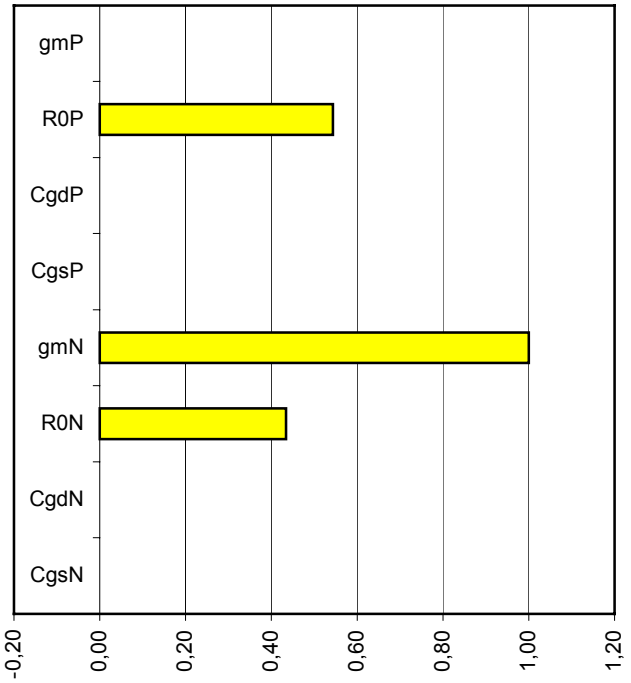

Figure 4 First-order sensitivities with respect to electrical parameters

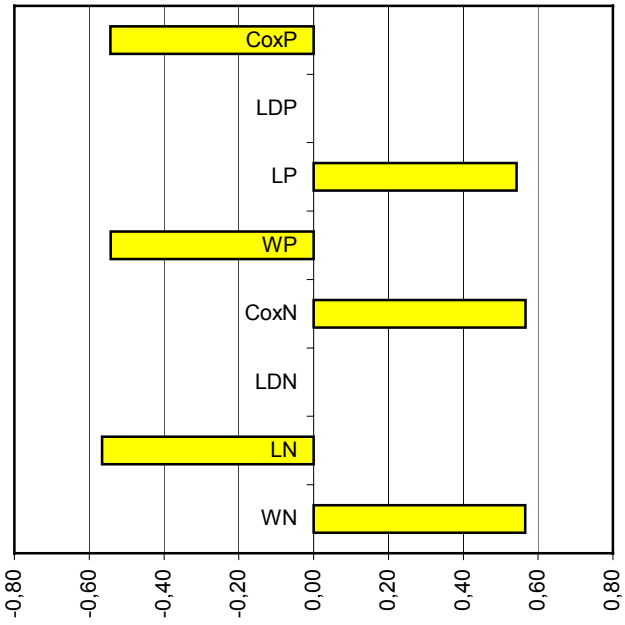

Figure 5 First-order sensitivities with respect to geometrical and technological parameters

We note that with actual technologies the influence of the overlap dimensions L_d is negligible but, as the geometry of the transistors shrinks, in the future this parameter may play a more important role.

6 Conclusion

An exact estimation of the maximum variations of the performance of interest in a MOS analog integrated circuit with respect to the transistor size variations is now available. Using this tool, the designer is able to predict if the circuit is enough robust with respect to inherent deviations affecting the MOSFETs geometrical parameters.

Since the tolerance analysis with a simple model is efficient, in the next future we hope to be able to improve the MOSFET model by considering the influence of the substrate on the threshold voltage.

Finally, it is highly desirable to extend tolerance analysis to MOS digital integrated circuits, especially to detect the influence of the geometrical parameters on the delay time.

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