Threshold Gate with Hysteresis using Neuron MOS

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Abstract: In this article threshold gates with hysteresis using neuron MOS (νMOS) are presented as basic elements in Null Convention Logic (NCL) circuits. NCL, which proposed by K. M. Fant and S. A. Branst, needs special gates having hysteresis, because NCL uses different ternary logic systems in computation phase and wiping phase of asynchronous behavior, respectively. To impliment the dinamic behavior, The traditional NCL circuits exploit extended CMOS structure which consists of a number of cascaded and parallel transistors connections. Then we improve the circuti with the characteristics of threshold function in νMOS, we designed hysteresial νMOS by means of feedback loop. This results the asynchronous circuits reducing the number of MOS and wire area. We provide two synthesis methods and simulation results of the gates and full-adder. The evaluation results of area dissipation and average delay show the advantages of the proposed circuitry.

Key–Words: Asynchronous Circuit, Delay Insensitive, Neuron MOS, Threshold Gate

1 Introduction

High-speed and high-performance synchronous circuit design in VLSI suffer some serious problems such as clock skew, clock noise and larger power dissipation. Asynchronous circuits solves such problems by use of request/acknowledge signaling instead of global clock direction. In the asynchronous circuit design, there are two main design categories based on. They are called *bounded-delay model* and *self-timed model* which came from different assumption of delays[1].

In this article, quasi-delay-insensitive model (QDI), which is one of the self-timed model, is assumed[2][3][4]. The QDI model is currently most practical assumption to construct asynchronous circuit systems, that is, delays in both gate-elements and wires are unbounded, and additionally signals propagating through forked wire are arrive simultaneously to different destinations. On the other hand, Null Convention Logic (NCL) [1][5] is a technique for design of asynchronous circuits and satisfies QDI assumption. While QDI oriented circuits are unaffected by changing of delays, it requires over head circuitry.

We present threshold gate with hysteresis using νMOS as components of NCL circuit. Exploiting the νMOS can reduce numbers of MOS transistors, thus it will save total area enough to develop speed of circuits.

2 Two Phase System and NCL

2.1 Two Phase Data Transfer

Asynchronous circuit usually adopts dual-rail logic circuit to satisfy QDI assumption. NCL also assumes QDI and dual-rail structure. The behavior of dual-railed asynchronous circuits is called two phase data transfer for detecting data arrival. That is to say, initial state of circuit takes invalid data value (0 0) at inputs and output of element. This state is achieved wiping phase preceding computation phase. Thus dual-rail, refer table 1, can transfer valid data and completion timing at a time. On the other hand, althogh this class of asynchronous circuits are usually based on weak Kleene logic (B-ternary logic)[6], NCL exploits strong Kleene (C type logic)[7] in computation phase and weak Kleene in wiping phase. To achieve this interesting system behavior, circuit requires hysteresis gates to justify front of wave of computations[5].

Table 1: Dual-rail ternary data expression

D_1	D_0	contents
0	0	invalid (NULL)
0	1	valid data 0
1	0	valid data 1

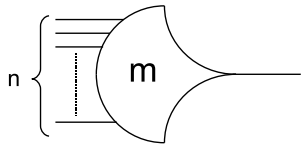

Figure 1: Symbol of TH gate

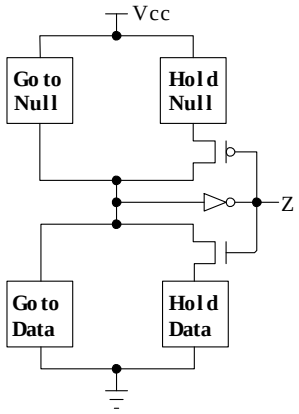

Figure 2: Block type TH gate

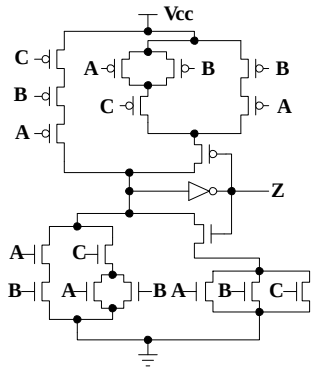

Figure 3: Block type TH23

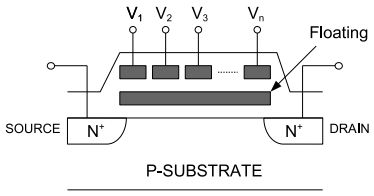

Figure 4: Structure of νMOS

2.2 Threshold gate with hysteresis

Threshold gate with hysteresis (TH gate) is used in order to synthesize of NCL circuits[8]. Fig.1 is a symbol of TH gate. TH gate has two parameters, one is the number of inputs and the other is a threshold value. A histerisial threshold gate which has n-inputs and threshold m is described as $THmn$ hence force. Note that the threshold m means that the gate output is activated to ON when m inputs or more are activated. Afterward output retains ON while all of input deactivated to OFF. In other words, TH gate is a spacial gate such as threshold of activating and deactivating are different. Note that a $THmn$ has activating threshold m and deactivating threshold 1, thus the output has hysteresis.

Fig.2 shows a TH gate synthesis using MOS transistors. It is called *block type* TH gate because it has four MOS network blocks. For instance, Fig.3 is a block type $TH23$ gate where A,B,C are three inputs of $TH23$. Block type requires a number of MOS transistors.

3 Design of TH gate using νMOS

3.1 Basis of νMOS

νMOS (neuron MOS) is one of the floating gate which has some inputs and an output. Fig.4 is the structure of νMOS and fig.5 is the equivalent circuit. The behavior of νMOS is as follows. Suppose V_0=0 as in fig.5 and the V_F in the floating gate is stated as follows.

$$V_F = \frac{\sum_{i=1}^{n} C_i V_i}{\sum_{i=0}^{n} C_i} \tag{1}$$

That is, V_F increases depending on the number of asserted inputs m'. When threshold voltage is V_{th} and $C = C_1 = C_2 = \cdots = C_n$, the ON condition of νMOS is stated as follows.

$$V_F = m' \cdot \frac{C}{nC + C_0} V_d > v_{th} \tag{2}$$

where C_0 is the capacitive coupling coefficient between the floating gate and the substrate. Therefore, when the number of activated inputs m' exceeeds threshold m, the νMOS activate to ON.

Fig.6 is a νMOS threshold gate having three inputs. And Fig.7 is a wave form of V_{OUT} and V_F in Fig.6. The wave form shows the output of the gate is activated when two or more inputs are activated.

In the following we propose two kinds of techniques to implement TH gates. The one is a technique exploiting νMOS at the four blocks in Fig.2, and the other is νMOS with feedback to synthesize TH gates. Both techniques reduce the number of MOS transistors then higher speed operation can be expected.

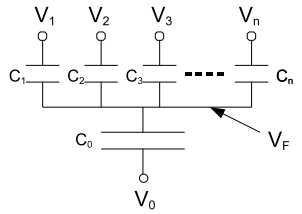

Figure 5: Eqivalent circuit

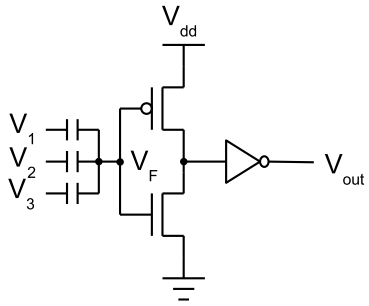

Figure 6: Three inputs threshold νMOS gate

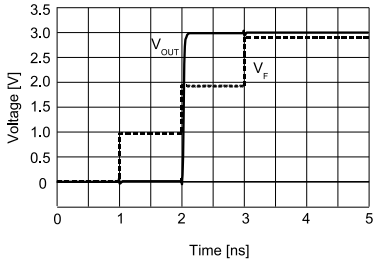

Figure 7: Characteristic wave form of νMOS

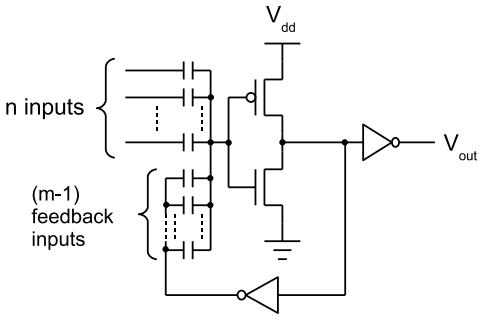

Figure 8: νMOS THmn gate

3.2 νMOS TH gate

The proposed TH gate (hysterisial threshold gate) with feedbacked νMOS is shown in Fig.8. In case of $THmn$, the number of feedback inputs $\mid I_f \mid$ is

$$\mid I_f \mid = (m-1). \tag{3}$$

And the number of unit capacitance $\mid C_u \mid$ is

$$\mid C_u \mid = n + (m-1). \tag{4}$$

Thus initially an $n+m-1$ inputs νMOS has to be prepared to fabricate $THmn$.

Instead of the above, a feedback with capacitance;

$$C_f = (m-1) \cdot C_u \tag{5}$$

in a νMOS can implement the same THmn gate.

Let's consider the case $\mid C_u \mid = n + (m-1)$ for simplicity. In Fig.8, when activated inputs are m or more, the output V_{out} goes up HIGH (ON), and the feedback input also activated to ON. In the sequel, V_F goes up by bias voltage $(m-1) \cdot C_u$. Then until all the activated inputs goes down to LOW, V_{out} retains ON because the V_F stays $m \cdot C_u$ or more.

Fig.9 indicates $TH23$ with νMOS. The $TH23$ SPICE simulation is shown in Fig.10. The result shows when two or more inputs are activated to HIGH, the output goes to HIGH and a feedback input is also activated. Then floating gate voltage V_F is biased by C_u and the output remains HIGH until all input goes down to LOW.

3.3 Block type TH gate with νMOS

The second technique is block type TH gate with νMOS (Fig.11). Block type TH gate has four MOS network blocks. Each block can be defined simple threshold function. Define threshold function $Th(x)$ as;

$$Th(x) = \begin{cases} ON & m' \geq x \\ OFF & otherwise \end{cases} \tag{6}$$

where m' is the number of activated inputs. Then the four blocks in Fig.2 can be synthesized with $Th(x)$. The activating conditions of each block is stated as follows;

GOTO NULL : $Th(m)$
GOTO DATA : $Th(m)$
HOLD NULL : $Th(1)$
HOLD DATA : $Th(1)$

Therefore, each block can be synthesized only one νMOS.

Fig.12 is the block type $TH23$ with four νMOS's. Clearly Fig.12 is simpler construction than traditional block type $TH23$ in Fig.3. Especially, delay of block type TH gate is depend on GOTO NULL block, then the delay is reduced because GOTO NULL block in Fig.11 has only one transistor. Note that connecting PMOS transistors makes longer delay.

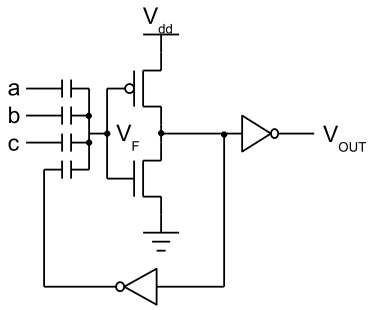

Figure 9: νMOS TH23

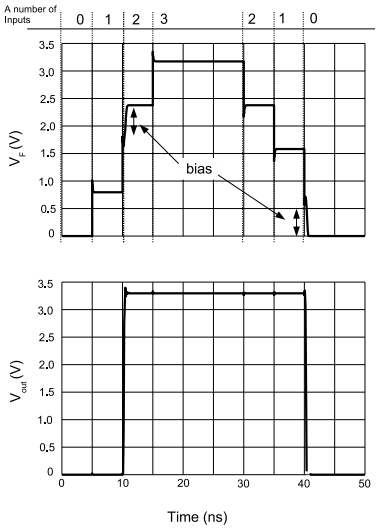

Figure 10: wave of V_F-V_{OUT}

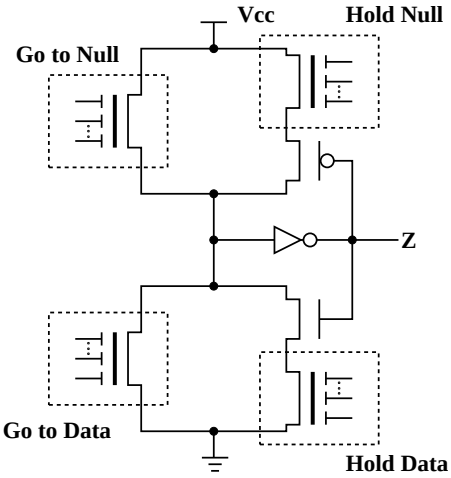

Figure 11: Block type TH gate with νMOS

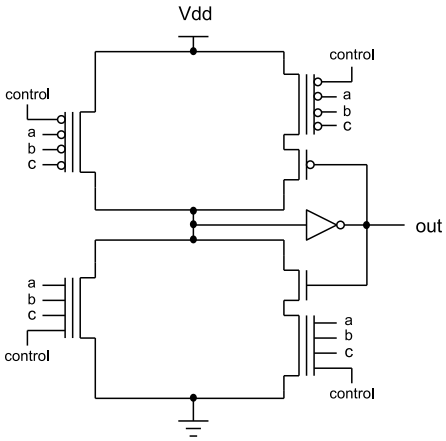

Figure 12: Block type TH23 with νMOS

4 Evaluation

We designed $THmn$ gates made from νMOS with feedback and from block type νMOS. Some comparison with the number of MOS transistors and delay will be shown here. We prepared MOS FET SPICE model provided by MOSIS[10] for simulations. The process rule is 0.35[μ m] and supplying voltage is 3.3[V].

Table.2 shows the comparison of the number of MOS FETs. Clearly, in table2, the number of MOS transistors of the proposed circuits are constant irrespective of the number of inputs and the value of threshold. On the other hand, traditional the block type circuits increase the number of transistors in accordance with n and m. Therefore proposed circuit technique is adequate for asynchronous systems.

Table.3 shows that the proposed circuits yields fewer delay than traditional block type circuits. The delay of traditional circuits depends on the number of PMOS in GOTO NULL block. Although νMOS block type is similar structure to the traditional one, it has only one PMOS in GOTO NULL block. Hence the delay of $THmn$ with blocked νMOS does not depend on the number of inputs or the value of threshold as shown in table.3.

Finally, a design of asynchronous full adder consists of $THmn$ gate is shown in Fig.13. Note that the symbols, shaped a ginkgo leaf, indicates a THmn gate where a numeral on a symbol is a threshold value of the gate. The computational wave form is also shown in Fig.14. This simulation provides favorable operations.

5 Conclusion

In this paper, we proposed two novel circuits exploiting νMOS to hysterisial threshold gates, which is one of the floating gate, for asynchronous systems. Two types νMOS TH gates are presented and they are com-

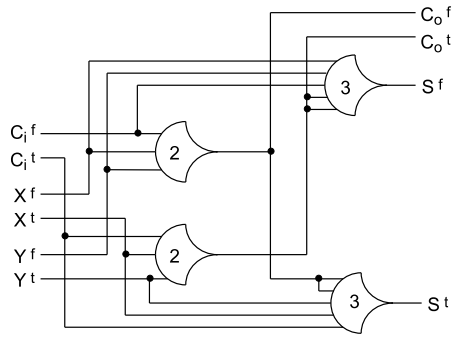

Figure 13: Full Adder based on νMOS THmn Gates

pared with traditional constructed NCL TH gates. As a result, we showed νMOS TH gates are smaller and faster than traditional one. And the number of MOS FETs and average delay time are efficiently reduced to 62% and 48% compared with traditional one, respectively. As a future work, we will try to design larger circuits like a multiplier with the proposed gates.

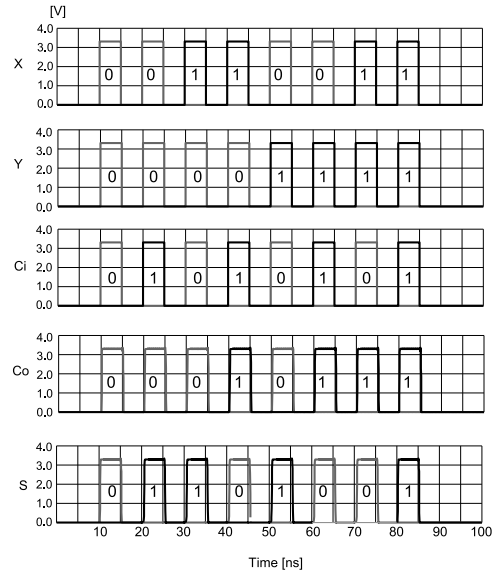

Figure 14: Full Computational Wave Forms of Full Adder

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Table 2: The number of MOS Transistors

	Traditional	THmn with C-νMOS	Blocked THmn with νMOS
$TH22$	12	6	8
$TH23$	18	6	8
$TH24$	18	6	8
$TH33$	16	6	8
$TH44$	20	6	8
Full Adder	80	24	31

Table 3: Avarage delay of THgate [psec]

	Traditional	THmn with C-νMOS	Blocked THmn with νMOS
$TH22$	280	160	266
$TH23$	450	260	271
$TH24$	890	416	390
$TH33$	400	197	348
$TH44$	535	220	423
Full Adder	1041	499	646

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