Optimizing Selective Decoupling Capacitors by Genetic Algorithm for Multiplayer Power Bus

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Abstract: - How to effectively use the decoupling capacitors to mitigate power/ground noise on high-speed power delivery systems is investigated in this paper. The objective is to determine the minimum number of added decoupling capacitors and their position on the printed circuit boards (PCB). The genetic algorithm (GA) is employed to implement optimizing the accurate choice of the decoupling capacitors and quantities for a pre-defined power/ground noise specification. This can improve design efficiency to reduce the empirical or try-and-error design cycle, and has the advantages of cost reduction and less PCB layout area. In an example of the PCB with dimension of 27 cm by 15 cm, the minimum number of capacitor is five with a specified target impedance of 1Ω and the most effective location of decoupling capacitor is nearby the input port. It can estimate correctly the least number of capacitor used.

Key-Words: - Decoupling capacitor, Genetic algorithm, Multilayer power bus, Power/Ground noise, Power delivery system, Printed circuit board.

1 Introduction

When the gigahertz of the computer microprocessor time comes, the traditional digital circuit design method becomes outdated. The phenomenon caused by high speed and high frequency seriously affects the quality of the circuit signals. Understanding the phenomenon caused by high-speed circuit is necessary for circuit designers. Signal integrity is an important word that is always heard in the high-speed design. All those topics related to signal quality can be counted as signal or power integrity. Reflection, crosstalk and ground bounce, etc are the concerned topics [1-3]. Ground bounce is being widely discussed in recent years, which we need to pay attention to especially in high-speed circuit. When the speed of the electronic products becomes faster, because of the fast switch of signals, the power supply needs to provide a large amount of current in a short time, and when the power system connects, there is inductance which will bring to a voltage decrease, thus will decrease the noise margin of the circuit and hence affect the normal work of the circuit. This is called power or ground bounce noise. The noise is also called simultaneous switching noise or delta I noise. When the CMOS process further improves the technology, the voltage becomes lower, from 5V in 1990 to 1.2V or 1V nowadays. Therefore, noise interference becomes very important. For example, when a device with 1ns rise time needs 30mA current, if this current passes through a 100nH connected inductance, it will lead to a 3V voltage drop temporarily. This voltage drop will possibly cause the circuit to function fail. As a result, how to lower the noise interference becomes more important and is also a challenge for the high-speed electronic products designers.

Generally, there are two ways to lower the simultaneous switching noise or delta I noise. One is using the decoupling capacitor [4-7], and the other is using power islands or power-plane segmentation [8]. Decoupling capacitor is to use large amount of capacitors to lower the impedance value of the power plane and hence to lower the noise. However, we have to pay attention to the series inductance of the decoupling capacitor and the amounts of inductance when it is connected, otherwise it doesn't work. Power island or power-plane segmentation is used to isolate the power of the faster circuit to avoid affects to other circuits, but how to isolate is an important point to discuss. Moreover, it comes to our attention that other signals integrity will be affected when signals cross over the borders of these isolated areas. This paper presented how to use genetic algorithm optimal determination the amount of decoupling capacitors. Although there are many discussions on this topic in the reference, it is lacking of an effective way to estimate the numbers of capacitor have to be used. Many still use experience to make a decision.

This paper will use genetic algorithm optimal the number of decoupling capacitors used and provide a simple design procedure for the designers of high-speed circuit power system as a reference.

2 Power/Ground Impedance Simulation Method

Following the increase of the circuit frequency, the design of the power distribution system of the printed boards becomes a key issue in high-speed boards. In the old days, because the operation frequency of the electronic circuit is not high, thus the connected inductance can be neglected and noise does not need to be taken into considerations. Gradually because the operation frequency increase, power connected inductance have to be considered. Increasing use of bulk capacitor is a necessary to reduce the noise; otherwise the circuit will be sensitive to noise. Due to the addition of bulk capacitors, the operation frequency can be improved into a few MHz. However, following the increase in frequency, the amount of inductance of the printed circuit board layout cannot be neglected, so the adding of the decoupling capacitors will enable to reduce the power noise efficiently. Since the decoupling capacitors have the effective series inductance which limit the operation frequency in a range of few hundred MHz, multiplayer printed circuit boards have to be used when the operation frequency is exceeded and there are two layers or multi layers power ground plane to provide stable voltage. To conclude the above, following the increase of the operation frequency of the system, increasingly uses of decoupling capacitors and the use of multiplayer power ground plane are the efficient ways to suppress the ground noise. When the frequency gets higher, the use of the technique of embedded capacitors or in-chip large amount of decoupling capacitors are other choices to suppress the ground noise.

Power bus impedance is the model to evaluate the ability to suppress the ground noise. For example, if the voltage of a system is 1.5V, its ground noise cannot exceed 5% of the power. When the current of the circuit needs 20 ampere, power bus impedance cannot exceed 0.0375 ohm, otherwise the ground noise will exceed 5%. So how to correctly use the decoupling capacitors to lower the power impedance becomes very important. Before choosing the decoupling capacitors, it is necessary to decide the impedance value of the power bus system. In this paper, two methods are used to find power bus impedance. The first method is to use hspice lump circuit. Cut the power and ground plane into tiny cells horizontally, compared to the smallest wavelength of the operation frequency, the area of the tiny cells has to be much smaller (needed to be 10 times smaller), then the original distributed calculation circuit can be changed to equivalent lump circuit. This can greatly simplify the calculation and the result is very accuracy. By Lee and Barber method [7] the distributed plane model can be built with a two-dimensional array of C's, R's, and L's as showed in Fig. 1. The capacitance of every cell is $C = \varepsilon \frac{l^2}{d}$, where ε, d and l are the dielectric constant, the thickness of the dielectric and side dimension of the cell respectively. The capacitance of the four corners is $C/4$ because its area is 1/4 of the cell and the surrounding capacitance is $C/2$ because its area is 1/2 of the cell. The effective resistance and inductance of every cell are calculated as $R = 2\frac{\rho}{t}$ and $L = \mu d$, where $\rho, \mu,$ and t are the resistivity of the plane, the permeability of the substrate and the thickness of the planes, respectively. The resistance and the inductance of the cells are R and L, respectively, and the surrounding power impedance and the inductance is $2R$ and $2L$, respectively, because the surrounding width is half the width of the cell, thus the impedance and the inductance are double. Figure 2 shows the equivalent lump circuit of the power plane. Hspice can be used to simulate the power bus impedance. Another point needed to pay attention to is the side dimension l of the cell. The shorter it is, the more accurate it is but longer the time it takes. How to get the balance needed to be discussed. we will refer to Chois' proposed formula[9].

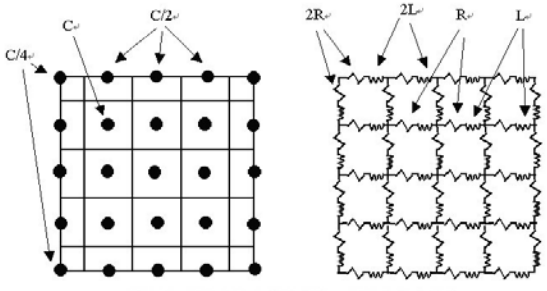

Fig. 1 The distributed plane model built with a two-dimensional array of C's, R's, and L's

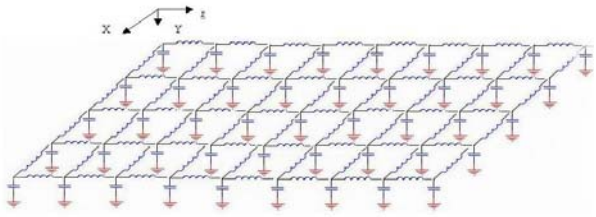

Fig.2 The equivalent lump circuit of the power plane.

$$2f_{\max} = \frac{c}{2\sqrt{\varepsilon}}\sqrt{\left(\frac{M}{a}\right)^2 + \left(\frac{N}{b}\right)^2} \text{ and}$$

$$l < \sqrt{12(2-\beta)\beta \frac{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}{\left(\frac{m\pi}{a}\right)^4 + \left(\frac{n\pi}{b}\right)^4}}$$

where $f_{\max}$ is the maximum system frequency, C is the light speed, ε is the dielectric constant of the material, a and b is the size of the power plane, M and N is the divided equal portion numbers of x axis and y axis, β is the expected eigenvalue difference.

The second method to find out the power impedance is to use Leis' proposed formula [8].

$$Z_{ij} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left(\frac{j\omega\mu h C_m^2 C_n^2}{P_x P_y\left(k_{xm}^2 + k_{yn}^2 - k^2\right)}\right)\cos\left(k_{xm}T_{xi}\right)$$
$$\times\cos\left(k_{xm}T_{xj}\right)\times\cos\left(k_{yn}T_{yi}\right)\times\cos\left(k_{yn}T_{yj}\right)$$
$$\times\operatorname{sinc}\left(\frac{k_{xm}L_{xi}}{2}\right)\times\operatorname{sinc}\left(\frac{k_{xm}L_{xj}}{2}\right)$$
$$\times\operatorname{sinc}\left(\frac{k_{yn}L_{yi}}{2}\right)\times\operatorname{sinc}\left(\frac{k_{yn}L_{yj}}{2}\right)$$

where *Px* and *Py* represent the printed circuit boards widths in the *x*- and *y*-directions, respectively, *h* is the height of the printed circuit boards, *Txi*, *Txj*, *Tyi* and *Tyj* are the coordinates of the center of the *i*th and *j*th ports in the *x*- and *y*-directions, respectively, *Lxi*, *Lxj*, *Lyi* and *Lyj* are much less than the wavelengths of interest and represent the *i*th and *j*th port widths in the *x*- and *y*-directions,respectively, *k* represents the real wavenumber for the lossless case, $k = \omega\sqrt{\mu\varepsilon}$, $k_{xm} = \left(m\pi/P_x\right)$, and $k_{yn} = \left(n\pi/P_y\right)$. The first one is a constant factor, $\frac{\mu d C_m^2 C_n^2}{P_x P_y}$, the second one Green's function factor, $\frac{j\omega}{k_{xm}^2 + k_{yn}^2 - k^2}$,is the only one dependent on frequency, defines the locations of the poles and peaks in the system impedance. The third one is cosine factor which decides the variation of the impedance value when the circuit printed boards are in different positions. In different coordinate, the impedance value will be different. The fourth one is sinc factor which is related to the segmentation of the PCB. Through this formula, we can find out the resonant frequency and can also discuss the affect of position on impedance. When the size of the printed circuit boards becomes bigger, lower the resonant frequency is and closer to the center it is, because of cosine, some resonant points can be eliminated. How to choose decoupling capacitor is based on the position of the resonant points. Eliminate every resonant, from which the interested frequency range will be smaller than the power target impedance. Figure 3 is the comparison between the measured Z_{21} on the printed circuit board 27cm x 15cm and the two above-mentioned simulations Z_{21}. It shows clearly that the resonant points and the impedance values are well matched. The hspice simulation result (blue line) is close to the measured result (red line). The resonant impedance value from the formula is higher (black line), that means through the simulation method, the power bus impedance which go according to the change of the frequency of the two-sided printed circuit board, still can be estimated correctly.

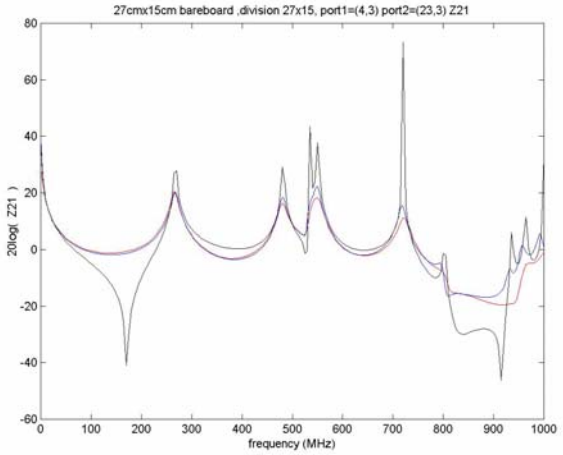

Fig. 3 The comparison between the measured Z_{21} on the printed circuit board 27cm x 15cm and the two above-mentioned simulations Z_{21}

3 Genetic Algorithm Optimal Decoupling Capacitors

Genetic algorithm mainly includes three

processes: reproduction, crossover and mutation. However, before preceding these processes, we have to encode every parameter into a finite bit string (i.e. one string represents one parameter). And randomly pick up a certain amount of individual base on the need of the question as an initial population. Decode the initial population and define a fitness function according to the purpose of the question to evaluate the adaptability and behavior of every individual and find out if this individual should be survived or not. Then reproduce the best one according to its fitness function value. After reproduction, base on the crossover probability of the newly produced population, randomly pick up two individual of the population and exchange part of the bit value of certain strings of one population enhance the production of a new production. Then pick up the best string from the information exchange pool to become a real value after decoding. Thus evolution of one generation after another, liked the natural development in the biological field, until the qualified optimization is found. When apply to genetic algorithm optimization, according to experience, the difficulties are how to decide: (1) the range of variations, (2) length of the bit string, (3) the population size, (4) crossover probability, (5) mutation probability, (6) fitness function, etc. since these variations will affect the final results. If it is applied to the search of parameters, genetic algorithm has to encode the range of the parameters and the range will seriously affect the result. And talking about the structure of the genetic algorithm, the length of the bit string will affect the resolution. The more the numbers of the bit string, the more accurate of the parameter and the better the result it will be. But it will take more calculating space and time relatively. As for the population size, the bigger the size, since more initial strings can be produced, there are more chances to produce the strings which have stronger adaptability and the search result will be better. But again it will take more calculating space and time. Also the selection of crossover probability and mutation probability plays an important role in the entire searching process. If the crossover probability is too large, it may result in the loss of the best factor. If it is too small, it will easily slow the process of evolution. And the decision of the fitness function is even the essence of genetic algorithm. How to face the core part of the problem and set up a qualified fitness function is another important issue of this paper.

Figure 4 is the diagram of the power bus circuit of this paper. We use formula Z_{ij} to find out the impedance value of the parallel plane and use different values of decoupling capacitor to reduce the impedance value of the power between the parallel planes. First set up a decoupling capacitor file for capacitor with different values, then find out the parallel impedance value of Z_{ij} and decoupling capacitors, and use genetic algorithm optimal selection of the number of the decoupling capacitor. Because there is difference in the value of the decoupling capacitors, the areas occupied on the printed circuit board is also different, so depending on the numbers used as an optimum is not always accurate. If taking the occupied area into consideration, a weighting factor can be included, so we can set the target as minimized $W_1N_1 + W_2N_2 + W_3N_3 + \cdots + W_nN_n$ to satisfy $Z < Z_{target}$, N_i is the number of different vale of decoupling capacitor used, W_i is its corresponding weighting. Fitness function can be defined as

$Fitness = W_iN_i + Penalty$ if $Z > Z_{target}$

or $= W_iN_i$ if $Z <= Z_{target}$

$Penalty = Coeff.x|Z - Z_{target}|$

When the impedance $Z > Z_{target}$ and a factor is included, the principle of evolution will not be fulfilled and through this process, the best combination can be obtained. Through hspice to simulate, we can see if these obtained values have the best result or not, we can also use the actual production of the printed circuit boards to verify the accuracy of result if the S-parameters are changed to Z-parameters.

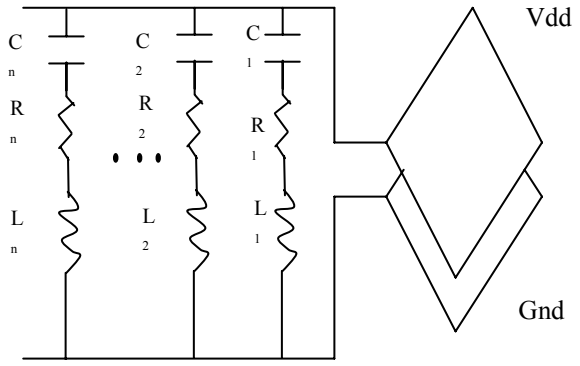

Fig.4 The diagram of the power bus circuit with decoupling capacitor.

In this paper, we choose 20 capacitors with different capacitance and its series impedance and inductance, use GOAT genetic algorithm optimal using of the numbers of capacitor to find out or measure the power impedance as shown inFig.3. To simplify, assume 1Ω is the targeted impedance, the number of capacitor used inversion is the targeted fitness, Figure 5 is the development process of the targeted

fitness. When the targeted impedance is 1Ω, the best number of capacitor used is 5. Table 1 lists all of the selected capacitors used in the simulation. What we need to pay attention is optimization is not the only way. The maximum power bus impedance value of using 5 decoupling capacitors is 0.998Ω, which satisfy the assumed target impedance. Figure 6 shows the power bus impedance whether adding or not adding decoupling capacitors. Clearly, the impedance is significantly reduced by adding decoupling capacitors. Figure 7 is to verify the accuracy of the result of genetic algorithm optimization. In the diagram, it is obvious that the impedance value will be 1Ω if any one of the capacitor out of these five is lacking. For example, if 680nF capacitor is deleted, the impedance value is 8.4Ω, 10nF capacitor is deleted, the impedance value is 1.2Ω, 470pF capacitor is deleted, the impedance value is 1.23Ω, 33pF capacitor is deleted, the impedance value is 1.45Ω, 22pF capacitor is deleted, and the impedance value is 1.12Ω. From this example, we learn that using genetic algorithm, we can obtain the optimal number of capacitor used, and this can solve the problem of depending on using experience.

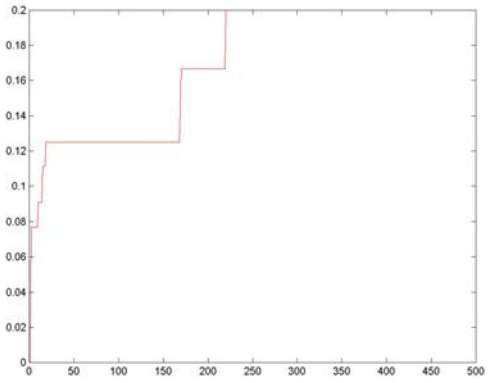

Fig.5 The development process of the targeted fitness used genetic algorithm optimization.

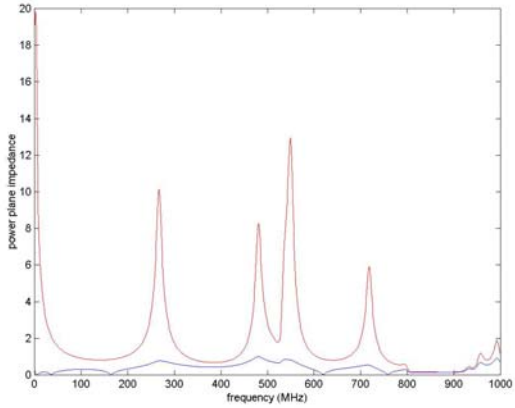

Fig.6 The power bus impedance whether adding or not adding decoupling capacitors.

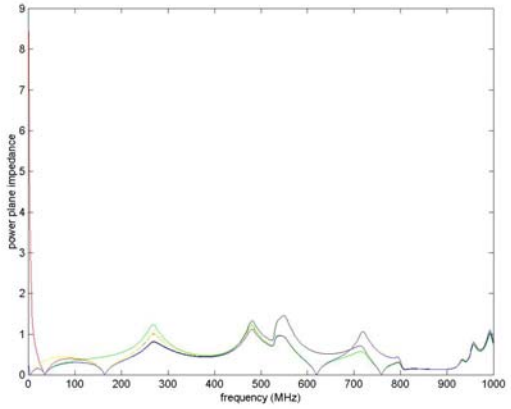

Fig.7 Verify the accuracy of the result of genetic algorithm optimization with or without any one of decoupling capacitor.

Table 1 All of the selected capacitors used in the simulation

Capacitor (F)	ESL(H)	ESR(Ω)	Numbers
680e-6	5e-9	0.01	0
100e-6	5e-9	0.01	0
68e-6	5e-9	0.01	0
10e-6	3e-9	0.01	0
6.8e-6	3e-9	0.01	0
1e-6	3e-9	0.01	0
680e-9	2e-9	0.01	1
100e-9	2e-9	0.01	0
10e-9	2e-9	0.01	1
1e-9	2e-9	0.01	0
680e-12	2e-9	0.01	0
470e-12	2e-9	0.01	1
100e-12	2e-9	0.01	0
82e-12	2e-9	0.01	0
47e-12	2e-9	0.01	0
33e-12	2e-9	0.01	1
22e-12	2e-9	0.01	1
18e-12	2e-9	0.01	0
15e-12	2e-9	0.01	0
10e-12	2e-9	0.01	0

4 Conclusion

From the above discussion, it is clear that the resonant behavior of the power impedance can be accurately simulated through formula and hspice, and compared to the measured value, it has well accuracy. So the simulated impedance value and the measured value can be used to optimize the number

of decoupling capacitor used. In this paper, we use genetic algorithm to optimize the selection. From the simple example listed above, it is very obvious that through this method, we can estimate correctly the least number of capacitor used, which will solve the problem of using experience to make decision in the past and provide a good reference for the designers in the future. In this case of the PCB with dimension of 27 cm by 15 cm PCB, the minimum number of capacitor is five with a specified target impedance of 1Ω and the most effective location of decoupling capacitor is nearby the input port. In addition, the RLCG equivalent circuit modeling power/ground plane in spice simulation was examined with the decoupling capacitor to find the best location.

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