Test pattern designing software for electrical appliance testing platform.

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Abstract: -This paper presents the design and implementation of software for creating test patterns and communicating them to a test platform for electrical appliances as well as the architecture of the testing platform. The software lets the user design different types of voltage fluctuations, repeat and sequence them making testing Series and store them on a PC. The testing Series are communicated with special protocols to the platform. The architecture of the platform consists of a DC/AC inverter that can produce variable frequency and variable voltage up to a maximum voltage level, Spike Production Circuit to produce spikes at levels higher than that of the inverter and electronic relay circuit for switching between the inverter and the Spike Production Circuit. Microprocessors control the inverter, the Spike Production Circuit and the relay in order to produce the desired output waveform to the appliance/device-under-test. The algorithms running on the microprocessors are presented.

Keywords: -Test Pattern Software, Appliance testing platform, Microprocessor algorithms, Communication protocols

1 Introduction

Power networks experience many abnormalities, which are unavoidable and most of the times are harmful and reduce the lifetime of the electric appliances. This paper presents the design of software and the architecture of a testing platform, which has the ability to cause voluntary electrical distress on the appliances in a similar way with the power network and in a programmable and repeatable fashion

The software is designed in such a way to give the user the ability to design and store testing patterns, make modifications on the type of programmed disturbances (different frequency, voltage, current, or energy of the spike) and then design new patterns and tests. Functional problems of the electric appliances caused by the abnormalities of the power network voltage depend on the nature of the appliance [1]. This type of platform helps in the acquisition of the "know-how" around the requirements of each appliance in power supply. Appliances can be designed to embody effective protection from the abnormalities of the power network. The platform will also offer the ability to classify the electrical appliances depending on their internal structure. Finally, the classification of the requirements for each electric appliance group will be able to be performed. The problems that appear in the electrical appliances from the abnormalities of the power network are of different kinds and depend mainly from the type of the appliance.

The Architecture of the testing platform will be presented in section 2. The testing Patern software features will be presented in section 3. How the patterns are created and sequences to make test Series are presented in section 4. The algorithms running on the processors of the testing platform follow in section 5. Conclusions are drawn in section 6.

2 Testing Platform Architecture

The Architecture of the Testing Platform is shown in fig. 1.

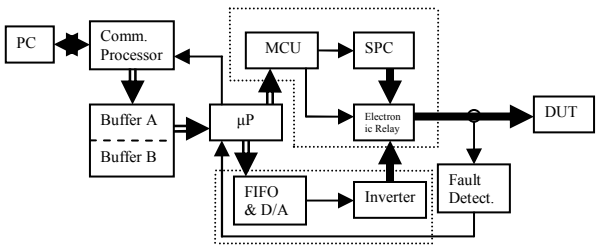


Fig. 1: Architecture for electrical appliances testing platform.

On the software running on the PC, testing patterns are designed and stored. When a test is to be performed to an appliance, the test sequence is assembled. When the test is ready to be exercised, the data is send from the software to the platforms's Communications Processor through a PC port. The Communications Processor fills up Buffers A and B with the test patterns in an interleaving fashion. The platform's central microprocessor (μP) reads the information from the Buffers, processes the commands and produces output voltage waveform data. It then decides if the output voltage will be produced by the inverter or by the SPC. If the slew rate of the voltage signal is high, or the maximum voltage is high, then the output voltage will be produced by the SPC, otherwise it will be produced by the inverter. The central microprocessor will distribute the voltage waveform data to the inverter or to the SPC.

The platform's central microprocessor will place the output voltage waveform data for the inverter in a FIFO memory. The FIFO feeds the D/A of the inverter for the production of the output voltage waveform. The frequency of the input reference signal of the inverter is digitally controlled from the Microcontroller. The amplification of the inverter is also controlled digitally using a digital potensiometer. The DC/AC inverter [2] can produce a variable frequency and variable voltage output. The inverter [3-5] uses a wide bandwidth design and is able to distort one or both of the peaks of its output sine-wave. This way the main abnormalities of the power network can be produced. The frequency and voltage variations can be easily produced. The microprocessor algorithm has the ability to change the amplification rapidly and produce peak and in general signal distortion at the output waveform.

The SPC's MCU will receive the output voltage's waveform from the central microprocessor only when it is out of the inverter's specifications. The SPC has the ability to produce high voltage with high bandwidth and at high slew rate that the inverter cannot do. Then the MCU will make the proper arrangements in order the SPC unit to produce the required voltage. The MCU has to control the relay to switch the produced voltage to the device under test and then switch back the relay to the inverter. The MCU is able to control the operation of the High Voltage Converter which determines the spike amplitude. The MCU also controls the relay switches of the Capacitor Bank and this way it changes the connected capacitance. The connected capacitance is possible to control the total energy of the spike. An Electronic Relay switches the DUT between the inverter and the SPC very fast.

3 The Testing Pattern Software

A PC application software was developed to interface the platform with a PC. The program is able to generate and store different testing patterns. This way the platform has the ability to cause electrical distress at the appliance in a programmable and repeated fashion. The application program has three main parts. In the first part, the user can manually control the output waveform while the platform is in operation. In the second part the output waveform of the inverter can be programmed and in the third part the spikes from the SPC can be programmed. The screen of the program that controls manually the output waveform of the inverter is shown in Fig. 2.

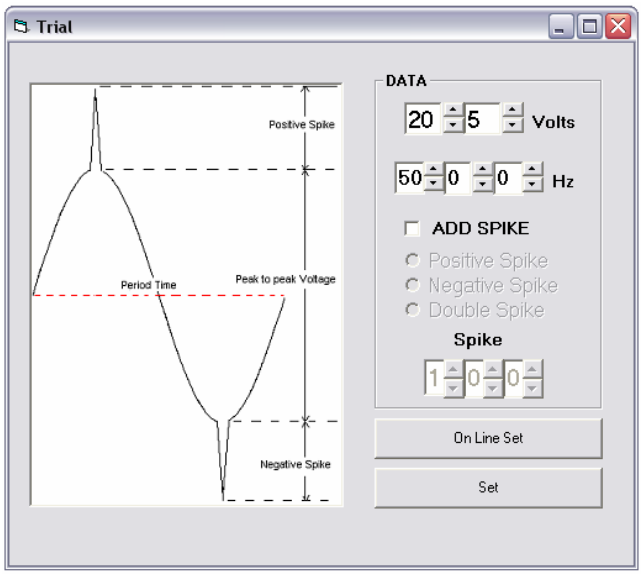


Fig. 2. The real time control screen of the output waveform of the inverter.

In this screen, it is possible to set the voltage and the frequency of the inverter and also to distort the peaks of the inverter output waveform with spikes. The real time control of the platform is helpful when is desirable to test the platform. Respectively, the screen of the programmable output waveform of the program is shown in Fig. 9.

The user can assemble a testing waveform consisting of different patterns. On the left side of the screen the user can give the parameters for inserting a pattern. The patterns will be executed in order. The stored data of the inserted patterns are shown in the white area of the screen where each row represents one pattern. The first number is the RMS Volts of the inverter output, the second is the frequency multiplied by 100. The symbol in the

third position represents the type of the peak spike and the number that follows is the peak value of the spike. The "+" sign designates positive spikes, the "-" sign designates negative spikes, the "=" sign designates both positive and negative spikes, "X" sign designates no spikes. In the last position the number represents how many seconds will be the duration of the pattern. Figure 3 shows the screen for controlling the inverter for producing test patterns of sine waves of different characteristics with the option to have spikes on the peak(s)

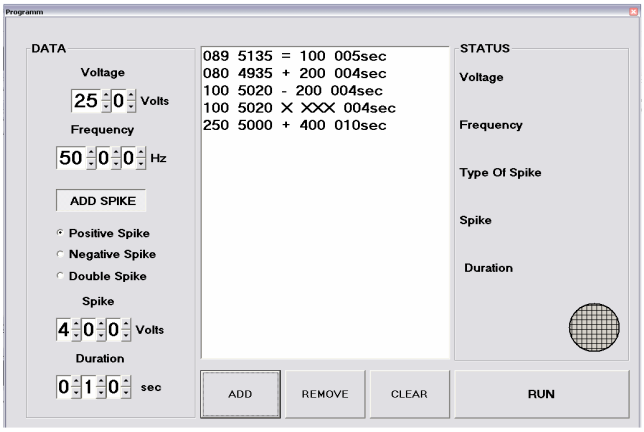


Fig. 3. The programming screen of the output waveform of the inverter

A more details software was developed that can produce any type of waveform. The software program contains pre-defined patterns inside libraries that is possible to be edited and enriched from the user. In the figure 4 is shown the contents of the waveform library.

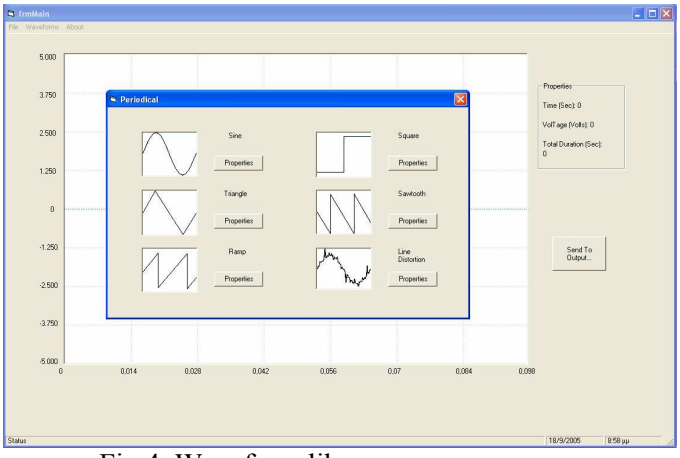


Fig.4. Waveform library.

The type of the abnormality is usually an irregular function. Such type of functions can be designed even pixel by pixel from the user and is also possible to be used as a library. The pre-defined patterns of the irregular functions are shown in figure 5.

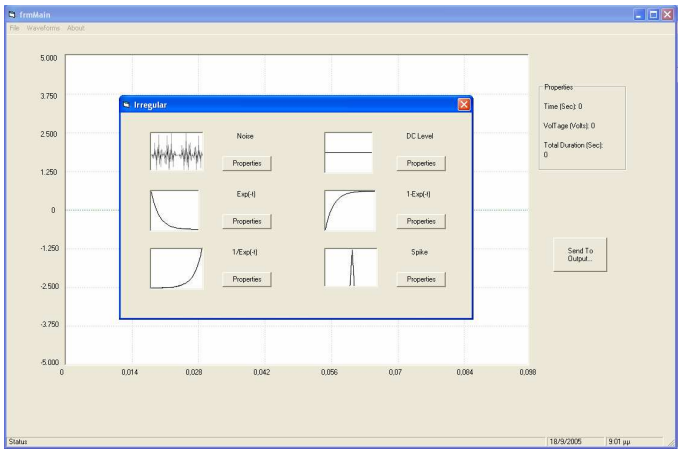


Fig.5. Patterns of the irregular functions

4 Making Patterns, Sequencing and test formation

The program is possible to produce long time sequences of patterns in order to create appliances test waveforms. This is achieved by placing the waveforms in time sequence and with the use of combine function. In figure 6 is shown the form of the combine function.

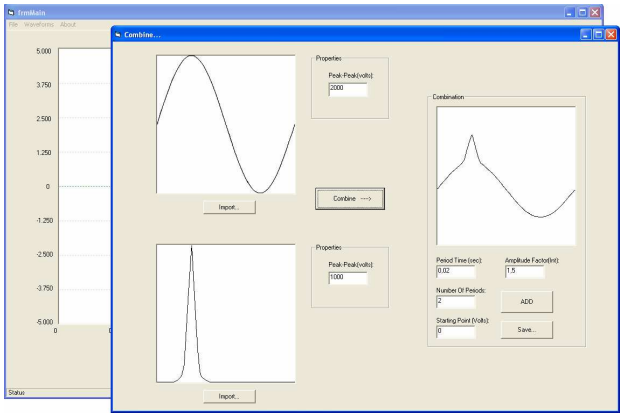


Fig.6. Combining two functions.

In this form two waveforms can be loaded from a file or a library and the ratio of their amplitudes is determined from their properties. The starting point of the resulted waveform can determine a DC point. The period time determines the frequency and the number of periods determines the total time that the waveform will be produced. In figure 7 the way that a library opens to select a waveform for combining is shown.

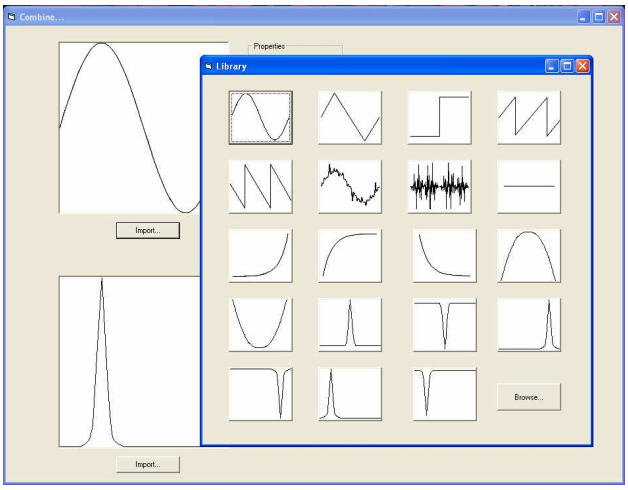


Fig.7. Combining functions library.

An example of a produced test pattern result is shown in figure 8 and could also be added to the Functions library.

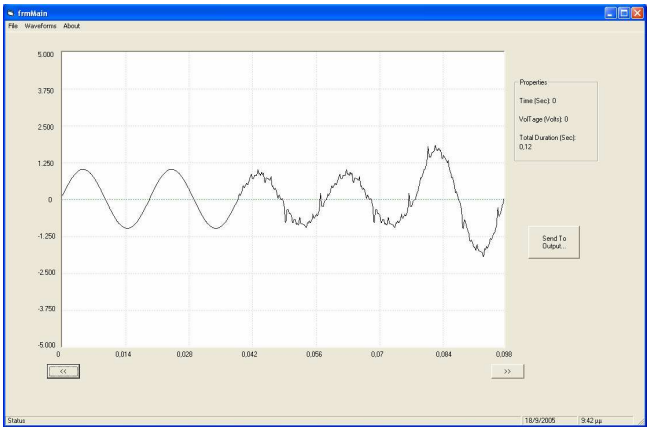


Fig.8. Resulting testing pattern example.

A testing sequence designed by the user for one appliance is broken down, by the PC software, to a series of test patterns or packets each consisting of Header (H) and Data as shown in figure 9. Each packet contains information of one test pattern as shown in figure 10. Each packet/test contains information for a number of periods of the produced voltage signal. The first number in the header defines the duration of each period of this test in msec. which is constant for the duration of the test. The second number in the header defines the number of periods in the test. For each period in the test, 256 points are given in the Data field on the packet/test. Each point is a 16-bit number representing the voltage signal value. The third number in the header defines how many times the whole test will be repeated. Figure 11 shows an example wherein the Header the Period is 21msec, the Number of Periods which data will be given is 9 and the whole test will be repeated 5500 Times. In the Data section of the Packet is shown the size 3x256 of the data points.

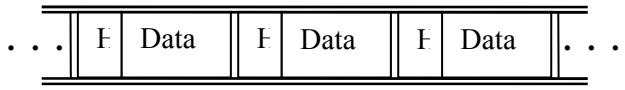


Figure 9. The Protocol

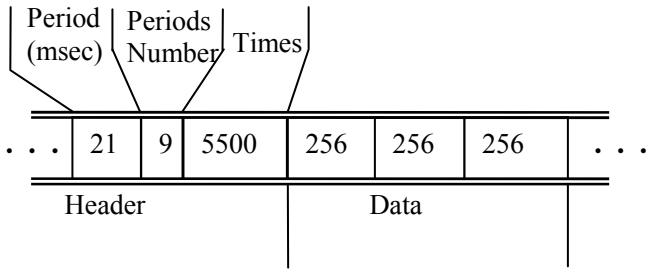


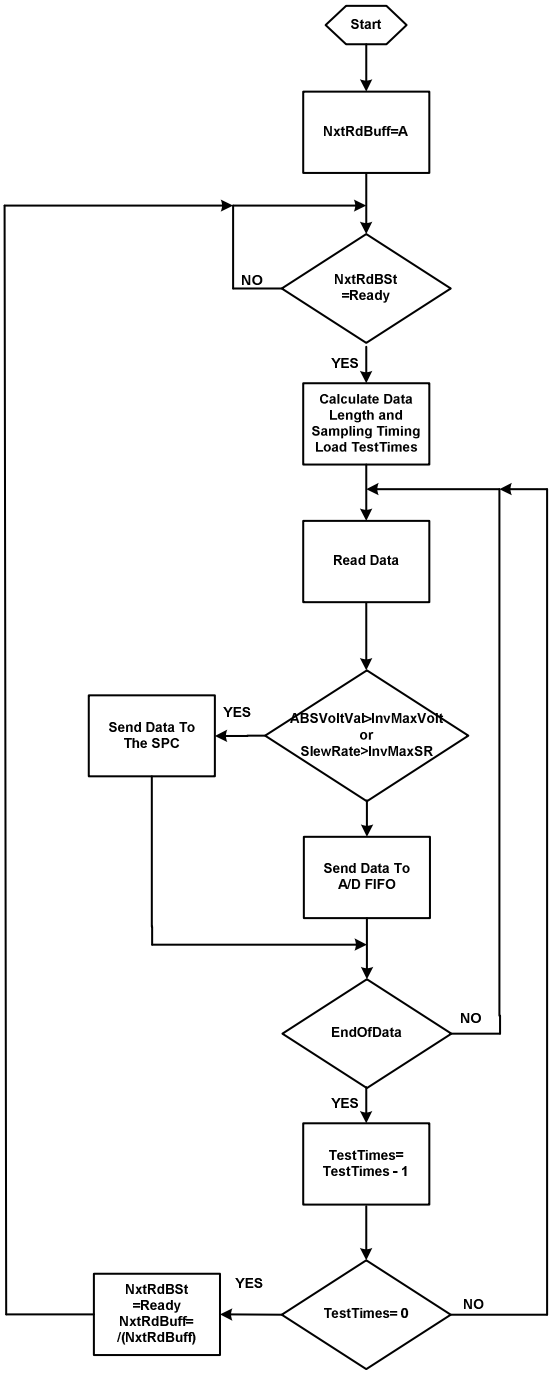
Figure 10. The Packet

The data will leave from the PC through a port and will be received by the communications processor of the control system. The PC will send the testing patters in the form of packets, one test per packet. The communications processor will place each packet in one of the two communication buffers: BufferA or BufferB in an interleaving fashion. While the Central processor is reading, processing the data and performing the test from the one buffer, the communications processor brings the data in from the PC to the other buffer to be ready for the following test.

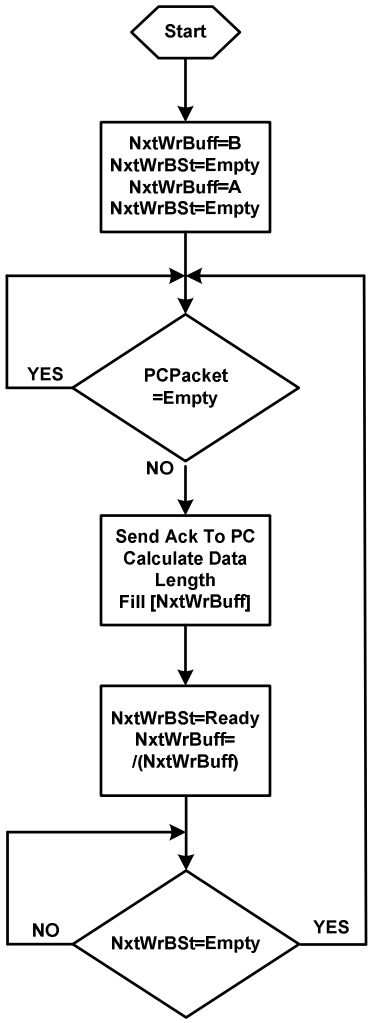
5 The Processing Units

The Control System of the platform is based on a central microprocessor (μP) and another processor (MCU) that controls and programs the SPC and arranges for the switching of the SPC. Another processor was used to handle the communication with the PC called Communications Processor. The algorithms running on each of the processors are shown in Fig. 11. Each of the BuffersA and BufferB has a status variable that is hold in the Buffer itself. The status of the Buffer is Empty, Write, Ready, Read. The Communications Processor can change the status of a Buffer and Write in it when the buffer is Empty. Then the Communications Processor changes the status of the Buffer to Ready. The Central Processor can change the status of a Buffer and Read from it when the buffer is Ready. Then the Central

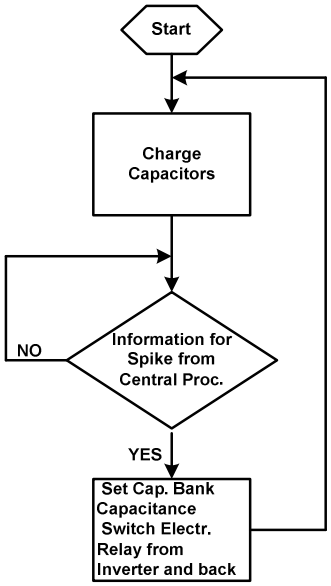
Processor changes the status of the Buffer to Empty. Communications Processor has a NextWriteBuffer (NxtWrBuff) binary variable where is kept which of the two buffers is the next buffer to be used by the Communications Processor for Writing. Central Processor has a NextReadBuffer (NxtRdBuff) binary variable where is kept which of the two buffers is the next buffer to be used by the Central Processor for Reading. NxtWrBSt, NxtRdBSt are the status variable of the buffers.



(a) Central Processor



(b) Comm. Processor



(c) MCU

Fig. 11: Algorithms of the microprocessors.

6 Conclusions

An Electrical Appliance Testing Platform was designed, constructed and tested on the laboratory. This platform is able to produce the most typical abnormalities of the electric power network and can be used to bring knowledge about the sensitivity of the appliances to them. This way more sufficient protection against the power network absnormalities can be utilized in the appliances and people will have less problems with them. A software that includes many testing pattern was constructed where the user may combine testing patterns to make new patterns. Also the patterns can be sequenced to make test series for testing the endurance and behavior of electrical appliances in fluctuations of their input voltage signal. The implementation of the software with many features makes the appliance testing platform very usable and manufactures of electrical appliances can now easily test the endurance of their appliances under different tests in a repeatable fashion and for long time periods.

Acknowledgments

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