High-Speed POF Receivers

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Abstract: - In this work we present a high-speed optical receiver with external large-area photodiode. The optical receiver is realized in 0.35μm SiGe BiCMOS technology. The input circuit is a two-transistor transimpedance amplifier using an common-emitter and an emitter-follower configuration. An external silicon PIN photodiode of a squared area of 0.25mm² with a rise time of 0.4ns at 850nm light is used. The POF-receiver offers quick response for 1.25Gbps optical wire-line access networks. In addition a high sensitivity is also required, where the receiver presented reaches a sensitivity of -26dBm at the optical input using low-cost silicon-based material only.

Key-Words: - Low-Noise, Plastic-Optical-Fiber, external large-diameter photodiode, BiCMOS, 0.35μm-SiGe, optical interconnects, last-mile.

1 Introduction

Optical interconnects offer a solution for the increased bandwidth demands in communication traffic within electronic systems, e.g., from long haul to last-mile communication traffic, which is growing rapidly as Internet including varied high definition and fidelity multimedia use expand. Further similar opto-couplers and transceivers may speed up information interchange between electronic boards via optical backplanes or via free space, in distributed microcontroller applications or even in multiple split central processing unit cores within Harvard-architecture-based high-speed micro-processor systems. In fiber-systems high-bandwidth and high-sensitivity optical receivers are especially necessary when many couplers or many beam splitters are implemented in the optical transfer path. The same demands hold for free-space optical interconnects when the emitted optical power is spread over a large area to reach many receivers.

The optical receiver described here might also be interesting for application in short-range data transmission via optical fibers in last-mile up to local area networks and for fiber-to-the-home (FTTH). Due to its EMI-safety and galvanic isolation it may even find indispensable applications in robotics industry or automotive and aerospace applications. Low-cost, high-reliability, and high-performance photo receivers are needed to support the growth of optical interconnects. Further reduced power consumption requires smaller minimum feature-size and low-noise CMOS or BiCMOS technologies, also gaining the reliability of all system components involved.

The presented approach results in the advantage of lower costs of a silicon external large-diameter photodiodes and small circuit chip area in rather costly high-speed and low-noise SiGe (Silicon-Germanium) technology compared to an OEIC (opto-electronic integrated circuit) in the same technology. This is because for a photodiode only one sixth to one eights of mask and processing steps compared to an IC process is necessary. Low costs are important for mass products like plastic-optical-fiber systems and for short-distance optical interconnects which are used e.g. in distributed microcomputer applications, and even short-distance free-space transmission. Furthermore the photodiode and the amplifier can be optimized independently and therefore a better performance compared to an OEIC solution can be achieved especially for large-area photodiodes, non-massively parallel receivers and longer optical wavelengths.

Optical diffuse, not always line-of-sight free-space data transmission between different computers, printers, scanners, consumers and entertainment electronics within rooms in apartments or offices also requires highly sensitive receivers.

2 Circuit Aspects

The general issue in question to solve is to find the amplifier's optimum operating point for low-noise and high-speed capability, and at the same time avoiding any noise contribution through the current sources or passive components, what usually form a complex multi-pole optimization problem with many tradeoffs and limitations as well.

The circuit we have chosen, is a two-transistor transimpedance amplifier receiver in common-emitter and emitter-follower stage configuration as shown in Fig. 1, with an external PIN photodiode of a squared area of 0.25mm² a rise-times of 0.4ns, at 850nm light. We present considerations and results for both 660nm and 850nm, because these carrier wavelengths are beneficial in numerous aspects depending on several

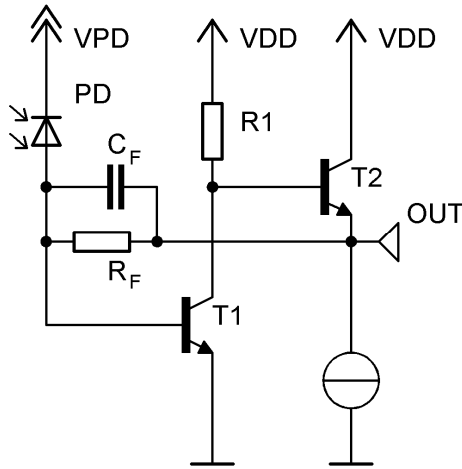circumstances for POF- and PCS-based systems, respectively. [1]

Fig. 1: Simplified schematic of the main TIA stages

A mathematical model aggregation of the bandwidth optimization issue is given in (1), where R_F is the feedback resistor, C_F the capacitance in parallel to R_F connecting the TIA circuit's input and output stage,

$$f_{-3dB} = \cfrac{1}{2\pi \left(R_F \cdot C_F + \frac{C_{\pi 2}}{g_{m2}} + \frac{1+g_{m2}\cdot R_F}{(1+g_{m1}\cdot R_1)\cdot g_{m2}} \cdot C_f \right)}, \quad (1)$$

with

$$C_f = C_{PD} + (1 + g_{gm1} \cdot R_1) \cdot C_{\mu 1} + C_{\pi 1}, \quad (2)$$

which contributes the diode capacitance C_{PD} the effect of the first stage's base-collector capacitance converted by Miller's theorem, and base-emitter capacitance $C_{\pi 1}$, where R_1 is the current limiting line resistor of the common-emitter circuit stage amplifier, with the transconductance g_{m1}.
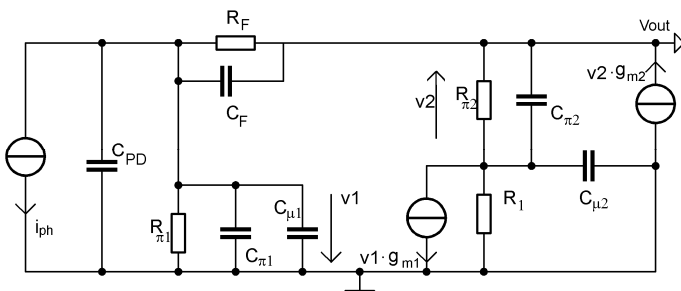

Fig. 2: Small-signal equivalent circuit of the circuit in Fig. 1

The AC small-signal equivalent circuit in Fig. 2 yields an overview over the used abbreviations for the derivation of equitation (1) and (2).

A major drawback of the large-diameter photodiode is the limited speed, due to huge capacitance at the input node of the TIA in the order of several pF, much more than parasitic bond-pad capacitances. Besides the influence on the bandwidth, the large input-node capacitance of the TIA also may result in a lower

sensitivity, which can be critical for the POF receiver. Therefore, we use an appropriate photodiode at higher reverse voltage to reduce its capacitance.

3 Realizations and Measurements

Tab. 1 lists a short comparison of published results on highly sensitive and high-speed POF receivers.

Process	Sensitivity	Detector & noise current	Data rate	Ref.
0.35 SiGe BiCMOS	-30.2dBm BER=10⁻¹⁰	6·0.4 A/W 13.2pA/√Hz	1.25Gbps	[2]
0.6μm BiCMOS	-22.1dBm BER=10⁻⁹	0.36 A/W 11.7pA/√Hz	1.5Gb/s	[3]
0.6μm BiCMOS	-23.0dBm BER=10⁻⁹	0.36 A/W 23.3 pA/√Hz	250Mbit/s	[4]
MSM GaAs	-15.7dBm BER=10⁻⁹	0.22 A/W 24.2 pA/√Hz	2.5Gbps	[5]
0.12μm CMOS	-29.1dBm BER=10⁻⁹	0.85 A/W **6.0pA/√Hz**	1.25Gbps	[6]
0.35 SiGe BiCMOS	-26.0dBm BER=10⁻⁹	0.49 A/W **7.1pA/√Hz**	1.25Gbps	This work

Tab. 1: Comparison of a few published comparable and competitive POF receivers.

Ref. [2] uses an avalanche photodiode with a multiplication factor of 6 to reach a higher sensitivity. The POF receiver in [6] has a lower average noise current, but at the expense of much higher CMOS 0.12μm mask costs than in 0.35μm SiGe BiCMOS and it is worse in figure of merit, with the much smaller detector area of 490μm², requiring a costly lens, compared to this works detector's area of 0.25mm². The figure of merit PFM (POF-Figure-of-Merit = PFM) we introduce is given by

$$PFM := \frac{A_{PD} \cdot DR}{\sqrt{\overline{i_n^2}}}, \quad (3)$$

with the detector's area A_{PD}, the date rate (DR) and the average input noise current at the given data rate in the denominator. Therefore the PFM value in [6] reaches just 102.27e9 m²/A·bit/√Hz compared to 8.64e12 m²/A·bit/√Hz in this work.
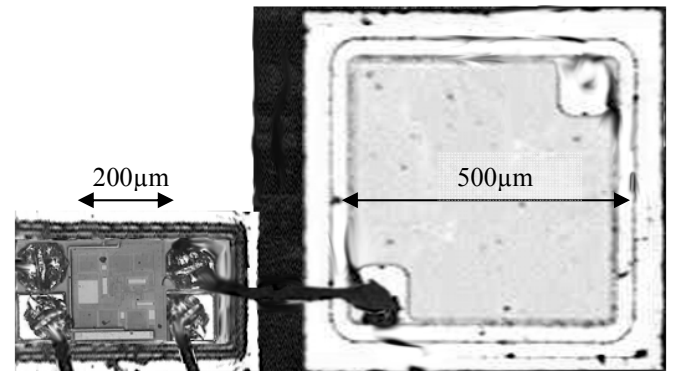

Fig. 3: Chip-photo of the receiver (left, bottom) and the PIN photodiode (right).

Fig. 3 provides a chip photograph of the entire POF receiver, illustrating the benefits of the external

photodiode, such as the circuit chip can be processed in a commercial technology optimal for high-speed and low-noise circuits, requiring a comparably small chip area. The properties of the photodetector chip can be optimized independently, in respect to the material system, design and process steps. In our case we have chosen the PIN diode PS0.25 from Silicon Sensor. The PIN detector is on a lightly n-doped silicon substrate reaching responsivities of 490mA/W @ 850nm and 368mA/W @ 660nm. At a bias voltage of 20V the diode has a bandwidth of 900MHz @ 850nm light and a capacitance of 1.12pF.
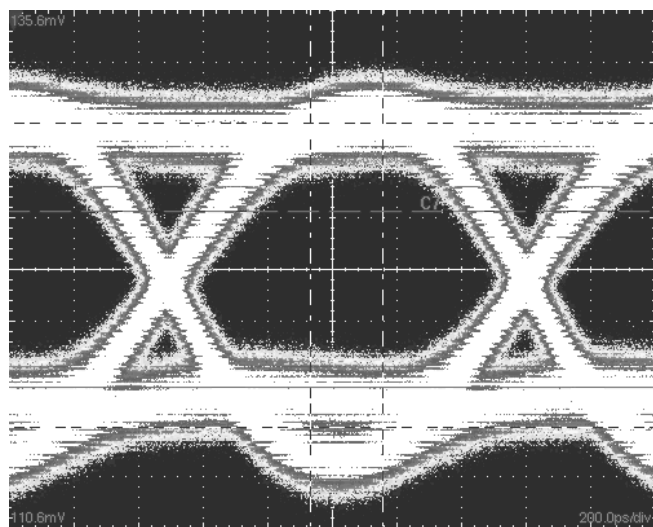

Fig. 4: Measured eye diagram at 1.25Gbps @ 660nm.

In Fig. 4 we provide an eye-diagram taken at a data-rate of 1.25Gbps, using the Communication Signal Analyzer CSA8000. By counting errors with an bit-error analyzer, we achieved a sensitivity of -26.0dBm at a BER of 10^{-9} at 850nm and a PRBS (Pseudo-Random-Bit-Sequence) of 2^7-1.
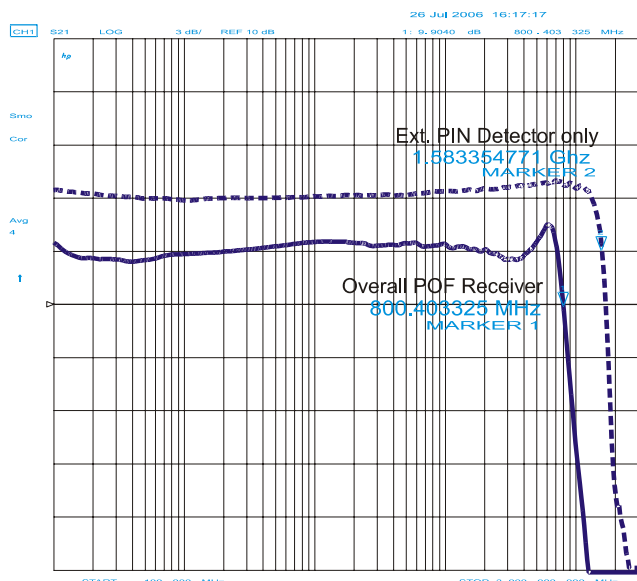

Fig. 5: Measured AC–characteristics of the TIA presented (solid line) and an external PIN diode alone (dashed line).

The AC measurement result of the TIA presented in Fig. 5 present the transfer characteristics of the overall receiver and the PIN detector alone, biased at a reverse voltage of 50V with detecting an 850nm 10Gbps laser source's signal at 27µW optical power at the input, but at different internal reference levels of the Hewlett Packard 8753E, vector network analyzer.

4   Conclusion

An external photodiode is advantages compared to an integrated photodiode especially for large PD diameter, increased speed (because a higher bias voltage for the ext. PD or III-V compounds can be used) or wavelengths up to e.g. 1.5µm. Longer wavelengths allow a better optical sensitivity in combination with an amplifier possessing the same equivalent input noise current, due to the lower photon energy. Furthermore, even an external avalanche photodiode can be used to improve the sensitivity further. The presented receiver compares to an OEIC in [3] with -22.1dBm at 1.5Gbps and a GaAs OEIC in [5] with -15.7dBm @ 2.5Gbps both with much smaller integrated photodetectors. The POF OEIC receiver recently presented in [4] provides a sensitivity value of -23.0dBm at 250Mbps and 660nm. Compared to 0.12µm CMOS receivers, the equivalent input noise current of our 0.35µm SiGe receiver is only a little bit larger, but 0.35µm SiGe clearly has to be preferred for ASICs in low or medium production volumes due to considerably lower lithography mask costs.

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