# Low Complexity Passives in MCM-D 4G Mobile Phones

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*Abstract:* - Next generation wireless communication applications such as wireless local area networks (WLANs) around 5 GHz require low power and high quality integrated transceiver solutions. The integration of RF front end especially poses a great challenge to these applications as traditional system on chip (SOC) approach is quite inefficient. A system on package approach can address the problems in an optimum way. In this paper we present design & implementation of different passive element fabrication choices for wireless application. These passives are to be fabricated between different modules on an MCM-D substrate. Inductors and capacitors are compared on the bases of their Q-factors and SRF( self resonance frequency).

*Key-Words:* - Q-Factor, resonance Frequency, Integrate Components, MCM-D Technology

## 1 Introduction

Major advances are being achieved in digital system miniaturization through the use of advanced, submicron technologies, the transition from conventional peripheral leaded packages to Ball Grid Array, Chip Scale Packaging and other area array packages and the development of much higher connectivity circuit technologies. Miniaturization in RF systems presents a very different set of challenges that arise from the critical demands of high performance, wireless communications systems. Such systems commonly call for the use of a wide range of active device technologies and a high ratio of passive to active devices. Such systems are very sensitive to parasitic components introduced by the packaging and interconnection of the devices. One of the constraints on the design of integrated RF systems is the availability of suitable and cost effective components. MCM-D technology offers many of the necessary components and also gives the advantage of size, repeatability and external component count reduction. The MCM-D technology allows the integration of different families of ICs together with integrated passives to produce miniature radio modules and RF functions which offer considerable size and performance advantages over conventional discrete solutions. The benefits are further enhanced by the use of MCM-D[1] passive components to produce structures such as filters which would normally consume significant space and cost in a conventional design. The range of passive component values attainable and their performance is superior to that available in IC technologies as a consequence of the relatively low-cost per unit area and low dielectric loss of the organic materials In the next sections the set of manufactured integrated inductors and capacitors on low-cost MCM-D technology is reported together with the electrical performance analysis and measurement based lumped models suitable for design library implementation. Set of available design options and parameters and their influence on element performance is analyzed. Finally, the comparison of the modeled passives with full wave EM simulations and measurement results is shown as the lumped model of the integrated passives verification.

Simulation and extraction technique

SONNET Suite (relaese 10.1) 3D EM simulator based on the Method of Moments (MoM) has been chosen as a simulation technique used to calculate the behavior of the passives elements. SONNET is a full 3D EM analysis tool in that both 3D fields and 3D currents are included in the analysis. This is in contrast to 2.5D analyses which, while including full 3D fields, allow only 2D currents. The reason that we use SONNET is it is very accurate modeling of the ohmic losses. The loss at low frequency (where the conductor is much thinner than the skin depth) is calculated based on DC resistance. At high frequency this loss is simulated by means of skin effect surface impedance formulation. In this way also imaginary inductive part of the skin effect in conductor is taken into account, which increases effective inductance of the coil and changes effective permittivity of the transmitting structure. More important, this tool models properly also the transition between electrically thin and electrically thick conductors combining both of the coefficients.

## 2 High-Q Spiral Inductors

For the accurate design of the inductors, a software program was developed. From Fig 1,2&Table 1& 1.1 The design flow is divided into three steps and is described below. First, the layout (readable by a standard chip layout tool) is created for a given inductance. Line width, spacing and thickness as well as the distance to maximally two ground planes (if available) are taken into account. An N polygonal shape (usually square or octagonal) and the orientation and length of the connecting wires have to be specified. Based on this information, the design program generates vertex coordinates for a Q-value optimized inductor layout based on static inductance calculations. The inductance calculations are performed by the program MUTUAL [2]. Using a greLiont method, the vertices are varied until the calculated inductance matches the target inductance.

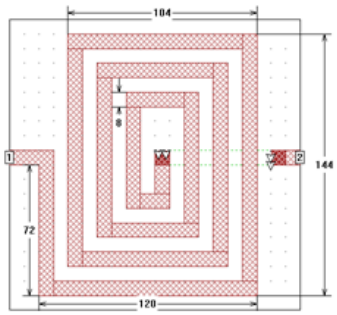


fig 1 Rectangular Spiral Unductor

Th is is usually accomplished in 5 to 7 steps which take only seconds of computation time for a typical 10nH inductor on a standard PC. The second step is to generate a lumped element model where each half turn of the spiral is represented by a single line

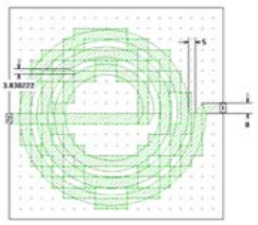

fig 2

model. Coupling capacitances and mutual inductances are included. In this model the complete geometry and technology information is taken into account. For consideration of the skin effect, the series resistance is modeled with frequency dependence.

The model is also used to investigate dependencies of the Q-factor and the high frequency behavior on parameter the third step is to fit this up to frequencies close to the first resonant frequency model using a simple circuit model. This model, together with the layout data can then be used as a library model for a circuit design tool. The self inductances Li and the mutual inductances Mik of the different Numbers of turns in the equivalent circuit are determined by MUTUAL [2]. For parallel lines an exact formula is used and for a finite angle between two segments a numerical integration is performed under quasistatic conditions [2]. The capacitance and resistance values are taken from published formulas (see e.g. [3]) and EM Comparison of the forward transmission parameter S21 obtained from an on-wafer two port measurement of a1nH to 40nh rectangular & Round Spiral inductor with the different turn multi-element lumped element model and the simple first order model. Good agreement is typically found. Show the comparison of measurements of different spiral inductors different turns multi element lumped element model. Especially the, big" model meets the measurements very accurately.

**Geometry**

| | |
|---|---|
| Box Size | 160 by 160 microns (276 microns high) |
| Number of Dielectrics | 3 (2 metalization levels) |
| Metals Used | Copper: Cnd= 5.8e7 T= 2 CR= 0<br>Metal2: Cnd= INF T= 0.2 CR= 0 |
| Top of box | Copper |
| Bottom of box | Copper |
| Number of Polygons | 17 (all staircase) |

### 2.1 Results (Inductors)

The fabricated inductors use two metal layers (except in the area of the underpass for the center connection). This doubles the effective line thickness and thereby decreases the line loss. The technology used for the fabrication of the samples is described.

**Dielectric layer Table**

| Material Name | Gallium Arsenide | Silicon | Aluminum |
|---|---|---|---|
| Thickness (microns | 250 | 1 | 25 |
| Erel | 12.9 | 11.9 | 9.8 |
| Dielectric Loss Tan | 0.006 | 0.004 | 0 |
| Diel Cond | 0 | 4.4e-7 | 0 |
| Mrel | 1 | 1 | 1 |
| Magnetic Loss Tan | 0 | 0 | 0 |

The Q values are higher than previously published values for spiral thin-film inductors on silicon due to a number of reasons: the high resistively substrate and the relatively high line thickness lower the resistive losses; the coil consequently uses both metal layers. The connection is made through a via

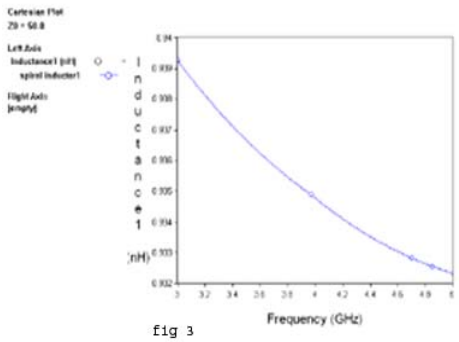


fig 3

over the whole length of the spiral (except for the underpass for the center connection), the geometries are optimized for maximum Q values. The shape should be of high symmetry and the ratio of the inner to outer radius should be approximately 0.43 for a circular coil [4], 0 the inductors are larger than

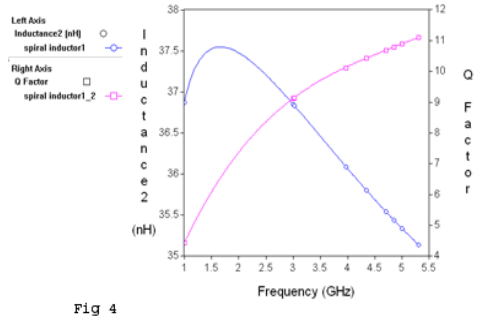


Fig 4

the previously published structures (The coils are located on a MCM substrate with significantly less space constraints than on a chip.) This widens conductor widths and further reduces losses. The maximum size is chosen such that the frequency of maximum Q value falls within the frequency range of the target application (Increasing the size of the inductor increases parasitic capacitances and lowers f-Qmax. The 37nH inductor has maximum Q around 5 GHz),0 the maximum size is chosen such that ground planes (if available) and height tolerances in assembly only have negligible influence on the inductance value (less than -5%). To satisfy this condition, the diameter of the coil should not exceed the distance to the nearest ground plane [4]. From Fig 3.4

## 3 Capacitor

Different types of capacitors are possible in MCM-D technology. First we have metal-insulator metal (MIM) capacitors, which are simply two parallel metal plates on top of each other with dielectric in between. In the classical configuration for MCM-D technology the bottom plate is connected to the circuitry above through vias. This inherently creates an asymmetric structure [5]. The use of photo-BCB, which has a good planarization and thickness tolerance per layer, allows the realization of precise capacitors. Another type of capacitor is the well known interdigital capacitor. This capacitor type is put on a single layer and is very sensitive to small changes in the gap spacing. The multi-layer MCM-D technology offers an alternative way of producing the capacitance value of the interdigital capacitor. This is a floating patch type capacitor based on a coplanar structure [II] with the central conductor in the top metal layer interrupted (gap) and capacitively coupled by means of a floating metal patch on the lower metal layer. In order to obtain the same capacitance value as with the interdigital or MIM type, a single overlap area must produce a capacitance which is twice as big. The basic geometries of the all capacitor types, mentioned above, are shown on Fig.6 together With the parameter list of some selected elements in Table2.

The minimum space between metal areas which guaranties high production yield is set to 2~ in this technology. This means that the design of the high quality interdigital capacitors with a high ratio of the intrinsic floating capacitance to capacitances to ground is not possible. By the use of floating patch capacitors instead of interdigital ones, one can benefit from larger capacitance value per area and, more important, reduced (by one order of magnitude) parasitic Capacitances to ground. These in turn can be further reduced with the MIM capacitors as they use 4 times less area for a specific intrinsic capacitance value in comparison to the

floating patch ones. However for a small capacitance value the implementation based on using of MIM can be difficult because of troubles in capacitance value prediction. These troubles are caused by the size dependent planarization effects.
Additionally, the influence of a via connection in the MIM configuration can decrease the resonant frequency in comparison with the floating patch configuration assuming the same distance to ground in both cases. The extracted equivalent element values of the MIM and interdigital capacitor model, shown on Fig.5, are collected in Table 2.

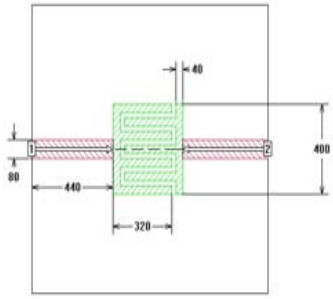


fig 6
integdig.Cap

The equivalent circuit of the floating patch configuration is a modified symmetric version of the model with additional capacitive element in-between representing parasitic gap coupling in the top strip and floating patch coupling to ground plane. It can be found in [5].

**Table: 2**

| Parameter R | cO2 | c06 | c09 | dO |
|---|---|---|---|---|
| c1 [pF] | 0.028 | 0.031 | 0.0992 | 0.0936 |
| c2 [pF] | 0.087 | 0.137 | 0.0924 | 0.0889 |
| c3 [pF] | 1. 069 | 3.332 | 0.1803 | 0.1819 |
| L [nH] | 0.93 | 0.52 | -0.8 | -1.0 |
| Cres [GHz] | 5.93 | 4.33 | -18.0 | -15.0 |

# 4 Conclusion

The inductors presented here are useful for on-silicon filters, RF resonators, inductive peaking and impedance matching. Investigations on the applicability of the inductors for fully integrated passive LC filters and results on sample low pass, high pass and band pass filters will be published elsewhere. The main passive components such as high quality spiral inductors and different type capacitors suitable for the MCM-D realization have been presented and discussed.

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