# Design and Fabrication of High-Q Spiral Inductors Using MEMS Technology

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*Abstract:* - This paper presents the design and modeling, fabrication and characterization of suspended spiral inductors on silicon substrate. The substrate materials underneath the inductor coil are removed by micromachining process to reduce the substrate loss which enables high frequency operation. A complete Library of spiral inductors with different line width, line spacing and number of turns have been designed and simulated. The results show that the *Q* factor as well as the self resonance frequency  $f_{srf}$  is greatly improved by removing the silicon underneath the inductor. The spiral inductors have a peak Q-factor of 35, and the maximum resonance frequency of the inductors is about 16 GHz. Fabrication of 2.5 turns inductor using MEMS technology is carried out. Measurements and characterization results are presented in this work.

Key-Words: - Spiral inductor, MEMS technology, High Q-factor, RF applications.

#### **1** Introduction

Recently, with the rapid growth of the demands in wireless communication products such as mobile phones and wireless network, low cost and high performance onchip radio-frequency devices are strongly needed. One important limitation in achieving higher levels of integration and further reduction of fabrication costs in the front-end of microwave transceivers is set by the difficulty of achieving high-Q on-chip inductors [1]. Usually, the planar spiral inductors are integrated on the low-cost standard (low resistivity) silicon substrate using standard silicon technology and aluminum (Al) metal interconnects. These inductors exhibit poor Qfactor due to the severe substrate loss of the standard silicon substrate at microwave frequencies and the ohmic loss of the aluminum thin-film. As a result, novel low-cost technologies need to be introduced for fabricating silicon-based high-Q inductors for the highperformance single-chip RFICs. While the ohmic loss can be reduced by using high-conductivity metals such as Copper (Cu) [2] or gold [3], the reduction of the substrate loss remains the major obstacle for highperformance silicon-based inductors. To overcome the substrate loss. several approaches have been implemented with improved O-factor. Ground-shielded inductors have been devised to reduce the substrate loss and noise coupling [4] with limited improvement in Qfactor (up to ten). Suspended inductors with the inductor

metal separated from the lossy silicon substrate have offered Q factor as high as 50 at 7 GHz [5]. Another approach to reduce the substrate coupling is to insert a low-loss low-K dielectric layer between the inductor metal and the lossy silicon substrate [6]-[8]. Recently, the use of silicon micromachining techniques to remove the substrate underneath the planar inductors has significantly increased both the inductor self-resonant frequency  $f_{srf}$  and quality factor Q [9]-[12].

In this paper, a complete library of spiral inductors on silicon substrate is designed and modeled. Also fabrication of one of these designed inductors is done using MEMS technology. Post processing step is utilized to remove the silicon underneath the inductor using micromachining technique. Great improvements in the Q-factor and resonance frequency have been achieved by etching away the silicon underneath the spiral inductor. The HFSS 3D electromagnetic simulation results are presented. Measurements and characterizations of the fabricated inductor is performed and presented in the paper.

## 2 Inductor Design and Model

Various rectangular spiral inductors have been designed using Greenhouse's method [9] and simulated using HFSS, a 3D electromagnetic simulator. The spiral inductors have a 2  $\mu$ m aluminum line thickness and 150  $\mu$ m inner diameter. Table 1 lists the number of turns, line spacing, and line width for these different spirals.

	N	S	W	Di
Device	number	line	line	Inner
Number	of turns	spacing	width	Diameter
		(µm )	(µm)	(µm)
1	3.5	5	10	155
2	3.5	5	20	155
3	3.5	5	30	155
4	3.5	5	20	155
5	3.5	10	20	155
6	3.5	15	20	155
7	3.5	25	20	155
8	2.5	5	20	155
9	3.5	5	20	155
10	6.5	5	20	155
11	3.5	5	20	90
12	3.5	5	20	155
13	3.5	5	20	180

Table 1 Spirals different geometries.

The S-parameters which are calculated using HFSS are transformed into the Y-parameters from which the inductance L and Q factor can be calculated based on the following equations [13], respectively:

 $L = \text{Im}(1/Y)/2\pi f$  (1) Q = Im(1/Y)/Re(1/Y) (2)

Where: Y are the Y-parameters and f is the signal frequency.

## 3. Simulation Results

There exists a trade-off between the inductance and quality factor when increasing the number of turns of a spiral inductor. Figure 1 a and b shows the variation of inductance L and quality factor Q due to the change in the number of turns for three spiral inductors of the same dimensions. It can be seen from the figure that, when the number of turns varies from 2.5 to 6.5, the inductance increases while Q and self resonance frequency *SRF* decrease. Increasing the number of turns will increase the inductor length l. This results in increasing the self inductance. Moreover, the positive mutual coupling between the inductor turns will be increased as well. Both effects will cause the inductance to increase as the number of turns increases. The Q will be reduced due to increasing the series resistance, Rs. The increase in Rs

is due to increasing the inductor length. Second, the induced eddy currents in the inductor segments will increase as a result of increasing the number of turns. As the area of the inductor increases due to increasing the number of turns, the overlap capacitance  $C_s$  and the capacitance in the oxide layer  $C_{ox}$  are increased. As a result, the SRF will be reduced. Figure 2 shows the variation of inductance and Q for the simulated inductor groups as the line spacing increases. It can be seen from figure 2 a and b that, increasing the line spacing from 5 um to 25mu has a week effect on the total inductance and Q. The SRF is kept constant as the line spacing varies. The main reason behind this is the small range which has been investigated for the line spacing. However, this range of line spacing is the practical range which is usually used in practical spiral inductors. The spiral size is usually limited by the chip area, which in turns prohibits the spiral line spacing to be greater than 25 um.



Fig. 1a Inductance variations with different No of turns



Fig. 1b Quality factor variations with different No of turns



Fig. 2a Inductance Variations with different line spacing



Fig. 2b Quality factor variations with different line spacing

Figure 3 illustrates the effect of the line width on Q for inductors with the same inductance but different line width. Three spiral inductors are designed with line width equal to 10, 20, and 30 µm. Inductors with wider lines have smaller series resistance  $R_s$ , which is inversely proportional to the width of the strip. However, they also have more shunt substrate parasitics because they occupy larger area. At low frequencies, the larger inductors offer higher Q because of lower series resistance  $R_s$ . At high frequencies, the substrate effects as well as the proximity effects dominate and the smaller inductors actually achieve higher Q.

The variation in the wire cross-section dimensions has little effect on the inductance. Generally, wires with smaller cross-section have a slightly larger inductance because they generate more magnetic flux external to the wire.



Fig. 3a Inductance Variations with different line width



Fig. 3b Quality factor variations with different line width

Therefore, increasing the line width will slightly decrease the self inductance and also the mutual inductance for the spiral inductor. As the area of the inductor increases due to increasing the line width, the overlap capacitance  $C_s$ , and the capacitance in the oxide layer  $C_{ox}$  will increase. As a result, the *SRF* will be reduced.

Figure 4 illustrates L and Q, SRF as a function of frequency when inner dimensions are varied, while all other characteristics are kept constant. The conclusion drawn is that as the area occupied by the spiral inductor increases, the inductance value increases, while the value of Q and SRF decrease due to the reasons discussed previously.



Fig. 4a Inductance Variations with different inner diameter



Fig. 4b Quality factor variations with different inner diameter

#### 4. Fabrication

Realization of 2.5 turn suspended inductor is achieved using standard technology MOSIS, 0.8um and CMP as a third party for etching process of the fabricated chip.

Figure 4a shows the inductor's layout. Etching simulation has been performed, to insure the required etching time before doing the post processing step. TMAH has been used to etch the silicon under the inductor to release the suspended structure. Figure 4b shows a scanning electron microscope (SEM) microphotograph for the fabricated suspended inductor after performing the etching step.

#### 4 RF Measurement & Characterization

The two-port S-parameters of the fabricated inductor is measured using Network Analyzer and the SUSS-Micro-



(a)



(b)

Fig. 4 Fabrication of suspended inductor using standard technology

Tech coplanar ground-signal- ground probe in the frequency range of 0.1 to 10 GHz. The parasitic parallel capacitance and series contact resistance between the substrate and the contact pads of the inductor are deembedded using well-designed dummy patterns [14]. The de-embedded S-parameters are transformed into Y-parameters from which the inductance and Q factor of the inductors are calculated based on equation 1, 2 respectively. Figure 6 shows the measured results of the fabricated inductor with 2.5 turns. The results obtained from measurements are close to the results obtained from electromagnetic simulation as shown in figure 1a.



Fig. 6 The measured inductance of 2.5 turns inductor

## 5 Conclusion and Discussion

In this work a complete Library of spiral inductors with different line width, line spacing and number of turns have been designed and simulated. The performance of suspended spiral inductors on silicon substrate has been electromagnetic investigated using simulator. Fabrication of 2.5 spiral inductor is realized using MEMS Technology. The substrate material below the inductors is removed by wet etching process. The results show that the self resonant frequency  $f_{srf}$  and Q factor of the micromachined inductor increase with many factors as described in the designed inductors library. Also it is understood that significant inductor performance can be obtained with the proper selection of number of turns N, line width W and line spacing LS.

## References

[1] G.W. Dahlmann, E.M. Yeatman, P. Young, I.D. Robertson, S. Lucyszyn, Fabrication, RF characteristics and mechanical stability of self-assembled 3D microwave inductors, Sensors and Actuators A97-98 (2002) 215–220.

[2] H. Jiang, Y. J. La, Y. Wang, and N. Tien, "Electromagnetically shielded high-Q CMOScompatible copper inductors," in IEEE Int. Solid-State Circuits Tech. Dig., 2000, pp. 330–331.

[3] K. Kamogawa, K. Nishikawa, I. Toyoda, T. Tokumitsu, and M. Tanaka, "A novel high-Q and wide-frequency-range inductor using Si 3-D MMIC technology," IEEE Microwave Guided Wave Lett., vol. 9, pp. 16–18, Jan. 1999.

[4] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," IEEE J. Solid-State Circuits, vol. 33, pp. 743–752, May 1998.

[5] J.-B. Yoon, C.-H. Han, E. Yoon, and C.-K. Kim, "Monolithic high-Q overhang inductors fabricated on silicon and glass substrates," in IEDM Tech. Dig., 1999, pp. 753–756.

[6] J. Rogers, T. Liang, T. Smy, N. Tait, and G. Tarr, "A high Q on-chip Cu inductor post process for Si integrated circuits," in Proc. IEEE Int. Interconnect Technology Conf., 1999, pp. 239–241.

[7] S. Jenei et al., "High Q inductor add-on module in thick Cu/SILK<sup>™</sup> single damascene," in Proc. IEEE Int. Interconnect Technology Conf., 2001, pp. 107–109.

[8] P. Pieters, K. Vaesen, W. Diels, G. Carchon, S. Brebels, W. De Raedt, E. Beyne, and R. P. Mertens, "High-Q integrated spiral inductors for high performance wireless front-end systems," in IEEE Radio and Wireless Conf., Denver, CO, 2000, pp. 251–254.

[9] J. Y. C. Chang, A. A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2-\_m CMOS RF amplifier," IEEE Electron Device Lett., vol. 14, pp. 246–248, May 1993.

[10] C. Y. Chi and G. M. Rebeiz, "Planar microwave and millimeter wave lumped element and coupled line filters using micromachining techniques," IEEE Trans. Microwave Theory Tech., vol. 43, pp. 730–738,Apr. 1995.

[11] A. Rofougaran, J. Y. C. Chang, M. Rofougaran, and A. A. Abidi, "A 1 GHz CMOS RF front-end IC for a direct conversion wireless receiver," IEEE J. Solid-State Circuits, vol. 31, pp. 880–889, July 1996.

[12] J. M. López-Villegas, J. Samitier, J. Bausells, A. Merlos, C. Cané, and R. Knöche, "Study of integrated RF passive components performed using CMOS and Si micromachining technologies," J. Micromech. Microeng., vol. 7, pp. 162–164, 1997.

[13] I. J. Bahl, "High-performance inductors," IEEE Trans. Microwave Theory Tech., vol. 49,no. 4,pp. 654-664,Apr. 2001.

[14] T. E.Kolding, "Afour step method for deembedding gigahertz on-wafer CMOS measurements," IEEE Trans. Electron Devices, vol. 47, no. 4, pp. 734– 740, Apr. 2000.