A MEMS BASED 2.7V, 2.4GHZ LNA FOR BLUETOOTH™ APPLICATIONS

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Abstract: A CMOS LNA using MEMS Technology. Highlighting the "on-chip" inductors with quality factor used to replace previous off chip models. The operating frequency $f_o=2.4$GHz with power dissipation of 20mW and overall noise figure of less than 1dB. It achieves an input return loss $S_{11}=-37.7$dB. With a supply voltage of $V_{dd}=2.7V$ giving out $S_{21}=24.3$dB, $S_{12}= -40.7$dB, and $S_{22}=-30$dB. Cascode topology was used with an output buffer that dramatically reduces power dissipation while conserving the gain.

Keywords: LNA, MEMS Inductors, Bluetooth LNA, 2.4GHz LNA

1. Introduction

THE rapid evolution of wireless technology and manufacturing techniques resulted in tremendous amount of research and development that contributed a lot in today's modern world. The LNA is the first stage in the receiver chain as it directly follows the antenna. Due to its critical position in the reception path in the whole analog front end this specific block represents the majority of problems in the integration of the CMOS substrate. The quest for building new LNAs that have to cope with the technology advancements facing newer and more sophisticated chips that operate on higher frequencies and require much higher gain and performance became a necessity. MEMS technology offers high "Q", low power consumption and on chip elements such as Inductors, Capacitors, and moving parts such as micro motors and micro mirrors[1]. The twinning of both the CMOS and MEMS technologies in LNAs have lead to very impressive results that will be later discussed in this paper. A simplified 2.4GHz Bluetooth transceiver [1] is shown in fig(1).

2. Input Stage Analysis

The LNA is a very critical stage because it setups the sensitivity of the receiver thus it's critical that its input stage would achieve high gain and low noise while providing a well-defined real input impedance. That's why deep analysis and study should be exerted in this area to choose the best topology to be used that would fit the required design criteria. In the shown architecture the first amplification and down-ward conversions are the most critical to the system performance as they will affect the later stages. In a simple example that will give a better understanding of how critical the LNA is and how it works the $f_o=2.4$GHz will be used in the analysis of this circuit.

As seen from the figure 2(a) the Cascode stage with inductive degeneration has been commonly used in CMOS LNA implementation. In this topology the source degeneration inductor introduces a real part into the input
impedance seen to the gate this is used to match the amplifier to the source impedance $R_s$ (D. K. Shaeffer and T. H. Lee, 1997),

$$R_{in} = \frac{g_m}{C_{gs}} L_s$$  \hspace{1cm} (1)

where $g_m$ is the transconductance, $C_{gs}$ is the gate source capacitor, and $L_s$ is the source inductor at this point to achieve an input power match the $R_{in}$ and $R_s$ must be equal to avoid any power reflection of an already weak received signal. To compensate for the reactive part at our desired frequency of operation adjustments have to be made to the $\omega_b$ by the selection of gate and drain inductors $L_s$ and $L_g$ such that:

$$\omega_b = \frac{1}{\sqrt{(L_g + L_s) C_{gs}}}$$  \hspace{1cm} (2)

The NF optimization method of fixed power dissipation for short channel devices is used to estimate the optimum quality factor of the input circuit[2], where

$$Q_{opt,Rs} = |c| \left[ \frac{5\gamma}{\delta} \left( 1 + \frac{3}{|c|^2} \left( 1 + \frac{\delta}{5\gamma} \right) \right) \right] \approx 4.5$$  \hspace{1cm} (3)

where $\gamma$ and $\delta$ are the bias dependent coefficients of channel thermal noise and gate noise respectively, the ratio $\delta/\gamma$ is nearly 2. $c$ is the correlation coefficient between the drain noise and induced gate noise and equals 0.4 for microwave frequencies. Once $Q_{opt,Rs}$ has been determined, the optimum device width is given by

$$W_{opt} = \frac{3}{2\omega_b L_C R_s Q_{opt,Rs}}$$  \hspace{1cm} (4)

For $f_o=2.4\text{GHz}$, $R_s=50\text{ohm}$, The optimum width for the input transistor is nearly 370 $\mu\text{m}$.

3. Circuit Design

As shown in fig (3); The circuit consists of three parts; the first part is the current mirror used for setting up the DC bias point followed by an input matching network using an LC circuit where matching takes place by the tuning of both the $L_s$ and $L_g$ and parameters of the transistor. The second part is a the amplifying section formed of a two stage cascode architecture that represents the core of the LNA design. Here the drain of $M_2$ is tuned by 10nH on chip spiral inductor $L_d$. This inductor resonates with the total capacitance at the drain of $M_2$ including $C_{gr}$ of $M_3$. Output matching is achieved using buffer stage that was specially designed to counter the dramatic effects of reduced gain after the buffering.

The Size of the cascode transistor $M_2$ is the same as $M_1$ 370/0.35 $\mu\text{m}$ such that they can be laid out as a dual-gate transistor to minimize the parasitic capacitance of $M_1$, thus improving the noise figure. While the size of the biasing transistor $M_3$ is 37/0.35 $\mu\text{m}$ and that of the buffer transistor is 120/0.35 $\mu\text{m}$; such size of the buffer transistor assures 50 $\Omega$ output resistance.

4. Spiral Inductor Design

Generally the inductors obtained from standard Silicon process cannot provide high-Q factors Sufficient for high performance LNAs, and consequently a proper alternative was chosen; that is the air-suspended inductors from the substrate provided by RF MEMS techniques to reduce substrate coupling loss.

Integration of these RF-MEMS inductors can be achieved using the UV-LIGA process. Such process makes use of photo-definable resist such as SU-8, conventional optical lithography and electroplating technique. Once spin coated resists are spin-coated and pre-baked, the optical lithography process defines the polymeric mold structures with post–exposure backing step for electroplating process. Upon the completion of copper electroplating process, the same process can be repeated on top of each other to realize RF MEMS components. The removal of polymeric molds reveals air-suspension of RF MEMS devices. ( Youngkyun J., et al., (2004))

All of the inductors are designed using hollow inductors technique to reduce magnetically induced losses. All of the inductors have same width of 10 $\mu\text{m}$ and conductor spacing is 5 $\mu\text{m}$. (J. Craninckx and S. J. Steyaert, 1997).

$L_d$ is a 3 turn Square type inductor with outer side length of 470 $\mu\text{m}$ yielding Inductance of 10.1 nH, $L_g$ is a 2 turn Square type inductor with outer side length of 470 $\mu\text{m}$ giving an inductance of 5.3nH while $L_s$ is 1nH inductor formed of a single turn Square type inductor with outer side length of 200 $\mu\text{m}$.
5. **Simulation Results**

5.1 **S-parameters**

To verify the operation of the proposed LNA operating at 2.4 GHz simulations were carried out using cadence Orcad Simulator. These simulations were done using TSMC 0.35 µm CMOS technology parameters. The forward gain (S21) and input matching parameter (S11) simulation results are shown in Fig. 4 and Fig. 5. The tuned LNA achieves $S11=-37.7\,\text{dB}$ and $S21=24.3\,\text{dB}$. The reverse isolation ($S12$) is $-40.7\,\text{dB}$ and output matching parameter($S22$) is $-30\,\text{dB}$.

5.2 **Linearity and Noise Figure**

Using two tones of equal amplitudes at frequencies 2.4GHz and 2.41GHz , the third order intermodulation frequencies are $2f_1-f_2=2.39\,\text{GHz}$ and $2f_2-f_1=2.42\,\text{GHz}$. The IIP3 is -5dBm as obtained from Fig. 6.
The proposed LNA achieves less than 1.1 dB of Noise figure at the frequency of operation. The simulation results of the LNA noise figure is shown in fig.

Simulations of the inductors were made by SONNET simulator, these inductors are designed to have 50 μm air-suspension and to be fabricated using 10 μm thick copper layer. The quality factor simulations of such inductors are shown in fig. 8.
6 Conclusions

A 2.4 GHz for Bluetooth applications has been designed using suspended air-cored inductors that achieved an input return loss $S_{11}=-37.7\text{dB}$. With a supply voltage of $V_{dd}=2.7V$ giving out $S_{21}=24.3\text{dB}$, $S_{12}=-40.7\text{dB}$, and $S_{22}=-30\text{dB}$; Such results match well with the Bluetooth transceivers. A proper layout to such circuit will be posted soon for fabrication.

REFERENCES


