Efficient low-voltage low-power Converters for Self Powered Microsystems (SPMS) based on 0.13µm technology

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Abstract: - In Self Powered Microsystem –SPMS- architecture based on a Micro Power Generator there are two main electrical circuits: an AC/DC converter and a DC/DC converter, which converts the available energy in the environment to a suitable electrical form to use in electronic circuits. Three AC/DC rectifiers designed in 0.13µm technology are presented in this paper in the frame of low voltage and low power applications. Two of them are synchronous rectifiers and the last one is based on a typical PN junction. The features of each rectifier are verified by simulation in terms of conversion efficiency. Finally, to define the SPMS system, an application with the best synchronous rectifier and an inductorless DC/DC charge-pump regulator is presented.

Key-Words: - Rectifiers, Self Powered Microsystems –SPMS-, DC/DC converter, charge-pump regulator

1 Introduction

Emerging portable power and low-power applications such as cellular telephones, PDAs, GPS, sensors [1] and a variety of handheld electronic devices have gained popularity with the reduction of the size-weight and energy requirements of the electronic devices. These devices are powered by external chemical power batteries, i.e. the conventional bulky Li-Ion batteries, with short and finite amount of energy that can produce drawbacks in applications where the battery replacement may be difficult such as unattended sensors or autonomous applications. This inconvenient has intensified the focus of designers on developing new power supply alternatives such as Micro Power Generator –MPGs- which is ten times smaller than a battery. A MPG can scavenge energy from ambient like Solar/Ambient Light [2], Temperature Gradients, Human Power [3], Thermal energy, Air Flow and Mechanical Vibrations energy [4] and convert it into electrical energy. In [3], researchers examines three different MPGs that can be built in a shoe to generate electrical power while walking and is showed a nice self-powered application that broadcast a RFID digital signal.

New autonomous systems based on the SPMS where are mixed in a single SoC micro generators, power electronics, sensors and actuators, are developed thanks to the appearance of MPG, ultra capacitors and MEMS Fuel Cells.

Three different power conditioning circuits –PCC- [6] based on rectification to extract the maximum DC voltage from piezoelectric MPG ac voltage are explored in this paper. An unregulated ac low-voltage is generated by the MPG based on piezoelectric effect that uses mechanical vibrations as the ambient source. As a result, an electronic rectification circuit is needed due to the loads require regulated dc voltage. One analyzed circuit is based on a simple diode bridge rectification, and the other two are based on synchronous rectification –SR- to improve the power efficiency.

Suitable AC/DC converters presented in this paper are designed into the frame of LVLP technologies, like the hcmos9gp from ST of 0.13µm and 1.2 volts, for scavenging applications.

The reminder of this paper is organized in six sections. Section 2 presents the idea for a MPG and rectification and section 3 explains the used technology. In section 4, the different rectification methods are analyzed and commented while section 5 presents the results and discussions. Section 6 shows a possible application with a charge pump, as a DC/DC converter, defining the SPMS. Finally, section 7 summarizes this paper.

2 Background

As we said before, piezoelectric membranes generate an unregulated ac voltage, which means that only a micro generator can not be used to supply the loads to be applied at the SPMS because it requires generally a DC voltage. Therefore, self-powered devices based on piezoelectric MPG usually use a power scheme based on three parts, as is depicted in Fig. 1. The first stage is the piezoelectric micro generator which generates the main ac voltage supply. The second one is the rectifier stage that converts the input ac voltage into non-regulated dc voltage. This is the most important part because it must extract maximum
voltage from the piezoelectric and must deliver it without considerable losses to the next stage. One of the best techniques to achieve good extraction voltage efficiency is to use a SR. Finally, a regulated dc voltage can be achieved thanks to a DC/DC converter.

The basic principle is simple, when a mechanical vibration is applied on the piezoelectric MPG, it generates an ac voltage that is rectified by the second stage and converted into non-regulated dc voltage. Later, the third stage regulates the dc voltage and supplies it to the load.

3 Technology
A commercial 0.13µm technology from ST capable to work with both 1.2 and 3.3 volts has been used to design the circuits. This technology is mainly used to develop digital designs but it is also possible to integrate analog and mixed blocks in a design. The basic devices are the 1.2 and 3.3 volts Nmos and Pmos transistors which are available in High Speed – HS-, Ultra Low Leakage – ULL- and Low Leakage – LL-versions. The Low Leakage transistors has been selected to avoid unnecessary losses. Furthermore, the speed is not an important requirement for this application because of the piezoelectric micro generator works in a low frequency.

There are also available resistors, capacitors and diodes. Resistors are based on P+ diffusion, P+ Unsalicied Poly, N+ Salicied Poly or hipo Resistors. All capacitors are made in Poly/Nwell, whereas the diodes are based in both, N+ diffusion in Pwell or P+ diffusion in Nwell available in 3.3 and 1.8 volts and in HS, ULL and LL. The LL diodes have been selected to avoid leakage currents.

4 Rectifiers
In this section is described the different circuits used to rectify the ac voltage signal provided by the piezoelectric MPG. The characteristic of this MPG is beyond the scope of this paper. The simple model that we can take for it is a sinusoidal signal of 1.2Vpp @ 500Hz. Our objective is to obtain the maximum voltage range from this MPG to supply integrated units. All solutions showed here base its operation in the half wave rectification. The first rectification circuit presented is based on a diode operation. Later, another two solutions based on synchronous rectification –SR- are implemented to improve the deficiencies of the first one in terms of voltage range and efficiency. An analog library has been designed to have the SR. This library is based on: current source, bias circuits and a class AB operational amplifier (OPAMP).

4.1 Diode Rectification
This rectification method is based on the classical half-bridge diode rectification topology as is depicted on Fig. 2. Diode D1 rectifies only the positive part of the voltage wave supplied by MPG whereas the capacitor C0 is charged. On the other hand, diode D1 does not work during the negative period of the signal and the load discharges the accumulated voltage in capacitor C0.

Diode bridge rectification – both, half bridge and complete bridge rectification-, is unsuitable method for applications where the MPG generates a low voltage that is comparable with the diode forward voltage drop involving an enormous inefficient rectification. In the above situation – low-voltage MPG output-, and to avoid the diode drop voltage, synchronous rectification is an elegant solution to improve the power supply efficiency.

4.2 Analog Library
This library has been designed with basical elements to develop the synchronous rectifiers. The main components are: 1µA current source, biasing circuits and one class AB OPAMP. All devices are supplied by 1.2 volts.

All elements are depicted on Fig. 3. A self-biased current source (a) with a start-up system has been designed. To generate all the necessary reference voltages to drive the OPAMP, two different biasing circuits have been developed, one of them controls the Nmos transistors (b) and the other controls the Pmos transistors (c). Furthermore, a special biasing circuit to control the class AB output stage has been designed (d).

Finally, an output class AB operational amplifier (e) with Nmos differential input pair has been designed. In Table 1 we present its main characteristics and Fig. 4 shows the gain and phase frequency response.
Fig. 3. Analog Library Circuits.

(a) 1µA Current Source, (b) Pmos Bias Circuit, (c) Nmos Bias Circuit, (d) Class AB Bias Circuit and (e) Class AB Bias Circuit.

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (DC)</td>
<td>65 dB</td>
</tr>
<tr>
<td>Unit Frequency</td>
<td>145kHz</td>
</tr>
<tr>
<td>Offset Voltage</td>
<td>2.4mV</td>
</tr>
<tr>
<td>CMR</td>
<td>23mV @ 1.17V</td>
</tr>
<tr>
<td>CMRR</td>
<td>75 dB</td>
</tr>
<tr>
<td>PSRR +</td>
<td>62 dB</td>
</tr>
<tr>
<td>PSRR -</td>
<td>70 dB</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>0.05V/µs</td>
</tr>
<tr>
<td>Current Supply</td>
<td>11µA</td>
</tr>
<tr>
<td>Voltage Supply</td>
<td>Vdd=1.2V ; Vss=0V</td>
</tr>
<tr>
<td>Power Supply</td>
<td>13µW</td>
</tr>
</tbody>
</table>

Table 1. Main features of the OPAMP.

The source-drain voltage of the N-channel mosfet is sensed by the comparator. When the source voltage is positive with respect to its drain voltage, the Nmos transistor conducts. The transistor only conducts in this situation; therefore, it works in the third quadrant. The schematic is depicted in Fig. 5.a.

The solution to supply the amplifier has been a 1.2 volts external source. This solution has been selected due to its on-chip simplicity integration. This source can be an external battery, e.g. Watch battery, or connect the power terminals directly to a regulated current source. A key aspect for the future is to use the same MPG to supply this voltage in order to have a full autonomous System.

4.4 Boosted Synchronous Rectifier

This rectifier presents an interesting improvement regarding the previous SR. The topology of the boosted rectifier is mainly the same as the simple, but it incorporates a boost stage between the switch transistor and the comparator. This stage reduces the on-resistance and extends the linear range of the switch using a signal higher than the supply voltage to control the switch transistor gate [7]. A Boost SR topology is depicted in Fig. 5.b.

The boost stage is based on the Bootstrap circuit [7] depicted on Fig. 5.c. It turns the switch on and off using the signal Φ from the comparator. When Φ is low, the switch gate is grounded across transistors M7 and M10. Meanwhile, the battery capacitor C3 is charged to Vdd by M3 and M12. Switch and capacitor are isolated by transistors M8 and M9. During the on phase, Φ is high, device M8 is activated by M5 and the load flows from battery capacitor C3 to switch gate activating it and M9. Furthermore, transistor M9 helps the switch gate to keep the voltage S shifted to Vdd. Devices M1, M2, C1 and C2 are not necessaries for the circuit but ensure a unidirectional charge of C3 by M3.

4.3 Simple Synchronous Rectifier

As we said before, a significant output piezoelectric MPG voltage drop is caused by the diode forward-voltage involving an enormous inefficient rectification. An efficiency increase can be achieved using SR [6]. Its structure is based on a comparator and Nmos transistor.
5 Simulations and Results
In this section, all rectifier circuits described above have been simulated using a 10µF as output capacitor. A 500Hz sinusoidal wave with 1.2Vpp has been selected as a first approach of ideal piezoelectric micro generator that is being developed in our department. The external supply source for comparators is 1.2 volts.

<table>
<thead>
<tr>
<th>Rectification Methods</th>
<th>Diode</th>
<th>Simple SR</th>
<th>Boosted SR</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{rectified}}$</td>
<td>296mV</td>
<td>833mV</td>
<td>1.16mV</td>
</tr>
<tr>
<td>$P_{\text{rectified}}$</td>
<td>8.76µW</td>
<td>69µW</td>
<td>135µW</td>
</tr>
<tr>
<td>Efficiency $\mu$</td>
<td>97%</td>
<td>70%</td>
<td>97%</td>
</tr>
</tbody>
</table>

Table 2. Resume of the main characteristics of the analyzed rectifiers.

In Fig. 6 are depicted the simulation waveform for all rectifiers, top waveforms. The simulation shows that the diode rectification scheme (a) involves an enormous voltage droop due to diode forward voltage. Its conversion efficiency is small –24.6%– because of the rectified dc value is between 300mV. On the other hand, the schemes based on synchronous rectification increase considerably the rectified dc value, raising the conversion efficiency. Waveform (b) shows the output dc voltage value –833.5mV–, this value is obtained with a simple synchronous rectifier and (c) shows the output dc voltage value –1.16V–which is obtained with a boosted synchronous rectifier. As we can see, the maximum extracted voltage with both SR, simple and boost, are 282% and 393% higher, respectively, of that diode rectification.

Furthermore, Fig. 6 shows in detail the bootstrapped circuit operation, lower waveforms. This circuit takes the switch control signal from the comparator (d) and shifts this to Vdd (e).

Table 2 shows the main features for each rectification scheme. All values have been obtained at the same conditions: load capacitor of 10µF, load resistance of 10kΩ and sinusoidal voltage of 1.2Vpp and a frequency of 500Hz as input source.

6 The AC/DC and DC/DC system
As a first approach a simulation of the best SR and suitable DC/DC system has been developed –Fig. 9-. The DC/DC in based on a charge pump. Taking into account the low level of power and that one of the future key aspects for the final SPMS system to develop will be the total weight; an inductorless solution has been adopted. This charge pump is based on a Two-Phase architecture [8].
The Two-Phase Voltage Doubler (TPVD) behaviour is controlled by two non-overlapped clock periodic signals ($\Phi_0$ and $\Phi_1$) that define two sequences: the charging phase ($\Phi_0$ and $\Phi_1$) and the transfer phase ($\Phi_0$ and $\Phi_1$). During the charging phase the flying capacitor $Cf$ is charged up to $V_{in}$, during the transfer phase, part of the charge stored in the flying capacitor is transferred to the load capacitor $CL$ and $V_{out}$ value is increased due to this transfer charge process. In an ideal situation (with no loses in the switching transistors, no resistive load in the output voltage, with 100% of efficiency…) and after several clock commutations it can be verified that $V_{out} = 2V_{in}$. In the Fig. 7 is depicted the charging and transfer phase in a TPVD.

Then, for an input of 135µW we have obtained an output of 95µW for 90µA of load current, achieving an efficiency of 70% for the CP. The CP power conversion efficiency increase with the load current as is depicted in Fig 8. Finally, Fig. 10 shows the Charge Pump output voltage (b) when the input voltage is a rectified dc voltage from Boost SR (a).

7 Conclusions
A study of three different AC/DC integrated rectifiers for low voltage low power applications has been presented. The best option to design a SPMS system is the SR which is based on a boosted switch. This rectifier presents an efficiency of 96.6 % and it is able to deliver practically the full range of voltage coming from the micro-generator, which is modeled as sinusoidal voltage source of 1.2Vpp and a frequency of 500Hz.

The system based on this single model of the micro power generator and our rectifier has also been simulated with an integrated Charge Pump, which represents the full SPMS that will be developed, with a global efficiency around 70%. We have presented the simulation of the SR based on a boosted switch and the DC/DC regulator which is based on a charge pump presented in [8].

From the simulation we can notice how we can have a regulated DC voltage from the micro-power source but having the best voltage range thanks to the use of the presented SR. The average power available at the output is 100µW.
The rectifiers and the charge pump have been designed and implemented in the hcmos9gp technology and we are waiting for the IC to test, this is depicted in Fig. 11, to proceed with the test phase. In future designs we expect to increase the efficiency of the CP using an special architecture for the CP level-shifters. In order to reduce the ripple of the output voltage the design of two parallel CP working in opposite face will be investigated.

References:


