Roadmap to Nanoelectronics for Developing Countries: A Realistic Approach

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Abstract: - Nanotechnology has potential applications in fields such as energy, medicine, electronics, computing, security and materials. Therefore huge investments are being made by the developed countries in Nanoscience and Nanotechnology research. The question, how the developing countries should get the advantages of this new technology keeping in view their present state – is addressed in this paper. The concept of leapfrog/jumpstart is not going to work, as they are not aware of the challenges in the development of this developing technology and have not sufficient number of the trained manpower that even understands Microelectronics. The idea of setting up of fabless application specific integrated circuit (ASIC)/ Programmable Logic design industry is worth considering. This industry may grow in steps to a point where the acquisition of own FAB facility becomes affordable.

Key-Words: - Nanotechnology, Nanoelectronics, ASIC Design, FPGAs, PLDs, Digital Design

1 Introduction

National Nanotechnology Initiative1 established by the US Government as a federal R&D program established to coordinate the multiagency efforts in nanoscale science, engineering, and technology defines Nanotechnology as the understanding and control of matter at dimensions of roughly 1 to 100 nanometers, where unique phenomena enable novel applications. Encompassing nanoscale science, engineering and technology, nanotechnology involves imaging, measuring, modeling, and manipulating matter at this length scale.

At the nanoscale, the physical, chemical, and biological properties of materials differ in fundamental and valuable ways from the properties of individual atoms and molecules or bulk matter. Nanotechnology R&D is directed toward understanding and creating improved materials, devices, and systems that exploit these new properties.

Researchers in the field of nanotechnology are enthusiastic about its potential applications in fields such as energy, medicine, electronics, computing, security and materials. This enthusiasm is based on laboratory discoveries, many of which are already being translated into highly advantageous products.

This enthusiasm has caused the establishment of countless number of Nanotechnology centers all over the world. 11,700,000 sites are found when words “nanotechnology center” were input to Google search engine.

On the other side some analysts are more cautious about the potential of nanotechnology, noting that other technologies were over-promoted and, in fact, failed to do many of the things that proponents said they would. Some are concerned that attention to potential shortcomings to a new technology, such as nanotechnology, be addressed2.

Forgetting about their present strength, high costs required in the establishment of Nanotechnology research centers and the challenges in the development of any new technology some developing countries like Pakistan are doing huge investments in this field. This paper discusses in detail the state of affairs in Electronics manufacturing in such countries and proposes the strategy to acquire nanotechnology.

2 Moor’s Law and Nanoelectronics

The semiconductor industry has experienced a tremendous progress and the performance of ICs improved at a rate much higher than any other product. The minimum size on a transistor has reduced from 10 µ in 1971 to 45 nm in 2006. (CNET News.com – January 26, 2006, 10:15 GMT). The powerful prediction made by Intel3 co-founder Gordon E. Moore in 1965 that, the number of transistors on a chip doubles about every two years still holds true. Intel has shown it practically4 (Fig. 1).
Fig. 1: Intel Products showing Practical Implementation of Moore’s Law

It is encouraging and promises the future of Nanoelectronics era. The establishment of countless Nanotechnology centers and the enormous investment by the developed countries makes sense.

3 Point for Consideration by Developing Countries

Many of the developing countries just following the developed countries have started investing in the establishment of Nanotechnology centers. In this endeavor the cost involved, the requirement of manpower and complexity of the technology developed must be understood in true prospectus. The number of transistors on a chip is increasing while the size of individual transistors is decreasing at an exponential rate; but simultaneously cost of fabrication is also increasing exponentially. Fig. 2 shows this trend\(^7\).

In fact the cost of Fabrication facility so far impeded the growth of electronics industry in developing countries. How will they be able to afford more expensive nanometer technology? Further having no prior experience in this area, they need to develop their human resource so as to meet their requirement at an affordable cost. Nanoelectronics is a complex area not yet developed. Main challenges include: Materials by design, Functional nano structures, Thermal physics at the nano scale, Tools and methodologies for nano electronic design, Nano devices beyond silicon, Integration of nano devices (on the silicon platform) and Nano electronic fabrication. It is also not clear that what architectures will win? Competitors include: Scaled CMOS, Molecular Electronics, Single Electron Transistors, etc. Various logic styles, such as Boolean, Threshold and Multiple valued might also be used.

4 Application Specific Integrated Circuits (ASICs) and Programmable Devices

Integrated circuits are made on a thin circular wafer, with each wafer holding hundreds of dies. The transistors and wiring are made from many layers built on top of each other. The lower nearly half-a-dozen layers define the transistors (the logic) and the top half-dozen define the metal wires between the transistors (the interconnect). The standard ICs are mass-produced for general applications and include fully customized logic and interconnect layers. A microprocessor is an example of a standard IC.

In ASICs all of the logic cells are predesigned. Using predesigned cells from a cell library makes the job of the designer much easier. The interconnect layers may be customized or programmed in the foundry (alternate name for fabrication facility) or by the user in the field. Similarly intellectual property high-level design blocks can be developed using Hardware Descriptive Languages such as Verilog or VHDL as a design entry or purchased from suppliers. High Level design blocks are used in larger systems. These approaches save many man-years of development and debug time; and assure first time success. The short product-life-cycle, faster time-to-market and technology reuse are pushing the industry towards Application Specific Integrated Circuits (ASICs). The ASIC Design industry mainly needs ASIC Designers and the Electronics Design Automation (EDA) Tools. The designs are described in an HDL. EDA Tools verify the designs for the desired performance and map them onto the silicon. The design files generated by the EDA tools
are submitted to the foundry for the fabrication of the chip.

ASICs are of many types including mainly Cell based ASICs, Gate Array based ASICs and Programmable Logic Devices as shown in Fig.3.

Field Programmable devices are useful for prototyping and the verification of the designs and low volume products. Their further classification is also shown. The field programmable gate arrays (FPGAs) are available with varying complexities at such a low cost that they are used for prototyping. This design verification provides error free IC designs. FPGA programming using HDLs would be the starting point of any ASIC industry.

![Fig. 3: ASICs and Programmable Devices](image-url)

To give an idea of the market for programmable devices, the following extract from Xilinx website is reproduced. "Today the worldwide market for programmable logic devices is about $3.5 billion, according the market researcher Gartner/Dataquest. The market for fixed logic devices is about $12 billion. However, in recent years, sales of PLDs have outpaced those of fixed logic devices built with older gate array technology. And, high performance FPGAs are now beginning to take market share from fixed logic devices made with the more advanced standard cell technology.

According to the Semiconductor Industry Association, programmable logic is now one of the fastest growing segments of the semiconductor business, and for the last few years, sales for PLDs have increased at a greater pace than sales for the overall semiconductor industry.

Says EDN Magazine, a leading electronics design trade publication: "Programmable-logic devices are the fastest growing segment of the logic-device family for two fundamental reasons. Their ever-increasing logic gate count per device 'gathers up' functions that might otherwise spread over a number of discrete-logic and memory chips, improving end-system size, power consumption, performance, reliability, and cost. Equally important is the fact that in a matter of seconds or minutes you can configure and, in many cases, reconfigure these devices at your workstation or in the system-

assembly line. This capability provides powerful flexibility to react to last-minute design changes, to prototype ideas before implementation, and to meet time-to-market deadlines driven by both customer need and competitive pressures." (EDN, "Annual PLD Directory," August 17, 2000.)"

5 Suggested Strategy for Developing Countries

Developing countries should concentrate on the human resource development in the design of electronic circuits using EDA tools and Design entry languages. They should encourage universities to teach digital courses using facilities available under university support programs by different manufacturers like; Altera, Intel, Xilinx, etc. The project design and fabrication process is shown in Figure 4 (on the last page of this paper). The design entry is a hardware descriptive language (HDL) such as Verilog or VHDL. Electronic design automation (EDA) tools provide different types of simulations of the circuits described in HDL. After successful simulation results the synthesis phase starts. The netlist is generated. EDA tools are available to transform the description into masks that generate different layers in the silicon.

To establish ASIC industry a suitable team, having skills in HDLs, the use of EDA tools, the ASIC technology and the intended applications, is the first requirement. The countries interested in setting up this industry must invest in human resource development through the university programs. This investment is going to pay back in many bounds. In case the number of ASIC designers produced in a country is larger than those needed locally, they will get jobs in the international market. Therefore they will contribute to their national economies, while enhancing their expertise.

More jobs are available to ASIC Designers as compared to those available to VLSI Designers in the global market. Using Google search, about 1,70,000 web pages dealing ASIC design industry and Job opportunities were observed.

An industry with a minimum of funding may take a start with the Field Programmable Gate Arrays (FPGAs). FPGAs are widely used mainly as a prototyping platform for ASICs and for low volume products. Their EDA tools are relatively cheap (about US$2500 for a single machine) and big designs can be run on a simple PC. Work started in field programmable devices in mid Eighties and the price per gate reduced from 1 Cent to 0.01 Cent in ten years. The complexity of the circuit has reached
the order of hundred thousand gates per chip. For example, the XC4000X Series available from Xilinx, provides the features needed for densities up to 500,000 system gates. Today the designers are seeking system on a chip with memories, cores such as CPU's, DSP's and Controllers etc.

There is a strong resemblance between the tools for FPGAs and those for other types of ASICs. Both use same HDLs and have almost the same design flow. Therefore, with an experience of FPGAs implementation it is easy to switch to the area of ASICs. The collaboration with a university is very useful in the process of development. EDA tool manufacturers provide these tools to universities for educational purposes at a very low cost. For example, Altera, Cadence, and Synopsis all have university support programs. They provide tools virtually free. On the other hand, for an industry the simulator, such as ModelSim approximately costs US$ 10,000, and the synthesis tools, for example Design Compiler of Synopsis and Ambit of Cadence cost about a million US dollars each. These synthesis tools work on SUN platforms. These tools generate netlists. These netlists are used in the layout and floor planning on the chip and then the final fabrication. Layout and floor planning tools cost another few hundred thousands of dollars and the fabrication facility costs billions of dollars. Before the local availability of the facilities, companies are available to fabricate the chips from any stage in the design after simulation. The general suggestion is to concentrate on fabless industry.

The fabless ASIC company is a logical progression of the trend to outsourcing in the semiconductor business. Fabless ASIC companies should have an advantage over traditional ASIC companies because of the reduced capital burden of their business models. Compared to design houses, fabless ASIC companies win by being paid for both design support and chip delivery, overcoming the business scalability issue that dogs traditional design service companies.

4 Conclusion
To get the benefits of nanotechnology the start by the developing countries should be taken from development of the skilled team and the low cost programmable technologies. This experience will prepare them for the design of complex products and acquisition of ASIC technology. The acquisition of fabrication facility is the last step and depends upon the economics of the industry.

References: