DESIGN OF TRANSFORMER BASED CMOS ACTIVE INDUCTANCES

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Abstract: - In this paper the design of a transformer based CMOS active inductance to be used for the realization of fully integrated RF CMOS front ends is discussed. The circuit topology employed aims at taking the maximum advantage of the limited transconductance gain of MOS devices for compensating the losses of the integrated magnetic structures. In this way, even if a 0.35 $\mu$m technology has been employed, it has been possible to obtain an equivalent “almost ideal” inductance of 6 nH at a center frequency of 2.4 GHz. The circuit operates with a supply voltage of 3.3 V and drives less than 1 mA. Moreover, two control voltages can be used in order to tune the maximum quality factor of the inductance and to change in a relatively wide range the frequency at which it occurs.

Key-Words: - Active inductance, Integrated transformer, CMOS, Quality factor, RF, Circuit design

1 Introduction

Modern RF front ends to be used for mobile communication and wireless networking require a considerable amount of digital signal elaboration thus making the CMOS technology the mandatory choice if one has to design very low cost fully integrated front ends. In the last few years, progresses in the CMOS technology have made MOSFET with sufficient gain in the GHz frequency range available, and therefore the main obstacle toward the fully integration of RF systems is represented by the difficulties encountered in the integration of high quality inductors. Particularly in the case of CMOS processes, integrated passive inductors have typical values of Q that are too low for implementing several fundamental RF functions (for example highly selective filters) [1,2]. Although the quality factor can be improved by resorting to special fabrication steps[3,4], the additional processing cost and complication resulting from a modification in the process flow make such an approach quite unsatisfactory. For this reason, there is a strong interest in the possibility of realizing high quality inductances by employing active circuits. A few topologies of active inductors have been proposed in the literature, which can be classified into three main categories. A first approach is the one in which a bi-pole with a negative resistance behaviour is put in series to the inductor in order to compensate the losses and increase the resulting quality factor Q[8]. A third approach exploits the magnetic coupling between the spirals of an integrated transformer and a current amplification between primary and secondary introduced by an active device in order to obtain a purely inductive behaviour[9,10]. As a general rule, inductorless circuits result in a smaller occupied area with respect to transformer based ones. However, it is believed that by resorting to a transformer in which the magnetic coupling controlled by an active device acts in such a way as to increase the quality factor of an otherwise passive inductive structure, one can get better noise and linearity performances with respect to impedance transformation circuit such as those based on gyrators. In the case of bipolar technologies, transformer based circuits have allowed the design of LNAs with noise performances quite close to what would have been obtained in the case of passive, high quality inductors loads[11]. In this paper it will be discussed a new topology that can be used for the realization of high quality, transformer based, CMOS active inductances. The design guidelines will be discussed in detail and simulation results will be presented that confirm the validity of the followed approach. Open questions that need to be addressed in order to make the actual design feasible will be discussed as well.
2 Problem Formulation

In a previous work a new topology for the design of transformer based CMOS inductances was introduced that was proven to have significant advantages with respect to the one that would have been directly derived from the topology employed in the case of bipolar technologies \[12\]. Here the properties of the new topology will be discussed in detail in order to derive guidelines to be used in the design for a specific application. A simplified diagram of the new topology that has been developed for the realization of high quality active inductances is reported in Fig. 1.

![Fig.1: simplified circuit of the CMOS active inductor proposed](image)

The parasitic resistances in series with the coils of the transformer are not shown in the figure. These, however, are shown in the small signal equivalent circuit reported in Fig. 2.

![Fig.2: small-signal equivalent circuit of the CMOS active inductor](image)

In order to simplify the discussion the equivalent transconductance \((g_m)\) of the cascode stage will be assumed to be purely real. The coupled inductances \(L_1\) and \(L_2\) represent the transformer whereas the capacitance \(C_R\) can be realized by means of a MOS varicap and therefore its value can be changed in a given range by means of a proper control voltage. The equivalent impedance \(Z'_{IN}\) is the parallel of the impedance \(Z'_{IN}\) in Fig. 2 and of the input capacitance of the MOSFET \((C_{GS})\).

As long as it can be guaranteed a purely inductive \(Z'_{IN}\), whose inductance value is below that which would be resonant with \(C_{GS}\) at the design frequency, it will be still obtained a purely inductive \(Z_{IN}\).

Let us define the impedance \(Z_P\) as:

\[
Z_P(s) = \left( R_R + sL_R \right) \parallel \frac{1}{sC_R}
\]

It can be written:

\[
V_{in} = V_{GS} = (Z_P + R_1 + sL_1)\frac{1}{s} + sM_{GS}V_{GS}
\]

And therefore, in the frequency domain:

\[
Z_{IN} = \left( Z_P + R_1 + j\omega L_1 \right) = \frac{1}{1 + j\omega M_{GS}} = \frac{(Z_P + R_1 + j\omega L_1)(1 + j\omega M_{GS})}{1 + \omega^2 M^2 g_m^2}
\]

If now the numerator of Eq.3 is taken into consideration it may be observed that the term \((1 + j\omega M_{GS})\) acts in such a way as to increase the phase of \(Z'_{IN}\) and therefore it can allow to reach, at a given frequency, a phase quite close or even exactly equal to \(\pi/2\). Note, however, that as the frequency increases, depending on the behaviour of the other terms at the numerator in Eq. 3, it is possible to end up with a bipole whose phase is larger than \(\pi/2\), that is an equivalent impedance with a negative real part. This situation has to be avoided as negative equivalent resistances may lead to instability. Therefore, it may be stated that the requirements for an equivalent impedance to be regarded as an ideal inductance at a given angular frequency \(\omega_0\) are:

- The equivalent resistance \(R_{in}\) of the impedance \(Z'_{IN}\) has to be 0 at the design frequency \(\omega_0\).
- The equivalent resistance \(R_{in}\) has to be positive in a neighbourhood of \(\omega_0\). In other words, it can be accepted as a “good” equivalent of an inductance any impedance with positive imaginary part provided that the real part has a minimum (close or equal to 0) at the desired design frequency. The above conditions translate analytically to the following set of simultaneous equations:

\[
\begin{align*}
R_\omega(j\omega_0) &= 0 \\
\left. \frac{\partial R_\omega(j\omega)}{\partial \omega} \right|_{\omega=\omega_0} &= 0 
\end{align*}
\]

Solving the above problem in our case is not difficult in principle, but it may become tedious and complicated because of the several parameters that are involved in the design. In order to extract general indications on the actual possibility of designing an ideal inductor with the proposed topology, we may proceed as follows.
Let us start by rewriting the impedance $Z_p$ in the following form:

$$Z_p(s) = \frac{1 + Q_s s}{\omega_0 s} \cdot \frac{1}{\frac{1}{Q_s \omega_0} + \frac{1}{\omega_0}}$$

$$Q_s = \frac{\omega_0 L_p}{R_p}$$  \hspace{1cm} (5)

In order not to complicate too much the discussion, let us assume that in any case the inductances $L_1$ and $L_2$ is characterized by the very same quality factor, that is:

$$\frac{L_1}{R_1} = \frac{L_2}{R_2}$$  \hspace{1cm} (6)

Now let us define the following quantities:

$$r = \frac{R_1}{R_2}; \quad \alpha = \omega_0 M g_M; \quad x = \frac{\omega}{\omega_0} R_2; \quad x_D = \frac{\omega_D}{\omega_0 R_2}$$  \hspace{1cm} (7)

With the previous assumptions and position it can be written:

$$z_n(x) = \frac{Z_{\omega_0}}{R_2} = \frac{(1 + jQ_s x)(1 + j\alpha)}{1 + j\alpha x^2} \cdot \frac{[1 - x^2] + j x}{[1 - x^2] + j \frac{x}{Q_s}}$$  \hspace{1cm} (8)

Therefore, finding the conditions for obtaining a purely inductive impedance at a given design (angular) frequency $\omega_0$, is equivalent to solve the system:

$$\begin{align}
\Re[z_n(x)]\big|_{x=x_D} &= 0 \\
\frac{d}{d x}\Re[z_n(x)]\big|_{x=x_D} &= 0
\end{align}$$  \hspace{1cm} (9)

where the relevant design parameters are reduced to the quantities $Q_M$, $\alpha$ and $r$ only.

The system can be solved numerically for different sets of parameters and the results are summarized in the graphs in Fig. 3 where the positions

$$Q_D = x_D Q_M = \frac{\omega_D L_p}{R_2} \quad \text{and} \quad x_D \alpha = \omega_0 M g_M$$  \hspace{1cm} (10)

have been used.

As an example of the possible applications of the plots in Fig. 3, let us assume that the design frequency $f_D$ is 2.4 GHz ($\omega_0=2\pi f_D$). Let us also assume that is available an integrated inductance $L_p=2.6$ nH with a quality factor at the design frequency of 0.5 (these are realistic parameters as reported in the AMS C35 process design parameters).

Let us also assume that it can be designed a transformer with $L_1=L_2=L_R$ and $R_1,R_2=R_R$ and characterized by a coupling factor $k$ of 0.8 so that the mutual inductance can be assumed $M=2$ nH. In order to obtain a purely inductive equivalent impedance, from the plots in Fig. 3 we have:

$$\omega_0 M g_M = 0.33 \quad \text{and} \quad \alpha_0 R = \frac{\omega_D}{0.72}$$  \hspace{1cm} (11)

and therefore it must result:

$$g_M = 11 \text{ mA/V} \quad \text{and} \quad C_R = 880 \text{ fF}$$  \hspace{1cm} (12)

Once the nominal values of the parameters $g_m$ and $C_R$ are obtained by means of the simplified approach that has been described so far, the designer can select the MOS transistor widths and the size of the CMOS varicap to be used. It must be noted that both the bias voltage $V_R$ and the varicap control voltage can be used as parameters for the fine tuning of the circuit both at the advanced design level (when verifying the circuit by means of a circuit simulator) and also as a means for compensating process parameters variation or for changing the frequency at which a pure inductance is obtained once the circuit is built. This fact is important since it could provide the means for designing compensation systems for tracking temperature and process parameters and for allowing the design of programmable high quality inductances. Although the means by which such systems can be designed and realized have not been investigated yet, it is important to understand how each single control
voltage acts on the equivalent impedance parameters.

To better understand the role of the varactor (\(C_R\) in Fig.1), let’s assume it to be removed (that is \(C_R=0\)).

The expression of the impedance \(Z_{IN}'\) then becomes:

\[
Z_{IN}' = \frac{R_g + j\omega L_g + R_1 + j\omega L_1}{1 - j\omega M_{in}} \rightleftharpoons \frac{R_g + R_1 + j\omega(L_g + L_1)}{1 - j\omega M_{in}}
\]

(13)

By setting the values for the various parameters as in the example above, it is possible to plot the phase of the impedance \(Z_{IN}'\) as a function of the frequency as in Fig. 4 (case \(C_R=0\)).

The other curves in the figure are obtained by plotting the phase of the impedance \(Z_{IN}'\) for different values of the capacitance \(C_R\). As it is apparent from the figure, the role of the capacitance \(C_R\) is that of causing the phase to decrease above a certain frequency. If the correct value for \(C_R\) is used (\(C_R=900 \text{ fF}\) in the figure, quite close to the value in Eq. 12), one can obtain the desirable situation of the phase having a maximum exactly equal to \(\pi/2\). The angular frequency \(\omega_D\) shown in Fig. 4 is the one for which the real part of \(Z_{IN}'\) is equal to zero, i.e., \(\omega_D\) satisfies the equation:

\[
Q_D \omega_D M_{in} = 1 \quad ; \quad Q_D = \omega_D \frac{L_g + L_1}{R_g + R_1}
\]

(14)

It is interesting to note that the angular frequency of operation, \(\omega_D\), in the case in which the value of \(C_R\) is such as to have the maximum of the the phase exactly equal to \(\pi/2\), is quite close to (slightly higher than) the angular frequency \(\omega_D\) that can be calculated from Eq.(14). This situation presents itself for almost any reasonable combination of circuit parameters, and therefore it can be used for an heuristic but effective fast design procedure.

In fact, if we are willing to design an ideal inductance at a given angular frequency \(\omega_D\), we can start searching for the proper circuit parameters that allow to satisfy Eq. (14) for an angular frequency \(\omega_D\) slightly lower than \(\omega_D\). Note that higher values of \(g_m\) lead to lower value of \(\omega_D\). As the value of \(g_m\) can be varied in the actual circuit by changing the bias point of the cascode stage, the actual choice of \(\omega_D\) is not critical.

As a first order estimation one can try to obtain \(\omega_D \approx \omega_R\) assuming the lowest value of \(g_m\) which can be obtained out of the cascode stage without degrading too much its frequency performances. At this point one can estimate the required value for the capacitance \(C_R\) by observing that the design angular frequency has to be in any case quite close to 0.7 \(\omega_R\) (Fig. 3).

The capacitance value thus obtained can be used to select the characteristics of the varicap to be used for its implementation. From the above results it can also be concluded that it is the value of \(g_m\) and therefore of the control voltage \(V_R\), that has the most important influence on the operating angular frequency \(\omega_D\), while acting on the varicap control voltage allows to have the correct phase behaviour in the neighbourhood of the design frequency. These observations can be regarded as the starting point toward the design of possible active compensation circuits.

### 3 Simulation Results

The approach described above has been employed in order to verify the feasibility of designing a purely inductive impedance above 2 GHz using a low cost 0.35 \(\mu\)CMOS process by AMS with a supply of 3.3 V.

In order to further reduce the requirements for the transconductance value \((g_m)\) a stacked integrated transformer has been designed in which the value of \(M\) is increased by increasing the number of turns of the secondary coil \(L_2\). This can be done while maintaining the same occupied area by reducing the width of the metal path at the cost of an increased value of the parasitic resistance \(R_2\). This does not significantly impair the performances of the circuit as long as a sufficiently high value of the output impedance for the cascode stage is obtained. The designed transformer occupies an area of 270x270 \(\mu\)m\(^2\). The relevant transformer parameters have been obtained by proper electromagnetic simulation using the Microwave Office tools and by carefully reproducing the process stack and the characteristic electromagnetic parameters derived from the AMS 0.35 \(\mu\) process manual for each process layer. A 3D view of the simulated structure is reported in Fig. 5. Note that the vertical scale is not linear in order to evidence the stacked transformer structure.
Fig. 5: 3D view of the simulate transformer structure. All dimensions are in microns. The different layers are represented using different scales in order to evidence the structure of the stacked transformer.

The self resonating frequency of the primary and secondary inductances were above 8 GHz, while the lumped model parameters extracted from the results of electromagnetic simulation were:

\[ L_1 = 1.65 \text{nH} \quad R_1 = 7 \text{Q} \quad L_2 = 5 \text{nH} \quad R_2 = 50 \text{Q} \quad M = 2.1 \text{mH} \] (15)

By comparing the Z parameters obtained from the lumped simplified model and by means of direct electromagnetic simulation, it has been possible to verify that the simplified model provides a good representation of the transformer behaviour as far as our discussion is concerned. All the other devices, including the inductance \( L_R \) and the varicap \( C_R \), were available as part of the RF AMS 0.35 \( \mu \text{m} \) library. All the parameters were set at the values used in the previous example. In particular, the CMOS varicap has been chosen in such a way to obtain a central value for the capacitance of about 800 fF.

Fig. 6 summarizes the results obtained after adjusting the bias voltage \( V_R \) and the control voltage of the varicap in such a way as to approach the condition of ideal inductance at about 2.4 GHz. The value of the inductance results about 5.5 nH. In Fig 7 the different behaviour of Q which can be obtained by setting proper values for the two available control voltages is shown. It must be noted that the condition of quasi-ideal inductance can be reached in a significantly wide frequency range, from about 2.2 up to 2.8 GHz. In Table 1 all the relevant parameters are listed that correspond to the three situations reported in Fig. 7, that is the value of the inductance at the maximum Q, the supplied current, the values of the bias voltage \( V_R \) and of the varicap control voltage.

Note that as one end of the varicap control voltage is \( V_R \) itself, the reported values refer to the difference between \( V_R \) and the actual voltage applied to the other control terminal of the varicap.

This result is quite encouraging as it suggests that, by designing a proper control system, such a wide tuning range could be exploited in order to compensate for process and temperature variations. The possibility of designing such a control system, together with a detailed analysis of the deviation from the ideal behaviour as can be expected in the actual realization of the circuit does not appear to be an easy task at present, but further investigations are being currently performed that are expected to provide the correct design guidelines.

In order to estimate noise performances, it has been evaluated the PSD (Power Spectral Density) of the equivalent noise current source in parallel to the equivalent inductance. In the case of the maximum Q occurring at 2.2, 2.4 and 2.8 GHz, the PSD is about 11.5, 11.0 and 10.5 pA/\( \sqrt{\text{Hz}} \), respectively. Although it is difficult to compare noise results with others reported in the literature, because of differences in process parameters and in target parameters such as equivalent inductance, power
dissipation or supply voltage, these noise results are better than those reported in [6] where a differential gyrator is used, thus possibly justifying the larger employed area with potentially better noise performances.

<table>
<thead>
<tr>
<th>$f_{Q_{\text{max}}}$ (GHz)</th>
<th>L @ $f_{Q_{\text{max}}}$ (nH)</th>
<th>$V_R$ (mV)</th>
<th>$\Delta V$ (mV)</th>
<th>I$_{\text{bias}}$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2</td>
<td>5.46</td>
<td>670</td>
<td>300</td>
<td>0.570</td>
</tr>
<tr>
<td>2.4</td>
<td>5.48</td>
<td>700</td>
<td>0</td>
<td>0.900</td>
</tr>
<tr>
<td>2.8</td>
<td>5.71</td>
<td>750</td>
<td>-100</td>
<td>1.3</td>
</tr>
</tbody>
</table>

Linearity is another important issue in the case of active inductances. Using typical figures employed for the characterization of linearity in amplifiers is not feasible in the case of a bipolar. In order to get information about linearity, a periodic steady state simulation has been performed using a sinusoidal current source driving the inductance. An equivalent impedance $Z_{\text{PSS}}$ has been evaluated as the ratio between the voltage fundamental harmonic across the inductance and the input current for increasing amplitudes. The results obtained in the case of the maximum Q occurring at 2.4 GHz show that compression effects (1dB) occur above about 1 mA. 

4 Conclusion

In this paper the design issues for the realization of high quality transformer based active inductances in CMOS technology have been discussed. An original topology has been presented that, while considerably reducing the requirements in terms of gain, transition frequencies and power consumption with respect to other designs, provides for two control voltages that can be used in order to accurately tune the circuit during its actual operation.

A 0.35 μm CMOS technology has been used to demonstrate the validity of the proposed solution which allowed to reach the condition of zero series equivalent resistance (that is a virtually infinite Q) for an inductance value of 6 nH at 2.4 GHz by properly acting on the above mentioned control voltages.

By following the proposed approach, almost ideal inductances could be obtained at higher frequencies provided that up to date technologies are employed. So, in the future, fully integrated CMOS RF front ends, for single chip, low cost, WLAN interfaces in the 5-6 GHz frequency range, could be realized.

References:


