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A ZVS Cycloconverter based Series Active Filter

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Abstract:- A new zero voltage switching (ZVS) series active filter (SAF) is proposed. The circuit includes a phase shift based PWM full-bridge inverter. A cycloconverter is used to control the polarity of output voltage pulses of mentioned inverter. Combination of operation of inverter and cycloconverter results in a continuous compensation voltage. Using the proposed power circuit topology it is possible to ZVS of all of switches of SAF that results in reduction of switching stresses, power losses and electromagnetic interference. The other advantageous of proposed topology is considerable reduction of size, cost and power losses of isolating transformer that is due to high frequency energy transferring between inverter and cycloconverter. The mentioned SAF could compensate for voltage sag, voltage swell, voltage harmonics and asymmetric voltage quality problems by a smooth compensation voltage waveform. It can recover the absorbed energy from DC side of inverter during switching periods. The circuit can be uses in single-phase as well as three-phase circuits. The analytical analysis is presented and simulation results are used to verify the superiority of this structure compared with similar circuits.

Keywords- Series active filter, zero voltage switching

1 Introduction

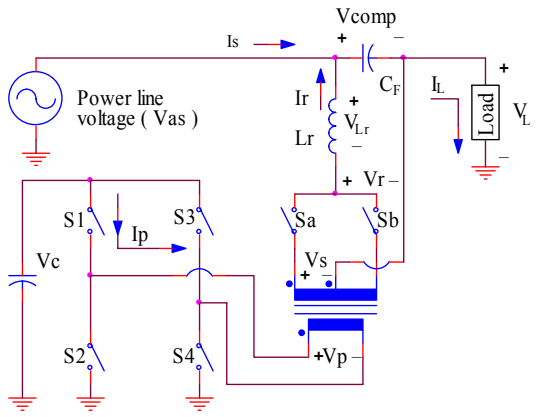
The term of Power Quality relates to a wide range of electromagnetic phenomenon in electric power system. It seems that this term, has been used in 1968 for the first time in a paper about the problems of utility voltage and its influence on electronic devices of United States Army [1]. In the same time in the Scandinavian countries and in Russia the term of Voltage Quality has been common [2]. The voltage quality is not a new subject. It seems that the first papers in this field have presented during 1969 and 1970 [2, 3]. Recently, the voltage quality has attracted a great deal of attention because of increasing of nonlinear loads, voltage sensitive loads, the possibility of monitoring and voltage quality compensation with power electronic systems such as series active filters (SAFs).

The common power circuit structure of SAF consists of a voltage source inverter that connects in series with utility usually by an isolating transformer. The SAF injects a compensation voltage in series with utility for voltage quality improvement of sensitive loads [4, 5]. Operation of SAF needs using self turn-off switches such as IGBT, GTO, etc. Commutation of these switches results in power loss, switching stresses, electromagnetic interference, etc. Many types of voltage source inverters with zero crossing modes are described to overcome these problems [6, 7].

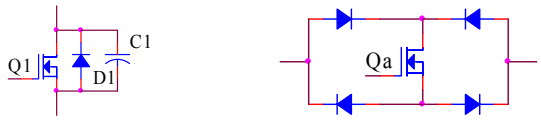
This paper proposes a new power circuit topology and control strategy for SAF with ZVS operation of all of its switches. It is possible using the proposed SAF for voltage quality improvement of medium and low power loads. Combination of a single-phase full-bridge inverter with a cycloconverter is used for charging or discharging an output capacitor that is in series with utility. It is interesting that the load current bypasses by switches and some inductances and it passes through the output capacitor. In any short time intervals of switching period, the voltage of capacitor increases or decreases smoothly for tracking of reference compensation voltage. There are twenty time intervals in each switching period to achieve ZVS of switches which could be controlled, easily. The power circuit topology, control strategy, principle of ZVS, phase shifting algorithm and simulation results besides of explanation of equivalent circuits in each switching time interval are described in following sections.

2 Power Circuit Topology

Fig. 1 shows the power circuit of proposed ZVS SAF. This circuit injects a series compensation voltage for canceling out the undesired voltage harmonics, voltage sag and swell. It should be



(a) Proposed power circuit topology for SAF



(b) Inverter switches (c) Cycloconverter switches

Fig. 1. Power Circuit of Proposed ZVS DVR

noticed that, it is possible using three number of proposed single-phase circuit topologies for voltage compensation in low and medium power three-phase loads. Input DC voltage V_C, is a constant voltage that could be supplied from a rectifier circuit from utility. There is a full bridge single-phase inverter with two legs containing S_1-S_2 and S_3-S_4 in primary side of isolating transformer (TR).

The width of bi-directional voltage pulses in primary side of isolating transformer V_p, is controlled by phase shifting strategy. In this well-known method, the gating pulses of S_3 and S_4 are phase lead in respect with gating pulses of S_1 and S_2. By controlling the phase shift angle, it is possible to control the width of pulses in primary side of TR. There is a cycloconverter circuit in secondary side of TR. This circuit consists of two bi-directional switches to achieve a bi-directional current flow possibility. This circuit can change the polarity of generated voltage pulses in secondary side of TR. In this way, the output voltage waveform of cycloconverter V_r, could be a PWM pulse train with any desired polarity. The frequency of energy transfer between inverter and cycloconverter is higher than power frequency and it reduces the size, cost and power losses in TR, considerably.

The voltage across output capacitor C_F, should follow the reference compensation voltage. The duration and polarity of output voltage of cycloconverter results in flow of charging or discharging current I_r, through C_F. Using L_r make it possible getting a smooth voltage variation through C_F. The output capacitor C_F is large enough to have a constant voltage during each switching intervals so, the current of inductor varies in almost linear form.

3 Determination of Reference Compensation Voltage of SAF

Fig. 2 shows a typical reference compensation voltage waveform that should be injected through output capacitor for voltage quality improvement of load. The control strategy for generation of this waveform is based on subdividing it into equal switching time periods, T_s. Each switching time period consists of twenty switching intervals by itself (T_0-T_{20}). These easy to control switching intervals, make it possible to achieve ZVS operation of all switches of SAF.

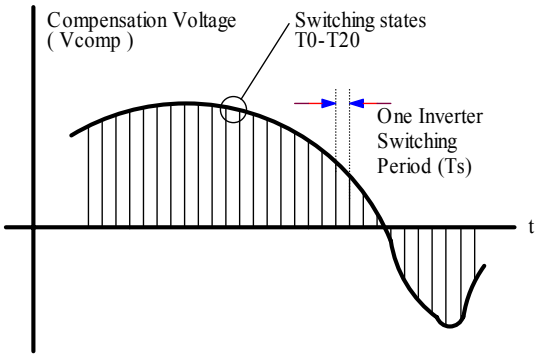


Fig. 2. A part of compensation voltage

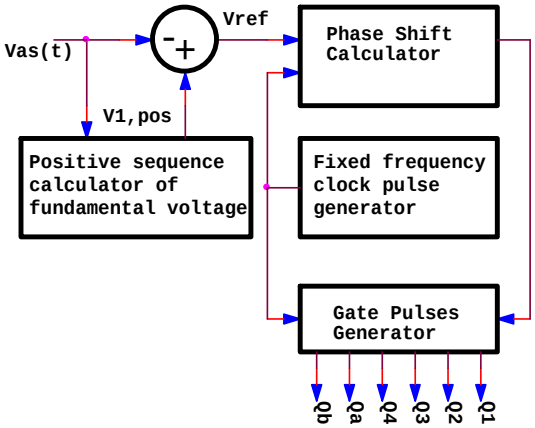


Fig. 3. Simplified control block diagram

Fig. 3 shows the control block diagram for generation of reference compensation voltage, v_{ref} and gating signals of switches. There is a control circuit for calculation of instantaneous positive sequence of fundamental frequency of utility

voltage, $v_{1,pos}$ [8, 9]. Subtraction of this voltage, from utility side voltage v_{as}, results in reference compensation voltage of SAF, v_{ref}. Obviously, it is possible using many other strategies for generation of reference compensation voltage and this subject is not the main purpose of this article.

Suitable gating signals of switches, results considering the switching diagrams of Fig. 4. This figure shows one of the switching periods in which the voltage across C_F rises because of a positive average charging/discharging current i_r. Fig. 4(a) to 4(d) and 4(e) to 4(h) show the gating signals and voltage across switches S_1 to S_4, respectively. These figures show that switching on of these switches is in ZVS mode. The ZVS of inverter switches is achieved using their stray capacitors and inductance of L_r. It is possible using auxiliary parallel capacitors with mentioned switches if it is necessary, too. Fig. 1(b) shows the inverter switches with their parallel stray (or auxiliary) capacitors in addition to an anti-parallel diode. Comparing Fig. 4(a) with 4(e) shows that S_1 is turned off at T_{12} and it is turn on in ZVS at T_{13}. It is easy to notice similar time intervals between the last switching off and beginning of gating pulses for all of mentioned switches, too. Gating signals of switches S_3 and S_4 are phase shifted compared with gating signals of switches S_1 and S_2. Gating signals of same switches on a leg is complement of each other. Fig. 4(i) shows the primary side voltage of TR that is a result of phase shift control operation. Operation of cycloconverter switches could result in changing the polarity of primary voltage of TR, to desired polarity. Fig. 4(j) shows the output voltage of cycloconverter v_r. The average voltage of cycloconverter v_r is given by eq. (1).

$$V_r \approx \frac{\alpha}{\pi} V_C \quad , \quad 0 \le \alpha \le \pi \tag{1}$$

The α, is the required phase shift value that is shown in Fig. 4(a). If V_{ref} be the desired compensation voltage, and $V_{1,pos}$ be the positive sequence of fundamental voltage of utility, then the reference voltage is obtained by (2):

$$v_{ref}(t) = v_{1,pos}(t) - v_{as}(t)` \tag{2}$$

For online restoration of load voltage it is necessary to have the following condition in which $v_{comp}(t)$ is the compensation voltage:

$$v_{comp}(t) = v_{ref}(t) \Rightarrow \alpha(t) = \frac{n_1}{n_2}\frac{\pi}{V_C}\left[v_{1,pos} - v_{as}(t)\right] \tag{3}$$

Fig. 4(i) shows a pulse width modulated voltage across primary side of TR by using phase shift control of inverter. The voltage on each secondary sides of TR is similar to its primary side by taking account the transformer turns ratio.

Fig. 4(j) shows the cycloconverter output voltage v_r, which in this figure has assumed to have an average positive value for increasing the output capacitor voltage. It should be noticed that, this voltage is same as voltage of secondary side of TR except its controllable polarity.

Fig. 4(k) to 4(n) shows gating pulses and voltages on switches S_a and S_b, respectively. This figures show a ZVS operation of mentioned switches, too. For example, S_a switches on at T_{15}, while voltage on it has reached zero at T_{12}.

Fig. 4(o) to 4(r) shows bi-directional currents of S_a, S_b, L_r and primary of TR. The current of L_r is the sum of currents of S_a and S_b and it controls the charging or discharging the capacitor C_F. By controlling of phase shift angle α, it is possible to control the pulse widths of v_r, that controls the amount of charging/discharging current of C_F. It is interesting to notice that, the circuit can recover the energy during the opposite polarity of v_r and i_r.

Fig. 5 shows the equivalent circuits in typical switching intervals between T_0 to T_4. This figure shows the important role of stray (or auxiliary) capacitors in commutation between S_1 and S_2 which are in same leg of inverter. During time interval T_0 to T_1, switches Q_1 and Q_4 are closed, so primary voltage v_p equals v_c and primary current i_p is positive. At $t = T_2$, switch Q_1 turns off and its current diverts to $C_1$and C_2, as shown in T_1 to T_2 interval. The i_p charges capacitor C_1 and discharges capacitor C_2 at the same rate because the sum of capacitor voltages C_1 and C_2 is equal to V_C. At $t = T_2$ the voltage across switch S_2 reaches to zero, so i_p starts flowing through D_2 and the commutation completes between S_1 and S_2. It is possible to explain the commutation between S_3 and S_4 in similar manner.

The gating pulses of S_a and S_b can be determined considering this fact that, if $v_{comp}(t)>0$ then the gating pulses of S_a and S_b are synchronize with gating pulses of S3 and S4, respectively (as is shown by comparison of Fig. 4(c) with 4(l) and 4(d) with 4(k)). If $v_{comp}(t)<0$ then the gating pulses of S_a and S_b are synchronize with gating pulses of S_4 and S_3, respectively. Eq.(4) shows the pairs of switches which their gating pulses are synchronize in each of two mentioned cases as follows:

$$\begin{cases} (S_3, S_b) \quad \& \quad (S_4, S_a) & for\ v_{comp} > 0 \\ (S_4, S_b) \quad \& \quad (S_3, S_a) & for\ v_{comp} < 0 \end{cases} \tag{4}$$

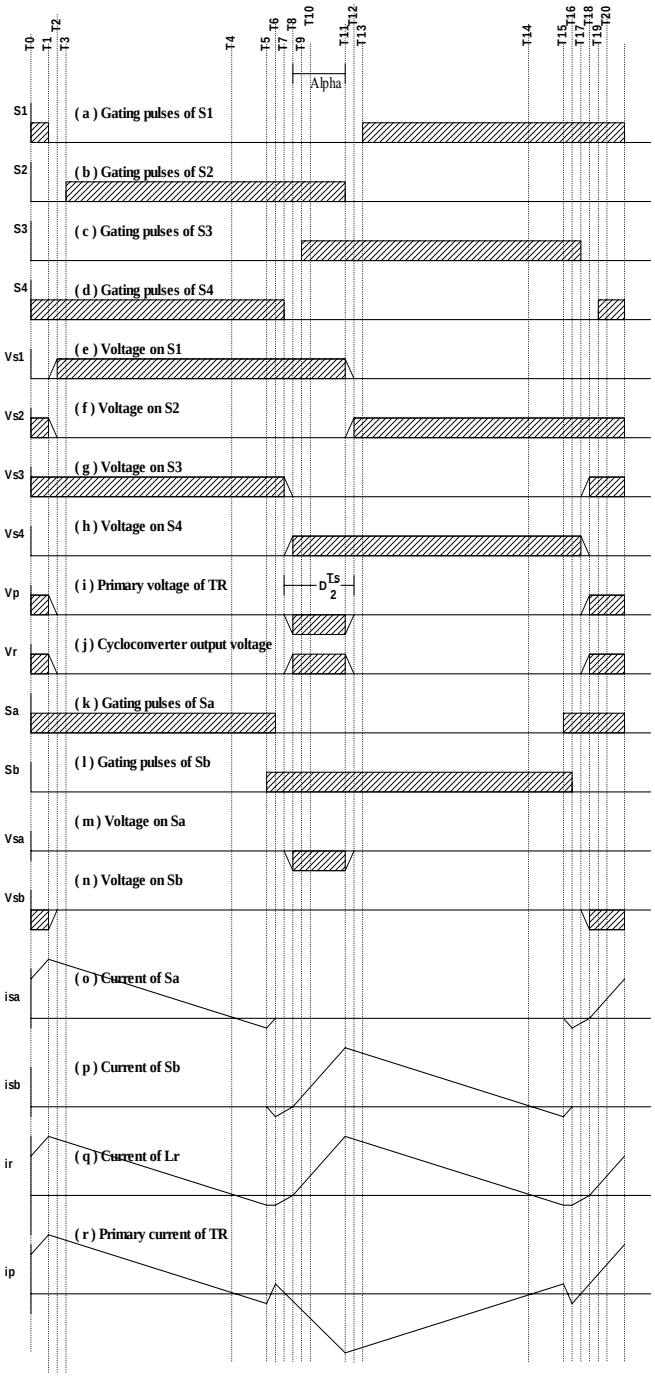


Fig. 4. Switching diagrams

4 Computation of L_r

As mentioned before, the overall ZVS operation of proposed circuit depends on stray capacitors of switches, the value of L_r and the source current i_s, that is equal with load current i_L. We have two operation modes in each switching period. Fig. 6 shows these two modes, their equivalent circuits and current waveform of L_r, during T_6 to T_{16} of Fig. 4(q).

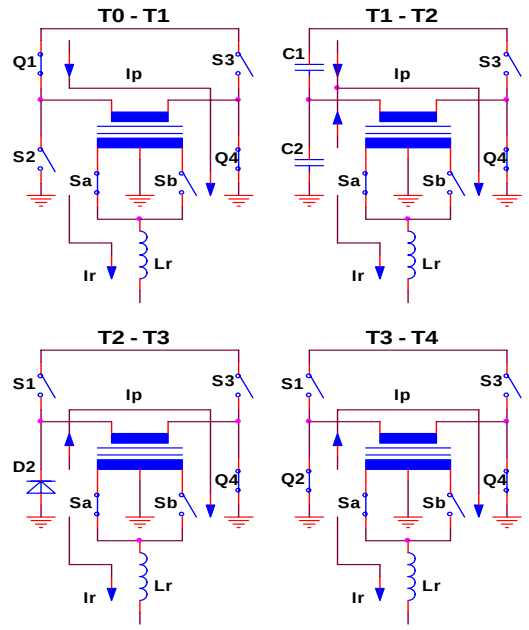


Fig. 5. Step by step of switching time diagram

There is two such current waveforms during each switching period.

Fig. 6(a) shows the equivalent circuit in first mode in which the voltage across secondary side of TR, v_r is not zero. This happens two times during a period of switching and it results in increasing of current of L_r if the average of cycloconverter output voltage would be positive (same as Fig. 4(j)). Obviously, if the average of cycloconverter output voltage be negative, this current will decreases during this mode. The time interval of this mode is equal with phase shift value α that is equal with $\frac{DT_s}{2}$ in which D is the duty ratio of voltage of cycloconverter output. Assuming constant supply current during switching period as i_s, it is possible to obtain the equations (5) to (8), during mode (I):

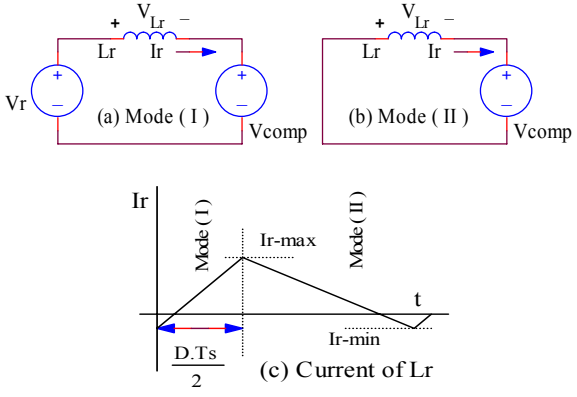


Fig. 6. Simplifies main modes of operations

$$L_r.\Delta i_r \approx v_{Lr}\Delta t \quad , \quad where: \quad v_{Lr} = v_s - v_{comp} \; ; \Delta t = D\frac{T_S}{2} \tag{5}$$

$$v_{comp} = D\frac{n_2}{n_1}V_C \; ; v_r = \frac{n_2}{n_1}V_C \tag{6}$$

$$\Delta i_r = \frac{1}{L_r}\left[D\frac{T_S}{2}\right]\left[\frac{n_2}{n_1}(1-D)V_C\right] \tag{7}$$

$$I_{r,max} = \frac{\Delta i_r}{2} - i_S \tag{8}$$

The energy stored in L_r, before commutation of S_1 or S_2 is very important because it should be more than the energy stored in their stray capacitors to guarantee their proper ZVS operation. The energy stored in L_r, just before turns off of S_1 or S_2 is achieved using following formula:

$$E(L_r+) = \frac{1}{2}L_r I^2_{r,max} \tag{9}$$

On the other hand, in second mode of operation that occurs when the voltage across secondary side of TR changes to zero the following equations can be obtained. This condition happens two times along each switching period.

$$v_{Lr} = -v_{comp} \; ; \Delta t = (1-D)\frac{T_S}{2} \tag{10}$$

$$I_{r,min} = \frac{\Delta i_r}{2} + i_S \tag{11}$$

Then the energy stored in L_r, before S_3 or S_4 switch turns off could be obtained by eq. (12):

$$E(L_r-) = \frac{1}{2}L_r I^2_{r,min} \tag{12}$$

Indeed, as mentioned before, proper ZVS operation of inverter switches could achieve only if the energy stored in L_r, be more than the energy stored in stray capacitors of switches. So by energy equilibrium, the amount of L_r can be obtained by following equations:

$$E(C_1;C_2) = 2E(C_1) = C_1 V_c^2 \tag{13}$$

$$E(L_r-) > E(C_3;C_4) \quad , \quad also \quad E(L_r+) > E(C_1;C_2) \tag{14}$$

In these equations, C_1, C_2, C_3 and C_4 are the stray capacitors of switches S_1, S_2, S_3 and S_4, respectively. By assuming $I_{r,min} < I_{r,max}$, the following condition achieves to determine L_r :

$$L_r > \frac{C_1 V_c^2}{I^2_{r,min}} \tag{15}$$

5 Simulation results

Simulation power circuit is similar to Fig. 1. Simulations of circuit are performed by PSCAD/EMTDC software with following values:

Inverter switching frequency = 5 KHz
V_C = 300 [V]
n_2/n_1 = 0.3
$C_1 \ldots C_4$=100 [pF]
Load power = P_L 400 [W]
Load power factor = 0.8 (inductive load).
L_r = 100[uH]
C_F=33 [uF]
$v_s(t)$= 220 *Sin*(314t) [rms, normal case]

Fig. 7 shows the utility side and compensated load side voltages. The source side voltage has changed during the following four stages:

1) Normal case 0<t<60
2) Voltage Sag 60<t<120
3) Voltage Swell 120<t<180
4) Voltage harmonics 180<t<240 (ms)

In normal case, the utility voltage is assumed to be a sinusoidal waveform with power frequency. In this stage, the SAF has no effect on circuit operation because the switches S_2 and S_4 are close and the primary side of TR is short circuited. The S_1 and S_2 are open and S_a (or S_b) is closed to bypass the output capacitor C_F. In this case, load current passes through L_r that its reactance is very small and there is almost no voltage drop across it.

In voltage sag condition, the utility side voltage has decreased to 180 (v, rms). The simulation results show very fast dynamic response and it has resulted to regulation of load side voltage magnitude.

In voltage swell condition, the utility side voltage has increased to 260 (v, rms). The operation of SAF has resulted in regulation of load side voltage with considerable dynamic response.

In utility voltage harmonic polluted case, a 250 Hz, harmonic with 40 (v, rms) is added to the utility voltage. The SAF has acceptable performance in compensation for utility voltage harmonics. The total harmonic distortion in utility side and load side has been 12.9% and 3.28%, respectively.

Fig. 8 shows the reference and actual compensation voltages across output capacitor, C_F. This figure shows that the proposed power circuit topology and control strategy has resulted in very good tracking performance of reference voltage using the proposed SAF.

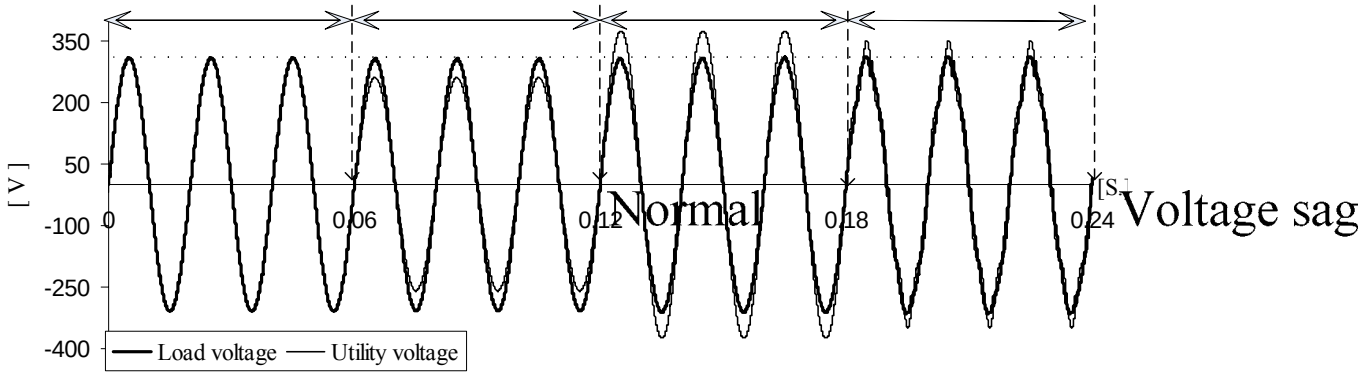


Fig. 7 Utility side and compensated load side voltageS

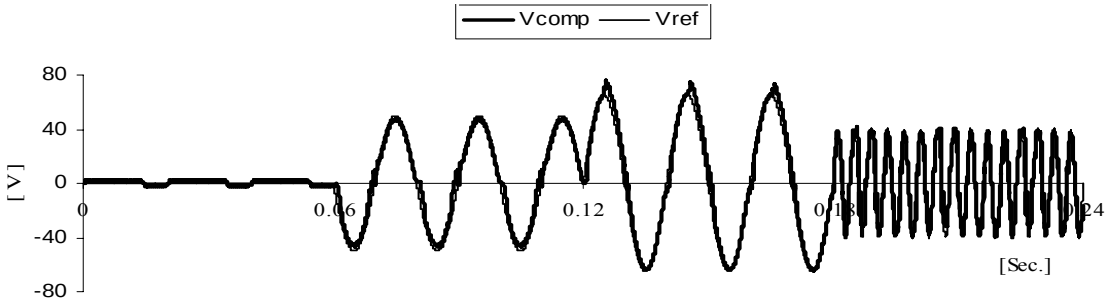


Fig. 8. Reference and actual compensation voltages

6 Conclusion

A new power circuit topology and control strategy for series active filters is proposed. Using the proposed SAF, it is possible to achieve the ZVS operation of all of the switches of SAF. The series compensation voltage of SAF is a continuous voltage waveform and it can compensate for different voltage quality problems such as voltage sag, voltage swell and voltage harmonics, successfully. The isolating transformer operates in high frequency that leads to its cost, volume and losses reduction. The different modes of switches operation in each of switching periods are presented and analyzed in detail. The gating signals and equivalent circuits in each of switching time intervals are presented. The simulation results show acceptable dynamic response and voltage quality improvement of sensitive loads.

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