

Nonuniform Sampling Delta Converters – Design Methodology

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Abstract: A new acoustic signal processing system, based on the non-uniform delta modulation method is presented in the paper. The main research milestones approach defining basic principles of converter is shortly described. In this issue the authors release a hardware example of their methodology and some difficulties occurred during its implementation. Finally, the new codec architecture addressed to System on Chip circuits is proposed.

Key-Words: Analog-digital conversion, Delta modulation, Adaptive systems, Variable-rate sampling

1 Introduction

Techniques for increase performance of data converters by signal processing has been in the research focus lately. Both university and industry try to develop methods that can provide the end user with a simple design, high error tolerance, greater compression and less power consumption codec at the low price. ADM (adaptive delta modulation) algorithms and their hardware implementation are suitable for these opposite requirements. Compression properties of DM systems are based on a rule that the A/D conversion is accomplished on the removed redundancy input process. The efficient samples decorrelation is usually made using the adaptation procedures [1, 2]. Step size adaptation is the simplest procedure. Uniform sampling ADM systems allow reaching an essential dynamic range of the constant SNR_{max} ratio; however the gained SNR_{max} value is not higher then in case of Linear Delta Modulation [1]. It results from uniform sampling that these methods do not utilize all compression possibilities involved within the ADM systems [3].

As seen from [3, 4] ADM systems with variable sampling frequency yield higher compression and SNR ratio than those with fixed frequency, especially at conversion of the highly non-stationary processes (i.e. speech and TV). The great advantage of the variable-rate delta modulations is high data-protection performance [4].

This paper is aimed at the study on the Non-uniform Sampling Delta Modulation (NSDM) codec design precondition and difficulties occurring during prototype building.

2 Principle of the NSDM technique

The NSDM schemes have been proposed and studied in [3, 5]. This modulation is a method adapting the sampling frequency to the input signal variation. The block diagram of its idea is presented in Fig. 1.

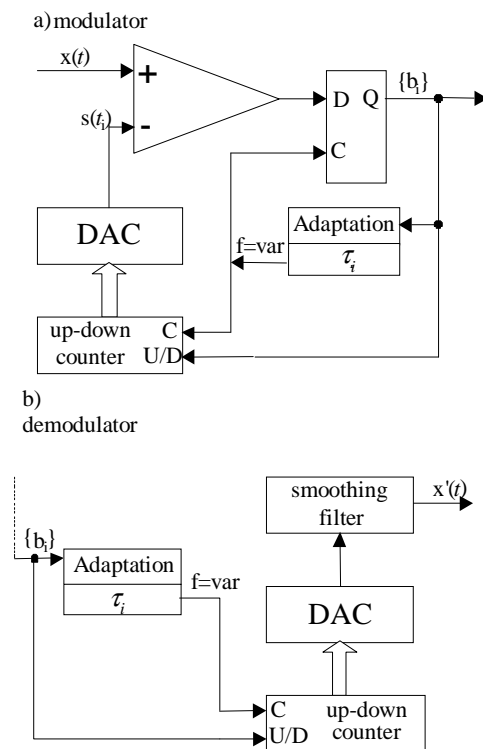


Fig. 1. Block diagram of NSDM converter

For the input signal $x(t)$ the staircase in the NSDM modulator can be expressed as in (1):

$$s(t_i) = s(t_0) + \sum_{n=1}^{i-1} \Delta d_n \quad (1)$$

where: $d_i = \text{sgn}[x(t_i) - s(t_i)]$

and the output code stream is as in the equation (2):

$$b_i = \begin{cases} 1 & \text{for } d_i = 1 \\ 0 & \text{for } d_i = -1 \end{cases} \quad (2)$$

Where: t_i is the sampling instant, and $s(t_i)$ is the coded signal $x(t)$, at t_i with the step size Δ . The sampling intervals $\tau_i = t_{i+1} - t_i$ vary according to the characteristics of $x(t)$ and the next sampling time t_{i+1} can be expressed as:

$$t_{i+1} = \tau_i + t_i \quad (3)$$

And sampling interval τ_s

$$\tau_s = \begin{cases} P \cdot \tau_{s-1} & \text{for } b_{i-2} = b_{i-1} = b_i \\ Q \cdot \tau_{s-1} & \text{for } b_{i-2} = b_i \neq b_{i-1} \\ \tau_0 & \text{for other } b_{i-2}, b_{i-1}, b_i \end{cases} \quad (4)$$

where: P, Q are constant factors of interval modification: $P \leq 1 \leq Q$.

Two other parameters establish a varying intervals border. The τ_{max} is the upper bound of the sampling period change and τ_{min} is the lower bound. These parameters sometimes assume the name f_{s_min} and f_{s_max} . The τ_0 is called f_{s_start} and its value decides about the average output bit rate.

Formula (4) represents the 3-bit interval change adaptation algorithm. It is also described by the Modify Interval Function (MIF) table (<1 means increase frequency, >1 decrease frequency, 1 denotes a come back to start frequency).

Table 1. MIF Table

b_{i-2}	b_{i-1}	b_i	MIF
0	0	0	<1
0	0	1	1
0	1	0	>1
0	1	1	1
1	0	0	1
1	0	1	>1
1	1	0	1
1	1	1	<1

One can see that the NSDM output binary stream carries the information of not only the changing trend of the source signal but also the sampling timing of the modulator. So that in the demodulation process the irregular staircase signal can be recovered [3].

2.1 Modulation features

The idea of using variable sampling to reduce the data rate of source coding is the topic that is still not completely understood. Earlier analytical investigations showed a very good performance of non-stationary input process reconstruction for the duration of conversion that

applied non-uniform sampling [6]. So there are some hopes for improvement the compression and quality results while converting, in the real time, speech signals (TV, video) [3,7].

A voice encoding system based on ADM codecs has already been used in the Shuttle system. ADM modulation was chosen by NASA for source encoding of voice because of its tolerance to channel errors. Today, there are many military and commercial systems using this method [8, 9, 10]. They are particularly useful for applications in TDM systems, switches and phones. Bluetooth™ standard [11] employs a low-cost, 64-kbps Continuously Variable Slope Delta (CVSD) modulation voice-coding scheme. Several semiconductor manufacturing companies (CML Microcircuit, National Semiconductor, and GCT Semiconductor) produce specialized telecommunication ICs based ADM codecs.

As far as ADM modulations (e.g. CVSD, CFDM) are concerned Abate [1] and, then, Taub [2] show that the introduction of adaptation of the quantization step size does not change the minimum value of the total noise of quantization, i.e. maximum ratio SNR. However, a considerable extension of the dynamic range DR in which this maximum value is obtained is the effect of the adaptation.

The NSDM mechanism can be included in the analog to digital converters providing increased dynamic range DR of the signals possible for processing in relation to the LDM modulation. The Abate [1] theses about equality of the maximum ratio SNR for LDM and ADM shows an increase of the dynamic range of ADM in relation to LDM modulation.

Another interesting feature which comes from the adaptation of sampling frequency is power reduction. If CMOS technology is used, two main components will determine the power consumption in this circuit: the static power consumption and dynamic power consumption. CMOS devices have very low static power consumption, which is the result of the leakage current. This power consumption occurs when all inputs are held at same valid logic state and the circuit is not in charging states. But, when switching at high frequency, dynamic power consumption can contribute significantly to the total power consumption. Charging and discharging a capacitance output load further increases this dynamic power consumption [12, 13]. Based on the fact that digital CMOS circuits generally consume the energy in dynamic state, each process decreasing the frequency is useful.

2.2 Principles of hardware realization

The adaptation of sampling frequency used to be extremely complicated for practical realization and non-profitable take into consideration costs. At the present

moment the development of microprocessor and frequency synthesis (for instance Direct Digital Synthesis - DDS or Phase Lock Loop - PLL) makes plain carrying out experimental investigations of the codec architecture with non-uniform sampling significant.

According to analytical and simulation analysis the following general method of the NSDM converter parameters selection is suggested [5, 14, 16]:

- for the pre-determined parameters of the input signal: quality (measured by SNR) and minimal signal power S_{min} , the minimal sampling frequency $f_{s_{min}}$ is found;
- having $f_{s_{min}}$ the step size Δ – is determined;
- having S_{min} , $f_{s_{min}}$, and assigned maximum signal power S_{max} (i.e. dynamic range DR necessary to achieve) $f_{s_{max}}$ is found.

Due to the emulation result of the processing speech signal, the interval (frequency) step modification factor P should be equal $0.5 \div 0.8$ and $Q - 1.1 \div 1.4$ [2, 7, 14].

So the based parameters were defined: step size, start frequency, range of frequency change ($f_{s_{min}}$ and $f_{s_{max}}$) and modification factors: P, Q .

3 Audio System based on NSDM

Building the system its quality and type of coded signal were assumed. In order to achieve good quality (SNR equal or greater then 21dB) the NSDM converter based on the principles in subsection 2.2 has to change sampling frequency from 10 kHz to 1MHz. In view of that, working in real time requires computational time between two consecutive samples less then $1\mu s$.

Due to the short processing time and fact that a shape of converter architecture was not known well at the beginning of the design, the DSP processor was chosen for codec implementation. It attracted a negative consequence (it is discussed in the following subsection) but guaranteed the flexible algorithm change.

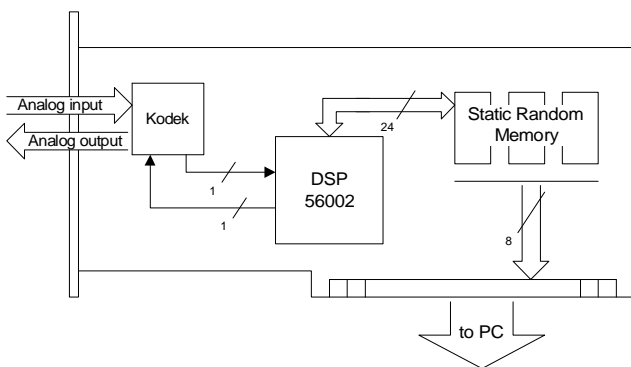


Fig.2. NSDM System PC Card

The evaluation kit with Motorola 56002 DSP processor that contains all necessary features and

capabilities to implement modulation was used. It also provided an efficient and cost-effective vehicle for hardware and software development [15]. The card is installed into PCI slots and communicates via special Windows driver (Fig.2).

3.1 DSP implementation

The NSDM codec idea is shown in Fig.3. It consists of 4 elements: A/D and D/A converter with 16 bits resolution, DSP processor with RAM, and PC computer with special application. The analogue input signal is coded by the A/D converter and then modulated with the NSDM algorithm in DSP. Output data are transmitted to the memory and storage. Encoding process begins with reading memory, then the demodulation algorithm is used and new data are transmitted to the D/A converter.

All the processes are asynchronous and triggered by the DSP processor. The sampled value from the A/D converter is transmitted to the processor Synchronous Serial Interfaces (SSI), which generates the interrupt signal when transmission ends. But the time when the current sample should be taken is triggered by the DSP.

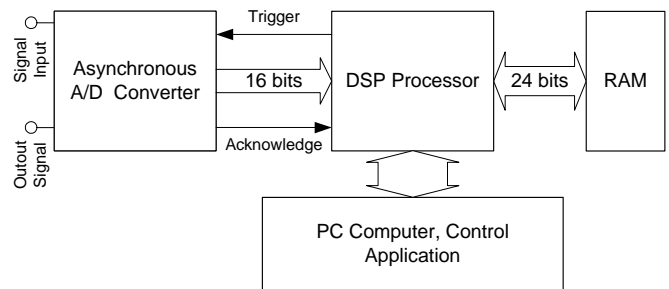


Fig.3. Block diagram of the NSDM audio system

In the first model, the time interval was generated by the DSP timer/counter unit that was programmed according to the current modulation result. When the timer reached the set value it generated its own interrupt and then processor triggered the A/D converter. The end of conversion caused another interrupt that starts a calculation of the current predicted signal amplitude and the time to the next sample moment. The sampling interval was determined by the timer/counter processor unit which was programmed by an initial value. All necessary sampling periods was placed in a special table, and the pointer to the position of the current value was modified according to the MIF table. After that, all not used processor units are turned off and idle time starts (Fig.4)

Unfortunately, presented realization did not meet the assumption, because maximum reached frequency was only 44.1 kHz. It was brought about by the too slow A/D converter. So the idea had to be rebuilt and now the A/D converter is working independently of the DSP processor sending a new sample directly to the processor SSI

interface. Then timer/counter unit trigger only the processor and obtained the sample is treated as analog value $x(t)$ (Fig.1.) that is converted to bit series of variable frequency. In this case the NSDM converter guarantees the assumed performance.

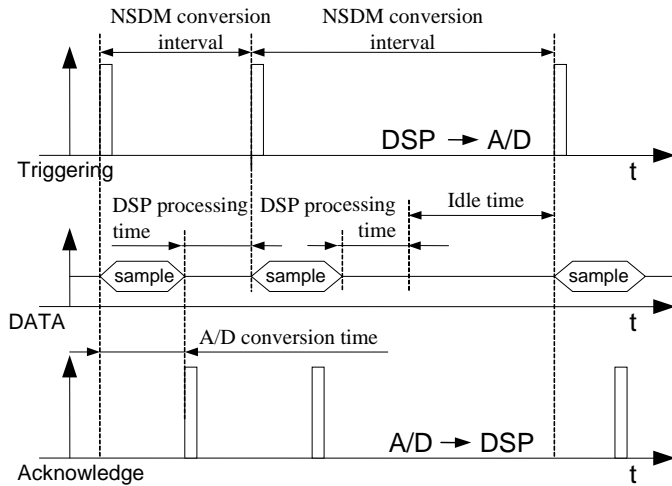


Fig.4. NSDM algorithm DSP implementation timing

3.2 Implementation problems

The main problem of the implementation audio system based on the non-uniform sampling delta modulation is processor computational efficiency required for precise determining a consecutive clock interval. Direct implementation of the pure algorithm requires 7 arithmetic operations (multiplication, addition and subtraction) to adopt a new sampling moment. It is obvious that it is the worse case, when the input signal slope has the greatest values and conversion time ought to be less than $1\mu s$. This relation occurs when:

$$T_{cmd} \leq \frac{\tau_{min}}{N_{oper}} \quad (4)$$

Where: T_{cmd} – command time, τ_{min} – minimum sampling interval, N_{opr} – number of the processor operation during one conversion cycle.

Because factors: P, Q and that of the established frequency boundary are constant during processing all intervals from τ_{min} to τ_{max} could be fixed and stored into the look-up table. So then the next sampling interval is considered of MIF and it is fast fixed without computing.

For the reason that, the timer register TCR resolution is 24 bits and the fixed number representation in the processor is 24 bits, all the calculated values are rounded down, so a little numerical error occur and the sequence of interval adaptation is upset. Although recently the development statistical analysis of frequency changing has shown that number of the most probable value might be limited and some of them are unnecessary.

The accurate look at the hardware implementation uncovers another trouble [16]. The interrupt driven management is advantageous when it is difficult to anticipate the service request of the peripheral, and when the service latency must be short. Unfortunately the SSI unit and the timer/counter unit have the same interrupt priority. In this case, the SSI unit interrupt service routine blocks the proper timer service. This mechanism causes a sampling jitter, that value is smaller than the minimum interval time. Considering NSDM modulation 100 times oversampling, the jitter negative influence in signal reconstruction is hardly noticeable and, furthermore, minimized by the smooth filter. Another successful solution is a disabling interrupt during the NSDM calculation.

To examine the system performance series of speech the coding process was recorded. Due to, the signal quality, maximum and minimum frequency were obtained. The shortest time between two samples was equal to $1.36\mu s$, so the was $f_{s,max}$ 730 kHz. It is a result of 90 necessary coding operations in front of the 15.1ns system clock period. So, that is why the quality becomes a worse. The maximum time is not strongly limited and could reach 0.25ms.

4. CODEC architecture

The result of DSP implementation has disclosed that advantages of a coding efficiency with NSDM require a drawing up new codec architecture (Fig.5). The simulation experiment of different realization allowed finding the best solution. Codec consists of the tree major elements: analog comparator, logic adaptation block with the sampling frequency generator and A/D converter (Fig.6).

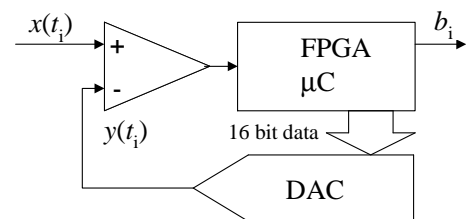


Fig.5. NSDM codec block diagram

The comparator is substantially the same and operates in substantially the same manner as the component of the basic block diagram. The adaptation interval block consists of the coincidence shift register, programmable clock divider and MIF. All these establish the time to the next sampling moment that is generated by the programmable clock. To eliminate computational complexity of frequency equation solving, all of them are calculated at the beginning of conversion and store

as a divider value in the frequency table. The loop back integrator, which reconstructs the input signal is known as a charge parceling integration [17]. This integration technique results in the application of a quantum of charge to the integrating capacitor C_1 . A controlled amount of the charge independent of current capacitor voltage is added to or subtracted from the integrating capacitor C_1 . Since the charge transfer is completely within a few nanoseconds the widths of the pulses from output gates do not affect the charge process consequently. The use of the charge parceling integration technique avoids step size variations due to timing fluctuations in the stair case appearance of the predicted signal [17, 18].

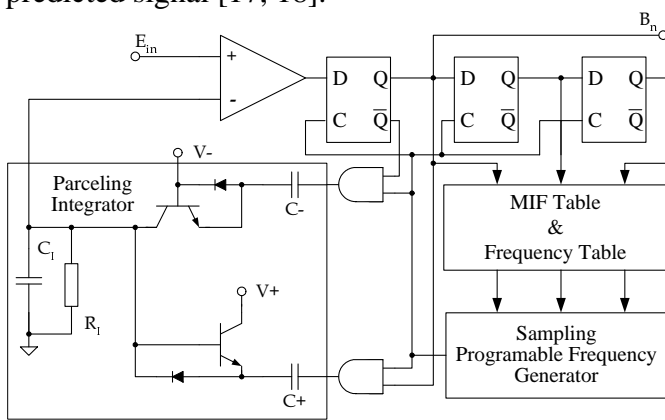


Fig. 6. Example of simple NSDM A/D converter's architecture with the R. Laane- B.T. Murphy parcelling integrator.

4 Conclusion

In the paper the NSDM algorithm implementations, their performance characteristics and new codec architecture were described. As it was shown, the key to effective use of the NSDM is a proper choice of its internal parameters (step size, start frequency, τ_{min} and τ_{max} , P , Q factors).

The DSP realization is used for the signal processing technique because it operates at a relatively high sampling rate. The implementation and refinements of the final form of the hardware were performed at the DSP evaluation kit with the special PC configuration program. The result of this implementation has disclosed that advantages of a coding efficiency will require new codec architecture.

The last paragraph illustrates the idea of the building analog to the digital converter with the help of the non-uniform sampling method. Each of elements, both analog and digital, that is used for this realization can be put together on one chip, making up a piece of the System on Chip circuit (or the ASIC chip dedicated to

special purpose, such as: wireless telecommunication, measuring, etc...).

The author's intention is to apply the variable sampling method for the CVSD modulation [10] in order to combine a large dynamic range of the NSDM modulation and high tolerance to channel errors of the CVSD modulation. The description of this kind of the hybrid modulation that is called ANSDM (Adaptive NSDM) has been given in the [7]. The presented codec could be applied in a multi-subscriber variable-rate communication system, where the sampling rate of each subscriber will be varied according to the speech activity improving the channel capability.

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