A Fully Integrated Concurrent Dual-band Low-Noise Amplifier Using InGaP/GaAs HBT Technology

YU-TSO LIN and SHEY-SHI LU Graduate Institute of Electronics Engineering National Taiwan University Taipei, 10617 Taiwan, R.O.C.

Abstract: - A fully integrated concurrent dual-band low noise amplifier using InGaP/GaAs HBT technology is demonstrated for the first time. A new methodology is proposed so as to achieve simultaneous narrow-band gain and impedance matching at multiple frequencies. The experimental results showed that input return losses of -16.2 and -12.1 dB, voltage gains of 16.8 and 20.1 dB and noise figures of 2.72 and 2.88 dB were obtained at 2 GHz and 4.6 GHz, respectively with power consumption of 12 mW.

Key-Words: - Concurrent, dual-band, LNA, HBT, wireless.

1 Introduction

The diverse range wireless of modern applications necessitates the need to develop a transceiver wireless that can integrate multi-standards in a single chip [1]. While dual-band transceivers by switching between two different bands and receive one band at a time have been introduced [2-3], they are not sufficient as multi-functionality transceivers [4]. In order to solve the inevitable increase in cost, footprint and power dissipation brought by the conventional receiver architectures with multiple independent signal paths for the simultaneous operation at different frequencies, recently Hashemi and Hajimiri have introduce a new concurrent dual-band receiver architecture and the concurrent dual band low-noise amplifier (LNA) for the new architecture [4]. Although excellent performance of this kind of LNA has been reported, one off-chip capacitor and 2 off-chip inductors are required [4]. In this work, a fully integrated concurrent dual-band InGaP/GaAs LNA without any off-chip component is reported. The experimental results showed that voltage gains of 16.8 dB and 20.1 dB, input return losses of -16.2 dB and -12.1 dB, and noise figures of 2.72 dB and 2.88 dB were obtained at 2 GHz and 4.6 GHz, respectively with power consumption of 12 mW.

2 Principles of Circuit Design

The schematic of our dual-band image rejection LNA is depicted in Fig. 1. In this circuit, both Q1 and Q2 operate as common-emitter stages, but they share the same bias current. The signal amplified by Q1 is

coupled to the base of Q2 by C1 while the emitter of Q2 is bypassed by C3 to ground. Power dissipation is reduced through the reuse of the bias current. Traditionally an emitter degenerative inductor is used to generate the 50 Ω for input matching [5]. The concurrent multi-band LNA based on this input matching method requires a parallel LC network in series with one inductor [4], which amounts to one off-chip capacitor and 2 off-chip inductors. Instead of using inductive feedback technique, the concurrent multi-band LNA presented here adopts the recently developed capacitive feedback technique for multi-band input matching [6]. Namely, the input impedance of the second stage amplifier in parallel with load resistance R1 of the first stage provides the necessary parallel RC load of the capacitive feedback amplifier composed of transistor Q1, inductor L1 and capacitor CF for input matching. For the new concurrent dual-band receiver architecture [4], image rejection is necessary. The LC tank consisting of L2 and C2 connected at the emitter of Q2 resonates at image frequency and hence reduces the gain of the image signal. A series LC branch (L4-C4) in parallel with the parallel LC tank composed of L3 and C5 introduces a zero in the gain transfer function of the LNA at its series resonant frequency, which determines the frequency of the notch in the transfer function. This notch also contributes to the enhancement of the image rejection.

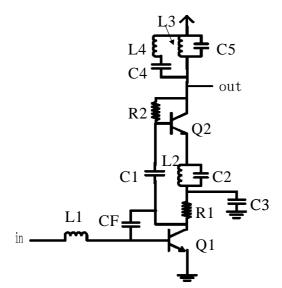


Fig. 1. The schematic of the InGaP/GaAs dual-band image rejection LNA.

3 Measures Results and Discussion

The concurrent dual-band image rejection LNA shown in Fig. 1 was implemented in a standard InGaP/GaAs process by the commercial foundry GCTC. The circuit parameters are: L1 = 0.18 nH, R1 $= 220 \Omega$, R2 = 1200 Ω , C1 = 3 pF, C2 = 2.3 pF, C3 = 2 pF, C4 = 2.24 pF, C5 = 2.48 pF, CF = 0.11 pF, L2 = 1.16 nH, L3 = 0.73 nH and L4 = 1.16 nH. Both transistors Q1 and Q2 have the same emitter size of 3 µm x 12 μm x 1 emitter finger. The die photo of the finished circuit is shown in Fig. 2. Note that the core circuit (excluding the pads for testing) only occupies a very small area of 380 µm x 560 μm. The noise and scattering parameters were measured on wafer using an automated NP5 measurement system from ATN Microwave Inc.

The measured input return loss S_{11} and voltage gain A_V of the dual-band image rejection LNA when biased with $V_{CC} = 3.3$ V and $I_C = 3.5$ mA are shown in Fig. 3. The S_{11} is below -10 dB from 1 GHz to 6 GHz, indicating a very broadband matching characteristic of this new input matching technique. Since this LNA is intended for integrated front-end circuits, the voltage gain (A_V) instead of S_{21} is reported here [4]. The narrow-band voltage gains of 16.8 dB and 20.1 dB at 2 GHz and 4.6 GHz are achieved, respectively. The notch is about 31.6 dB deeper than the peaks, which is translated to the same amount of improvement in image rejection. The measured noise figures are shown in Fig.4. Noise figures (NF) of 2.72 and 2.88 dB are obtained at 2 GHz and 4.6 GHz, respectively. From the experimental results, it is clear that a miniaturized, fully monolithic 2 GHz and 4.6

GHz concurrent dual-band image rejection LNA is realized. The comparison with the prior art of LNA [4] is shown in table one.

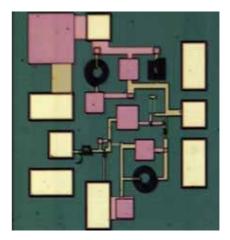


Fig. 2. The die photograph of the monolithic dual-band image rejection LNA

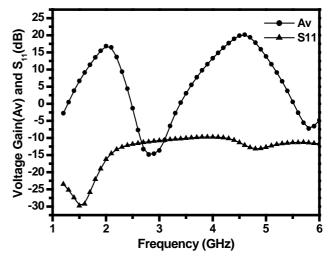


Fig. 3. The measured input return loss S_{11} and voltage gain A_V .

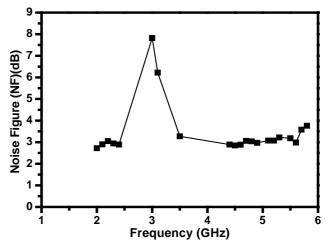


Fig. 4. The measured noise figure NF.

4 Conclusion

The first concurrent dual-band image rejection low-noise amplifier using InGaP/GaAs technology is reported. This fully integrated LNA does not need any off chip component for multi-band input matching and is very small (380 um x 560 um). Shunt-shunt capacitive feedback instead of traditional series-series inductive feedback technique is adopted for input multi-band matching. This concurrent dual band LNA achieves voltage gains of 16.8 dB and 20.1 dB, input return losses of -16.2 dB and -12.1 dB, and noise figures of 2.72 dB and 2.88 dB at 2 GHz and 4.6 GHz, respectively with power consumption of 12 mW. Image rejection ratio greater than 31.6 dB is also obtained.

Table one Comparison with the prior art of LNA

	This work		[4]		
Frequency band	2	4.6	2.45	5.25	GHz
Technology	InGaP 2 um		CMOS 0.35 um		
Voltage gain	16.8	20	14	15.5	dB
S ₁₁	- 16.2	- 12.1	- 25	- 15	dB
Noise figure	2.72	2.88	2.3	4.5	dB
Supply voltage	3.3		2.5		V
DC current	3.5		4		mA
Power consumption	12		10		mW

Acknowledgment

Financial supports from national science council unnder contract no. NSC94-2212-E-002-067 is appreciated.

References:

[1] T. Schwanenberger, M. Ipek, S. Roth, H. Schemmann, "A Multi Standard Single-Chip Transceiver Covering 5.15 to 5.85 GHz," *ISSCC Dig. of Tech. Papers*, pp.350-351, Feb. 2003.

[2] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," *IEEE JSSC*, vol. 33, no. 12, pp. 2178-2185, December 1998.

[3] J. Ryynanen, K. Kivekas, J. Jussila, A. Parssinen and K. Halonen, Helsinki University of Technology, Helsinki, Finland, "A dual-band RF front-end for WCDMA and GSM applications," *CICC Dig. of Tech. Papers*, pp.175-8, May 2000. [4] H. Hashemi and A. Hajimiri, "Concurrent dual-band CMOS low noise amplifiers and receiver architectures," *Dig. of Symposium on VLSI circuits,* pp.247-250, June 2001.

[5] R. G. Meyer and W. D. Mack, "A 1-GHz BiCMOS RF front-end integrated circuit," *IEEE J. Solid State Circuits*, vol.29, no.3, pp.350-355, Mar. 1994.

[6] P.-W. Lee, H.-W. Chiu, T.-L. Hsieh, C.-H. Shen, G.-W. Huang, S.-S. Lu, "A SiGe Low Noise Amplifier for 2.4/5.2/5.7 GHz WLAN Applications," *ISSCC Dig. of Tech. Papers*, pp.364-465, Feb. 2003.