Proceedings of the 5th WSEAS Int. Conf. on Electronics, Hardware, Wireless and Optical Communications, Madrid, Spain, February 15-17, 2006 (pp82-87)

RF SoS MOSFET Small Signal Model Extraction

ZONGRU LIU, EFSTRATIOS SKAFIDAS, ROB EVANS
Department of Electrical and Electronic Engineering
The University of Melbourne
Victoria 3010
AUSTRALIA

Abstract: - Access to an accurate small-signal equivalent circuit model is an important step in circuit design. Reliable small signal extraction procedures readily useable by the designer are now required in millimetre-wave designs because many foundry process development kits do not support millimetre wave frequency design. The extraction procedures successful at lower frequencies for lumped circuit extraction are prone to failure at higher frequencies. In many cases these procedures output unphysical values. This paper proposes a multi-step extraction procedure that is shown to accurately extract model parameters at higher frequencies. The contributions of this paper are: 1) A high frequency multi step extraction small signal model extraction procedure. This multi step procedure permits accurate extraction of parameters at millimeters wave frequencies. 2) A small signal equivalent high frequency model for a Silicon on Saphire (SOS).

Key-Words: - Small signal equivalent circuit, 60GHz, de-embedding, extrinsic parameters, intrinsic parameters

1 Introduction

In the last few years, 7GHz of contiguous bandwidth has been made available for unlicensed use at frequencies around 60GHz in the U.S.(57-64GHz) Canada (59-64GHz) and Japan (59-66 GHz). This allocation of spectrum has created significant interest in the communications community.

In order to facilitate cost effective solutions researchers have been investigating the applicability of designs based on CMOS type technologies [1]. The particular application pursued by the authors requires oscillators with low phase noise. In many cases the phase noise of oscillators is limited by the ability to build high-Q factor inductors [2]. Using Peregrine's silicon on sapphire process makes it easier for one to build high Q inductors. Unfortunately the supplied process development kit models do not support these frequencies.

The usual technique of either determining the parameters based on model extraction at one frequency non-least squares fit of data to a parameterized model, used successfully at lower frequencies [3,4,5], is prone to failure especially at these higher frequencies. A local minimum solution instead of the global and correct solution is found. In most cases the procedures described in [3,4,5] produce unphysical values, such as negative resistances and other components to the lumped circuit model.

These failure can be traced back to significant coupling between pads, radiation effects, higher measurement noise that is not additive Gaussian after the transformations from scattering (S) to impedance and admittance (Z and Y) parameters.

Physics usually guides the initialization at lower frequencies. Unfortunately at higher frequencies due to the increased complexity the relationship of the underlying physics to model parameters is more difficult to determine.

In this paper we will refer to components of the transistor model that are independent of biasing conditions as extrinsic components and those that depend on the bias conditions as intrinsic components.

In this paper a new method for small signal is presented in the next sections.

The new small signal model comprises of the following steps:

1. Measurement system calibration using a calibration substrate and a self consistent calibration model such as LRM+ or LRRM.
2. A 2-step de-embedding method using an open and short standard with pads built on the die to

determine and to extract the shunt and series parasitic contributions of pads.

3. Measurement of a new structure referred to as short-b is used to measure the contributions of the characteristics of the extrinsic series parameters. This structure is essentially similar to that of a transistor with pads, A least squares fit is performed in order to determine the series extrinsic parameters. These values are fixed during the optimization process (Another standard an open-b standard was also built. This was not used in this procedure because the extrinsic shunt parasitic after extraction where found not to be significant)
4. Measurement of the device under the required bias conditions. The intrinsic parameters are then extracted via the least square optimization method described in the subsequent sections.
5. Simulation of the extracted models and comparison with measured models.

The paper is organized as follows: Section 2) shows overall device model; Section 3) describes in detail the pads de-embedding procedure; section 4) describes the small signal model extraction; section 5) presents least square fittings of the extrinsic and intrinsic parameters; section 6) shows the results of the small signal extraction of a 0.25um 3 finger Peregrine transistor; section 7) concludes this paper.

2 Overall Device Model

Peregrine's Silicon-on-Sapphire (SoS) MOSFET's technology is a silicon technology built on a nearly perfect insulator. Figure 1 shows a transistors (3 fingers, finger width 8 um, channel length 0.25 um) built on using Peregrine's Silicon on Sapphire technology. The design is fabricated with three metal (aluminium) layers with the top layer being a thick metal layers

The pads are constructed as a sequence of metal squares on multiple layers with vias connecting the multiple metal and polycide layers.

Figure 2 shows the pad equivalent circuit. The exposed aluminum of the top layer grows an aluminum oxide layer which it with the combination of dissimilar metal being used in the probes and calibration substrate contribute to the extra contact resistance. Each pad can be modeled as a resistor in series with an inductor and each via as a shunt combination of an inductor and capacitor.

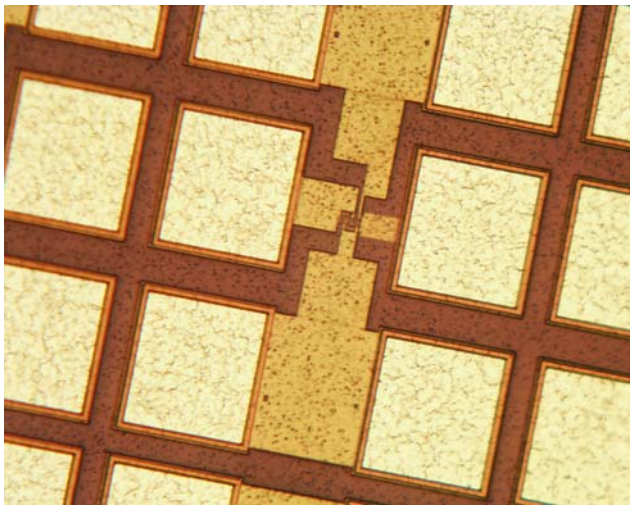

Figure 1
SoS MOSFET 3X8 P25

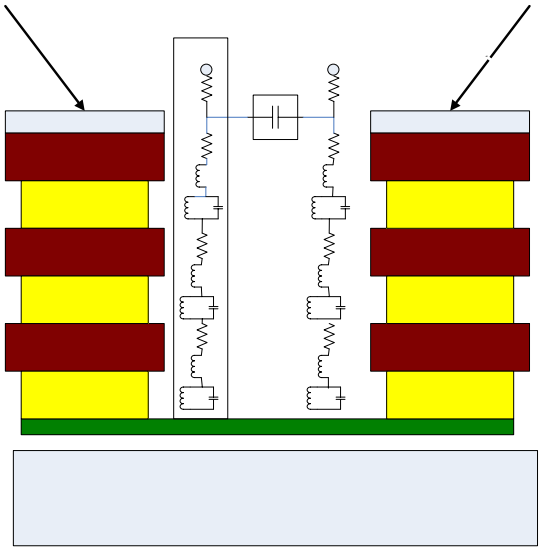

Figure 2
Equivalent Circuit for Pads

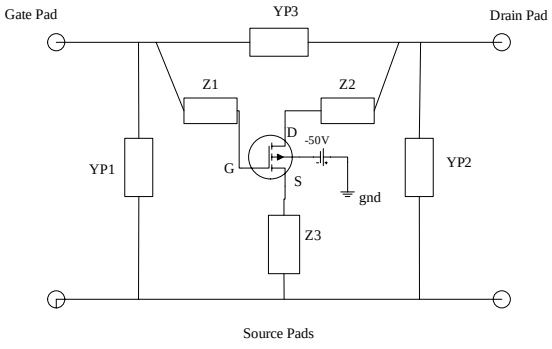

Figure 3
Transistor with parasitic components illustrated

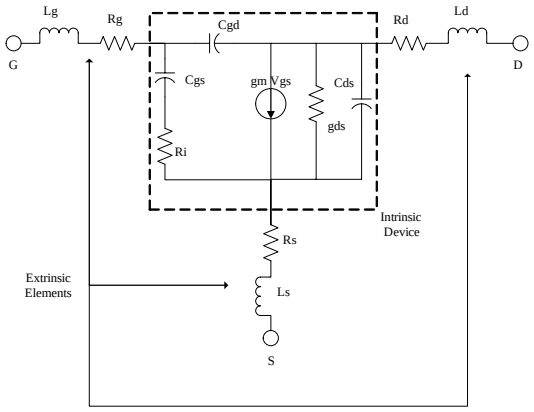

Figure 4
Transistor's Small-Signal Equivalent Circuit

Figure 3 illustrates the equivalent circuit of the series and shunt parasitics. For illustrative purposes a MOSFET is shown in this diagram with the base tied to a large negative value. This is to emphasize that the device is built on an isolating substrate. In this diagram the MOSFET includes all the intrinsic and extrinsic components. The small signal equivalent transistor circuit is shown in Figure 4 illustrating the intrinsic and extrinsic components. Note the extra resistance in the gate intrinsic component. This component has been added to permit a frequency dependant reduction in trans-conductance due to effects as carrier velocity saturation and other losses.

3 Pads De-embedding Procedure

When performing RF measurements on wafer, the measurement system has to be calibrated first, defining a reference plane for the S-parameter measurements at the probe tips using a standard technique such as LRM+ from SussCal Version 5.1.

De-embedding of PADs parasitics is needed. Figure 3 shows the actual transistor embedded in the parasitics introduced by the interconnect lines and bonding pads.

To determine the contributions of the device under test, we apply two step de-embedding method which uses an open and short standard shown in Figure 5 and Figure 6 respectively.

The open standard can be used to determine the parallel parasitics Yp1, Yp2, Yp3. The short standard with the shunt parasitics Yp1, Yp2, Yp3 and series parasitics Z1, Z2, and Z3 surrounding the transistor can be used to determine and remove the pad parasitics. This procedure is described next was first derived in [6] and included here for completeness.

Figure 5
Equivalent circuit for 'open' pattern. Note in this circuit the contact resistances have been lumped with the shunt elements

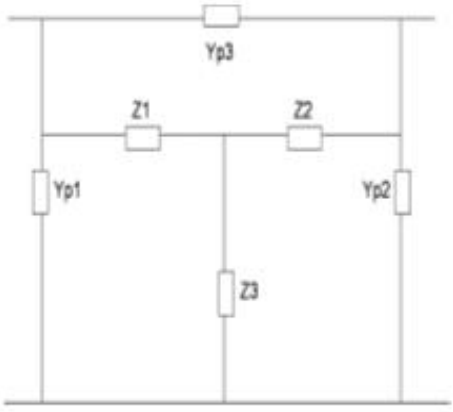

Figure 6
Equivalent 'Short' pattern used to characterize the series parasitics. Note that the equivalent circuit has the series impedances Z1, Z2 and Z3 embedded in parallel parasitics.

The transistor Z-parameters could be found by subtracting the Z-parameter matrix for the T-network from that of the total. This subtraction is performed at every measured frequency. No attempt is made to extract a lumped circuit model for the pads.
This pad extraction procedure is described as:

$$\begin{pmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{pmatrix} = (Y_{short} - Y_{open})^{-1} \quad (1)$$

$$Z_{trans} = (Y_{dut} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1} \quad (2)$$

where Y_{dut} is the measured Y-parameter matrix of the transistor together with parasitics and Z_{trans} is the actual transistor Z-parameter matrix after de-embedding.

4 Small Signal Model Extraction

The procedure for extracting the small-signal model is a two step process described below.

Step 1: After measuring the s-parameters of the short-b structure shown in Figure and its equivalent circuit in Figure . The conversion to Z-parameters is performed. The pads are de-embedded using equations (1) and (2). The lumped extrinsic elements are extracted by performing a constrained least square on the linear equations in (3).

$$\begin{bmatrix} R_g + j\omega L_g = Z_{11}^{short-b} - Z_{21}^{short-b} = Z_1 \\ R_d + j\omega L_d = Z_{22}^{short-b} - Z_{21}^{short-b} = Z_2 \\ R_s + j\omega L_s = Z_{21}^{short-b} = Z_3 \end{bmatrix} \quad (3)$$

The constraint is to ensure that the values of inductance and resistance are positive. The left hand side are the variables that are required to be extracted.

$$e_i = \sum_{n=1}^{N} \left| Z_i^{short-b}(f_n) - \hat{Z}_i^{short-b}(f_n) \right|^2 \quad (4)$$

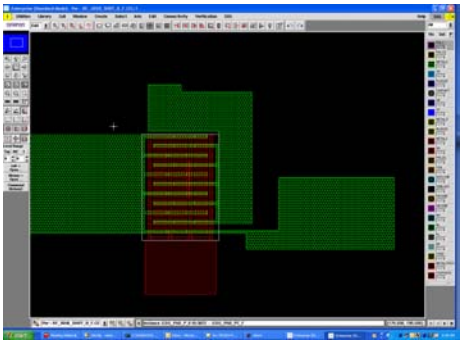

Figure 7

'Short-b' pattern on wafer used to characterize the extrinsic series parasitics.

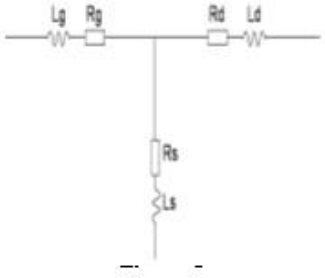

Figure 8

The equivalent circuit with series resistances and inductances Rs, Rd, Rg, Ls, Ld and Lg.

The inclusion of the short-b permits an accurate determination of the extrinsic elements.

Step 2: To calculate the intrinsic parameters, those extrinsic elements must be subtracted to get the intrinsic Y-matrix (Yin). Then we use formulas (5) to get the initial intrinsic elements.

$$\begin{aligned} R_i &= \max\left(\frac{re(Y_{11}^{in})}{im(Y_{11}^{in}+Y_{12}^{in})^2}, 0\right) \\ C_{gd} &= \max\left(-\frac{im(Y_{12}^{in})}{\omega}, 0\right) \\ C_{ds} &= \max\left(\frac{im(Y_{22}^{in}+Y_{12}^{in})}{\omega}, 0\right) \\ C_{gs} &= \max\left(\frac{im(Y_{11}^{in}+Y_{12}^{in})}{\omega}, 0\right) \\ g_{ds} &= \max\left(re(Y_{22}^{in}), 0\right) \\ g_m &= \left|Y_{21}^{in} - Y_{12}^{in}\right| \\ \tau &= \frac{\tan^{-1}\left(\frac{im(Y_{21}^{in}-Y_{12}^{in})}{re(Y_{21}^{in}-Y_{12}^{in})}\right)}{\omega} \end{aligned} \quad (5)$$

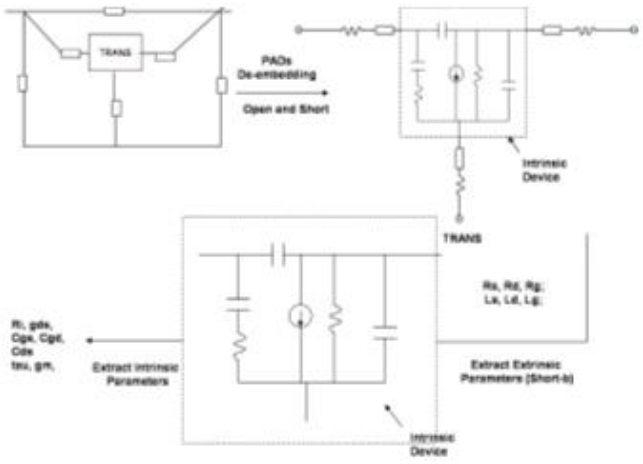

Figure 9

The detailed whole process

Figure 9 concludes the whole process including PAD de-embedding.

5 Least Square Fitting

Equations (6) are derived from the small signal intrinsic model [7], where $\hat{Y}_{ij}^{in}$ is the estimates of the intrinsic Y-matrix.

$$\hat{Y}_{11}^{in} = \frac{R_i C_{gs}^2 \omega^2}{D_1} + j\omega\left(\frac{C_{gs}}{D_1} + C_{gd}\right)$$

$$\hat{Y}_{12}^{in} = -j\omega C_{gd}$$

$$\hat{Y}_{21}^{in} = \frac{g_m \exp(-j\omega\tau)}{1 + j\omega R_i C_{gs}} - j\omega C_{gd} \qquad (6)$$

$$\hat{Y}_{22}^{in} = g_{ds} + j\omega(C_{ds} + C_{gd})$$

$$D_1 = 1 + \omega^2 C_{gs}^2 R_i^2$$

The error function is given by

$$e = \sum_{n=0}^{N} \sum_{ij} \left| \hat{Y}_{ij}^{in}(f_n) - Y_{ij}^{in}(f_n) \right|^2 \qquad (7)$$

The cost function given in equation (7) is minimized subject to the constraint that all the extracted components are positive.

6 Results

Figure 10 shows both the measured and de-embedded S-parameters of one of our smallest transistors (3X8 p25). The transistor is 3 fingers with finger width 8um, channel length 0.25 um. The bias condition is Vds = 1.5V, Vgs = 0.8V.

The success of subtracting the PAD parasitics is clear from the comparison of the measured and de-embedded S parameters.

Table 1 presents the extracted extrinsic parameters under the frequency range 0.5--65 GHz, where Rg, Rs, Rd are the series resistance in Ohm, Lg, Ls, Ld are the series inductances in pH. The values are independent of bias condition.

Table 2 presents the extracted intrinsic parameters (0.5--65GHz) under different bias conditions Vgs = 0.6V, 0.8V, 1.0V and 1.2V with Ri in Ohm, Cgs, Cgd, Cds in fF, τ in fs, gm, gds in mS.

Figure 11 shows the simulated S-parameter using Cadence Spectre versus the measurements after de-embedding. Good agreements are clear from the graph.

Rg	Rs	Rd	Lg	Ls	Ld
1.84	0.87	0.68	0.21	1.36	0.17

Table 1: extrinsic parameters

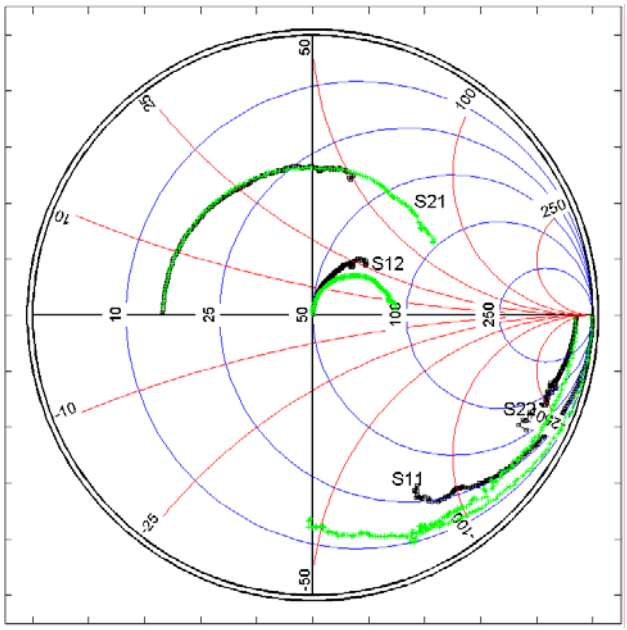

Figure 10
Measured (green +) V.S. de-embedded S-parameters (black)

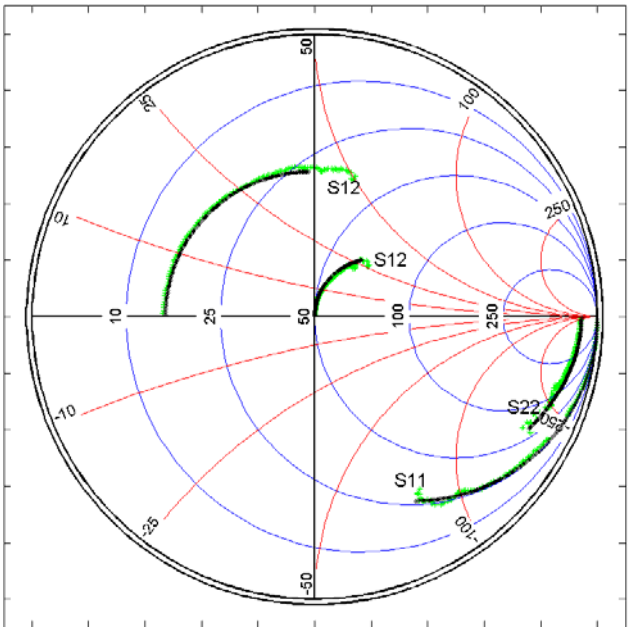

Figure 11
Simulated (green +) V.S. De-embedded S-parameters (black)

Vgs	Ri	Cgs	Cgd	Cds	τ	gm	gds
0.6	40.3	19.5	8.78	3.22	4.7	5.25	0.45
0.8	41.2	20.3	8.96	2.27	4.7	5.53	0.58
1.0	42.1	20.8	9.20	3.33	4.8	5.68	0.71
1.2	43.1	21.2	9.52	3.38	4.8	5.73	0.86

Table 2: intrinsic parameters

Ri------channel resistance (Ohm)
gm-----transconductance (mS)
gds-----reciprocal of drain-source resistance (mS)
τ -------transit time (fs)
L-------inductance (pH)
C-------capacitance (fF)
R-------resistance (Ohm)

7 Conclusion

A new extraction scheme has been demonstrated which, after introduction of new structure short-b, allows accurate and effective extraction of all small-signal circuit elements values from S-parameters measurements up to 65 GHz. The least square optimization technique is applied to compensate for the noisiness of the measurements. A two step de-embedding method has also been demonstrated. Unlike previews methods that need cold-FET technique or provide unphysical values, this new scheme is straightforward and provides physical values. The simulation results also show very well fit with the measurements.

Acknowledgement:

The authors would like to acknowledge Peregrine Semiconductor and National ICT Australia.

National ICT Australia is funded by the Australian Government's Department of Communications, Information Technology, and the Arts and the Australian Research Council through Backing Australia's Ability and the ICT Research Centre of Excellence programs.

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