Universal Sequencer for a Four-Phase Unipolar Stepper Motors

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Abstract: - The authors present in this paper a synthesis method of reversible pulse sequencers for 4 phase stepper motor and the usual operating sequences: normal drive, wave drive and half-step drive. From the study of different alternatives of pulse sequencers, the authors concluded that the synthesis using T flip-flops is more economical, concerning the simplicity of the combinational part and the time spared to perform this synthesis. Concerning the code used for assignation, the use of natural binary code led to simpler structures. The sequencers described in this paper, which can be made with TTL integrated circuits, offer a high functioning safety.

Key-Words: - Unipolar Stepper Motor, Sequencers Pulse and Synthesis Method.

1 Introduction

The performances of a Stepper Motor (SM) are tightly connected with type and quality of the used command and supply circuits. Among performances like damping, maximum values of operating frequency and dynamic torque, it can be noted here the efficiency and power losses which also depend in a large measure on the command and supply circuits [1], [2], [3].

Irrespective of open-loop or closed-loop control, in order to control and supply a SM the elements shown in Fig. 1 are needed.

The control of a stepper motor is usually done by a power electronic system, which supplies sequentially the phases of the SM. The distribution sense of supply, as well as the sequence type (symmetrical, asymmetrical) and the command frequency of phases are done by logical sequential processing with integrates circuits. The current waveforms in motor's phases are imposed by an electronic switching stage.

The role of this device is to take over the command pulses-usually standard TTL, CMOS (the command, sense and sequence type signals)-to distribute them sequentially, to amplify them and to deliver them to motor's phases (see Fig. 1).

Considering the above mentioned considerations, the authors present in this paper a synthesis method of reversible pulse sequencers for four-phase unipolar SM. The SM can be driven in three different sequences: wave drive mode, normal drive mode and half-step drive mode.

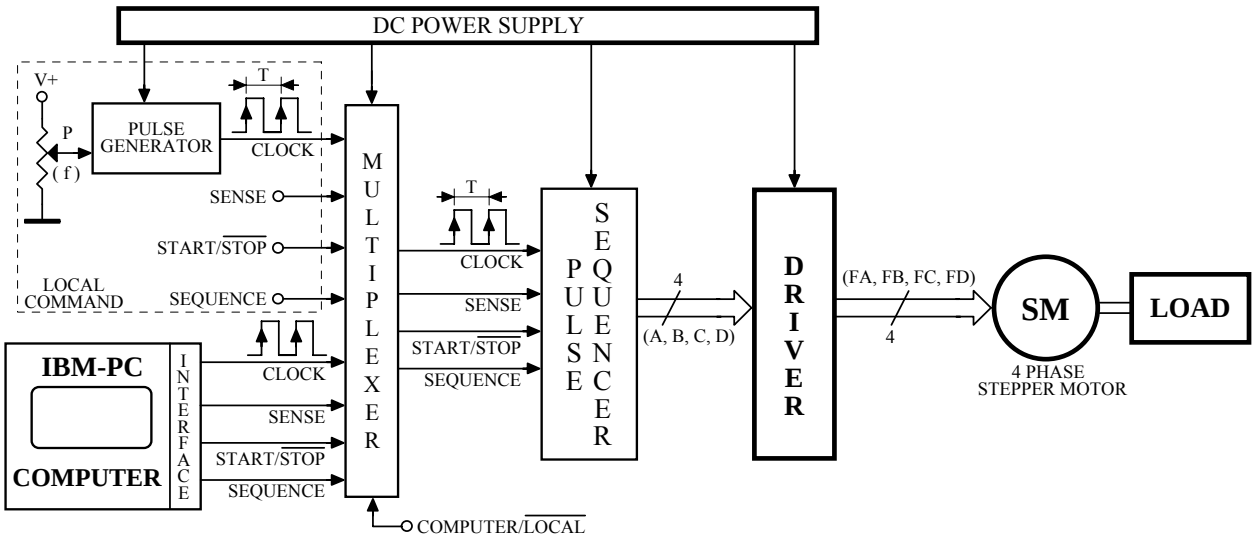

Fig. 1. Block diagram of the drive system of a SM.

2 Synthesis of pulse sequencers

The pulse sequencers are blocks which use command pulse train (TTL or CMOS compatible) and the sense command, in order to provide as outputs *m* (the number of motor phases) pulse trains phase shifted one to another with $2\pi/m$ electrical degrees (the electric step) [3], [4], [5], [7].

The versions achieved with flip-flop circuits are included among the simplest pulse sequencers [6], [7]. Using the synchronous flip-flops, the hazard phenomenon is eliminated.

We describe below the method of synthesis of a four phases stepper motor (A, B, C, D) sequencers for three supplies: wave drive, normal drive and half-step drive.

From the study of various alternatives of pulse sequencers, the authors concluded that the synthesis using T flip-flops is more economical, concerning the simplicity of the combinational part and the time spared to perform this synthesis. Concerning the code used for assignation, the use of natural binary code led to simpler structures. The T flip-flop functioning is based on truth (Table 1) and excitation (Table 2) tables as seen in Fig. 2.

Table 1

T	Q_n	Q_{n+1}	
0	0	0	Q_n
0	1	1	
1	0	1	$\overline{Q_n}$
1	1	0	

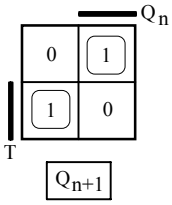

Table 2

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

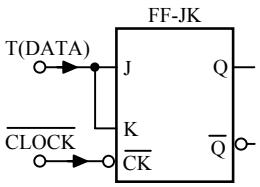

Fig. 2. Truth and excitation tables for T flip-flop.

$$Q_{n+1} = T \cdot \overline{Q_n} \cup \overline{T} \cdot Q_n = T \oplus Q_n \qquad (1)$$

The *S* variable establishes the rotation sense as following: clockwise S=1, anticlockwise S=0.

On wave drive mode (SS), at any moment it is supplied a single phase. So, there are the following situations:

-the clockwise (*S*=1) imposes the order: A, B, C, D, A, B, ...;

-the anticlockwise (*S*=0) imposes the order: A, D, C, B, A, D, ...

Analyzing the sequence for every rotation sense, results the necessity of a logical sequential circuit with four stable states. These can be materialized with two T flip-flops, of which outputs are noted with Q_1(MSB), Q_0(LSB).

On a normal drive mode (SD) there are supplied two phases simultaneously. So, there are the following situations:

-the clockwise (*S*=1) imposes the order: AB, BC, CD, DA, AB, ...;

-the anticlockwise (*S*=0) imposes the order: AB, AD, CD, BC, AB, AD, ...

As it was described above, it results the necessity of a logical sequential circuit with four stable states, which means two T flip-flops of which outputs are noted with Q_1(MSB), Q_0(LSB).

A half-step drive mode (SM) alternates a phase supply with two successive phases supply: one of these is the one supplied individually in a previous moment. There are following situations:

-the clockwise (*S*=1) imposes the order: A, AB, B, BC, C, CD, D, AD, A, ...;

-the anticlockwise (*S*=0) imposes the order: A, AD, D, CD, C, BC, B, AB, A, ...

As it was described above, it results the necessity of a logical sequential circuit with eight stable states, which means three T flip-flops of which outputs are noted with Q_2(MSB), Q_1, Q_0(LSB).

The assignation of states (Table 3) and the transitions graph are shown in Fig. 3.

Table 3

SM	SD	SS	PHASE SUPPLIED	STABLE STATES	FLIP-FLOPS			SEQUENCE
					Q_2	Q_1	Q_0	
0	0	1	A	S_0	0	0	0	WAVE DRIVE MODE (SS)
0	0	1	B	S_1	0	0	1	
0	0	1	C	S_2	0	1	0	
0	0	1	D	S_3	0	1	1	
0	0	1	A	S_4	1	0	0	
0	0	1	B	S_5	1	0	1	
0	0	1	C	S_6	1	1	0	
0	0	1	D	S_7	1	1	1	

Table 3 (Cont.)

SM	SD	SS	PHASE SUPPLIED	STABLE STATES	FLIP-FLOPS			SEQUENCE
					Q_2	Q_1	Q_0	
0	1	0	AB	S_0	0	0	0	NORMAL DRIVE MODE (SD)
0	1	0	BC	S_1	0	0	1	
0	1	0	CD	S_2	0	1	0	
0	1	0	DA	S_3	0	1	1	
0	1	0	AB	S_4	1	0	0	
0	1	0	BC	S_5	1	0	1	
0	1	0	CD	S_6	1	1	0	
0	1	0	DA	S_7	1	1	1	
1	0	0	A	S_0	0	0	0	HALF-DRIVE MODE (SM)
1	0	0	AB	S_1	0	0	1	
1	0	0	B	S_2	0	1	0	
1	0	0	BC	S_3	0	1	1	
1	0	0	C	S_4	1	0	0	
1	0	0	CD	S_5	1	0	1	
1	0	0	D	S_6	1	1	0	
1	0	0	DA	S_7	1	1	1	

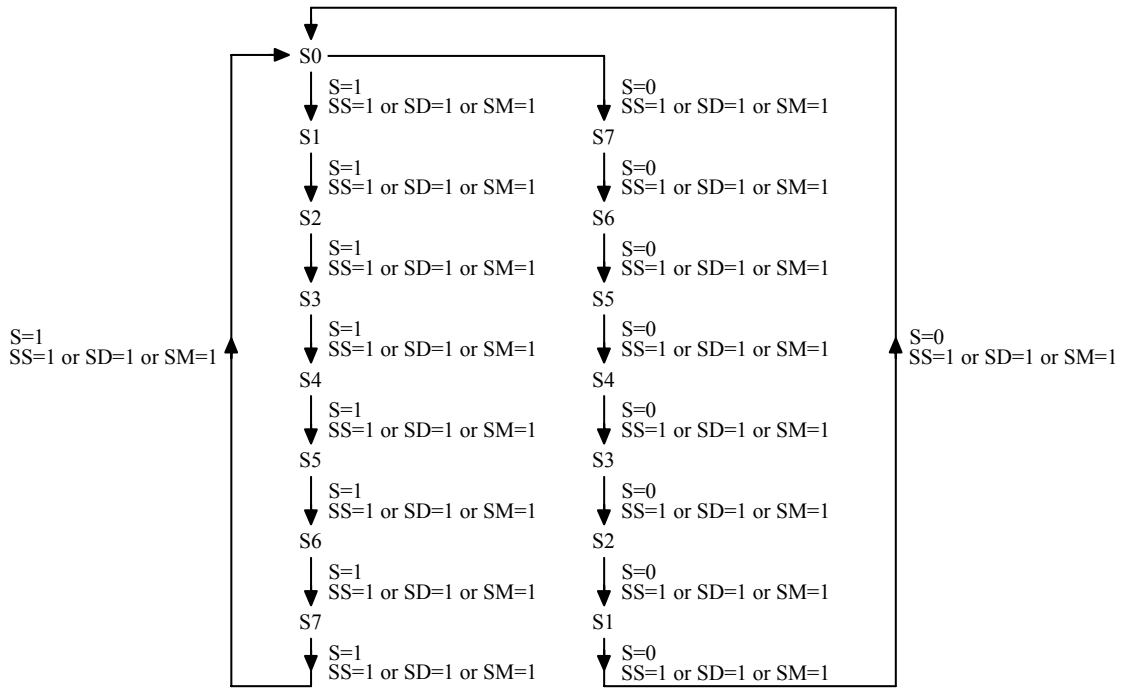

Fig. 3. Transitions graph.

The excitation table (Table 4) is presented in Fig. 4.

Thus, it results the same logical expressions for flip-flops inputs:

$$\begin{cases} T_2 = D^{SM\,SD\,SS\,S\,Q_2\,Q_1\,Q_0}_{1:(20,24,33,37,40,44,53,57,100,104,113,117)\ 0:(21,22,23,25,26,27,30,31,32,34,35,36,41,42,43,45,46,47,50,51,52,54,55,56,101,102,103,105,106,107,110,111,112,114,115,116)} = \\ = \overline{S} \cdot \overline{Q_1} \cdot \overline{Q_0} \cup S \cdot Q_1 \cdot Q_0 \\ T_1 = D^{SM\,SD\,SS\,S\,Q_2\,Q_1\,Q_0}_{1:(20,22,24,26,31,33,35,37,40,42,44,46,51,53,55,57,100,102,104,106,111,113,115,117)\ 0:(21,23,25,27,30,32,34,36,41,43,45,47,50,52,54,56,101,103,105,107,110,112,114,116)} = \overline{S} \cdot \overline{Q_0} \cup S \cdot Q_0 = \overline{S \oplus Q_0} \\ T_0 = \text{"1"} \end{cases} \quad (2)$$

Table 4

n_S (O)	SM	SD	SS	S	t_n			t_{n+1}			FLIP-FLOPS			SEQUENCE
					Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	T_2	T_1	T_0	
20	0	0	1	0	0	0	0	1	1	1	1	1	1	WAVE DRIVE MODE Anticlockwise
21	0	0	1	0	0	0	1	0	0	0	0	0	1	
22	0	0	1	0	0	1	0	0	0	1	0	1	1	
23	0	0	1	0	0	1	1	0	1	0	0	0	1	
24	0	0	1	0	1	0	0	0	1	1	1	1	1	
25	0	0	1	0	1	0	1	1	0	0	0	0	1	
26	0	0	1	0	1	1	0	1	0	1	0	1	1	
27	0	0	1	0	1	1	1	1	1	0	0	0	1	
30	0	0	1	1	0	0	0	0	0	1	0	0	1	WAVE DRIVE MODE Clockwise
31	0	0	1	1	0	0	1	0	1	0	0	1	1	
32	0	0	1	1	0	1	0	0	1	1	0	0	1	
33	0	0	1	1	0	1	1	1	0	0	1	1	1	
34	0	0	1	1	1	0	0	1	0	1	0	0	1	
35	0	0	1	1	1	0	1	1	1	0	0	1	1	
36	0	0	1	1	1	1	0	1	1	1	0	0	1	
37	0	0	1	1	1	1	1	0	0	0	1	1	1	
40	0	1	0	0	0	0	0	1	1	1	1	1	1	NORMAL DRIVE MODE Anticlockwise
41	0	1	0	0	0	0	1	0	0	0	0	0	1	
42	0	1	0	0	0	1	0	0	0	1	0	1	1	
43	0	1	0	0	0	1	1	0	1	0	0	0	1	
44	0	1	0	0	1	0	0	0	1	1	1	1	1	
45	0	1	0	0	1	0	1	1	0	0	0	0	1	
46	0	1	0	0	1	1	0	1	0	1	0	1	1	
47	0	1	0	0	1	1	1	1	1	0	0	0	1	
50	0	1	0	1	0	0	0	0	0	1	0	0	1	NORMAL DRIVE MODE Clockwise
51	0	1	0	1	0	0	1	0	1	0	0	1	1	
52	0	1	0	1	0	1	0	0	1	1	0	0	1	
53	0	1	0	1	0	1	1	1	0	0	1	1	1	
54	0	1	0	1	1	0	0	1	0	1	0	0	1	
55	0	1	0	1	1	0	1	1	1	0	0	1	1	
56	0	1	0	1	1	1	0	1	1	1	0	0	1	
57	0	1	0	1	1	1	1	0	0	0	1	1	1	
100	1	0	0	0	0	0	0	1	1	1	1	1	1	HALF-DRIVE MODE Anticlockwise
101	1	0	0	0	0	0	1	0	0	0	0	0	1	
102	1	0	0	0	0	1	0	0	0	1	0	1	1	
103	1	0	0	0	0	1	1	0	1	0	0	0	1	
104	1	0	0	0	1	0	0	0	1	1	1	1	1	
105	1	0	0	0	1	0	1	1	0	0	0	0	1	
106	1	0	0	0	1	1	0	1	0	1	0	1	1	
107	1	0	0	0	1	1	1	1	1	0	0	0	1	
110	1	0	0	1	0	0	0	0	0	1	0	0	1	HALF-DRIVE MODE Clockwise
111	1	0	0	1	0	0	1	0	1	0	0	1	1	
112	1	0	0	1	0	1	0	0	1	1	0	0	1	
113	1	0	0	1	0	1	1	1	0	0	1	1	1	
114	1	0	0	1	1	0	0	1	0	1	0	0	1	
115	1	0	0	1	1	0	1	1	1	0	0	1	1	
116	1	0	0	1	1	1	0	1	1	1	0	0	1	
117	1	0	0	1	1	1	1	0	0	0	1	1	1	

Fig. 4. Excitation table.

The states decoding (Table 5) is presented in Fig. 5.

Table 5

n_S (O)	SM	SD	SS	FLIP-FLOPS			STABLE STATES	PHASE SUPPLIED				SEQUENCE
				Q_2	Q_1	Q_0		A	B	C	D	
10	0	0	1	0	0	0	S_0	1	0	0	0	WAVE DRIVE MODE
11	0	0	1	0	0	1	S_1	0	1	0	0	
12	0	0	1	0	1	0	S_2	0	0	1	0	
13	0	0	1	0	1	1	S_3	0	0	0	1	
14	0	0	1	1	0	0	S_4	1	0	0	0	
15	0	0	1	1	0	1	S_5	0	1	0	0	
16	0	0	1	1	1	0	S_6	0	0	1	0	
17	0	0	1	1	1	1	S_7	0	0	0	1	
20	0	1	0	0	0	0	S_0	1	1	0	0	NORMAL DRIVE MODE
21	0	1	0	0	0	1	S_1	0	1	1	0	
22	0	1	0	0	1	0	S_2	0	0	1	1	
23	0	1	0	0	1	1	S_3	1	0	0	1	
24	0	1	0	1	0	0	S_4	1	1	0	0	
25	0	1	0	1	0	1	S_5	0	1	1	0	
26	0	1	0	1	1	0	S_6	0	0	1	1	
27	0	1	0	1	1	1	S_7	1	0	0	1	
40	1	0	0	0	0	0	S_0	1	0	0	0	HALF-DRIVE MODE
41	1	0	0	0	0	1	S_1	1	1	0	0	
42	1	0	0	0	1	0	S_2	0	1	0	0	
43	1	0	0	0	1	1	S_3	0	1	1	0	
44	1	0	0	1	0	0	S_4	0	0	1	0	
45	1	0	0	1	0	1	S_5	0	0	1	1	
46	1	0	0	1	1	0	S_6	0	0	0	1	
47	1	0	0	1	1	1	S_7	1	0	0	1	

Fig. 5. States decoding.

Thus, it results the same logical expressions for the logic sequencer outputs:

$$
\begin{cases}
A = D^{SM\,SD\,SS\,Q_2\,Q_1\,Q_0}_{\substack{1:(10,14,20,23,24,27,40,41,47)\\ 0:(11,12,13,15,16,17,21,22,25,26,42,43,44,45,46)}} = \\
= SS(\overline{Q_1}\cdot\overline{Q_0}) \cup SD(\overline{Q_1 \oplus Q_0}) \cup SM(\overline{Q_2}\cdot\overline{Q_1} \cup Q_2\cdot Q_1\cdot Q_0) \\
B = D^{SM\,SD\,SS\,Q_2\,Q_1\,Q_0}_{\substack{1:(11,15,20,21,24,25,41,42,43)\\ 0:(10,12,13,14,16,17,22,23,26,27,40,44,45,46,47)}} = \\
= SS(\overline{Q_1}\cdot Q_0) \cup SD\cdot\overline{Q_1} \cup SM\cdot\overline{Q_2}(Q_1 \cup Q_0) \\
C = D^{SM\,SD\,SS\,Q_2\,Q_1\,Q_0}_{\substack{1:(12,16,21,22,25,26,43,44,45)\\ 0:(10,11,13,14,15,17,20,23,24,27,40,41,42,46,47)}} = \\
= SS(Q_1\cdot\overline{Q_0}) \cup SD(Q_1 \oplus Q_0) \cup SM(\overline{Q_2}\cdot Q_1\cdot Q_0 \cup Q_2\cdot\overline{Q_1}) \\
D = D^{SM\,SD\,SS\,Q_2\,Q_1\,Q_0}_{\substack{1:(13,17,22,23,26,27,45,46,47)\\ 0:(10,11,12,14,15,16,20,21,24,25,40,41,42,43,44)}} = \\
= SS(Q_1\cdot Q_0) \cup SD\cdot Q_1 \cup SM\cdot Q_2(Q_1 \cup Q_0)
\end{cases}
\tag{3}
$$

The logic block diagram of the pulse sequencer is shown in Fig. 6. The achieved reversible pulse sequencer is remarkable for low cost, simplicity, high-reliability and multifunctional facilities (wave drive mode, normal drive mode and half-step drive mode).

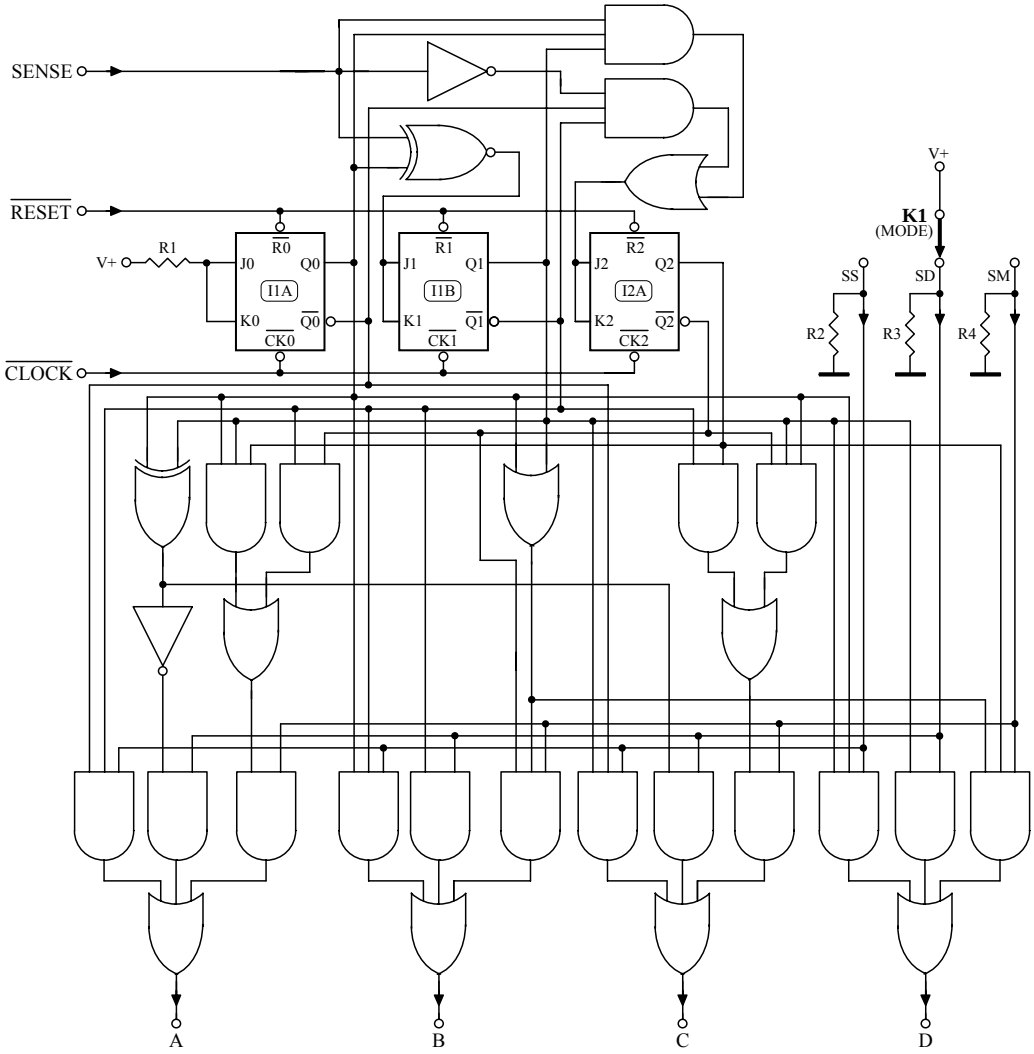

Fig. 6 Logic block diagram of the pulse sequencer.

4 Conclusion

The performances of a stepper motor are tightly connected with type and quality of the used command and supply circuits. Therefore, a high attention should be granted to the sequencer, too.

The sequencers described in this paper, which can be made with TTL integrated circuits, offer a high functioning safety. We preferred sequencers with counters instead of shift registers because of the noise behaviour (accidental external impulse) of these two types of sequencers.

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