Modeling and Simulation of Substrate Noise in Mixed-Signal Circuits Applied to a Special VCO

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Abstract: - The mixed-signal circuits with both analog and digital blocks on a single chip have wide applications in communication and RF circuits. Integrating these two blocks can cause serious problems especially in applications with fast digital circuits and high performance analog blocks. Fast switching in digital blocks generates a noise which can be introduced to analog circuits by the common substrate. This noise can decrease the performance of mixed-signal circuits; therefore, studying this noise and the way it is transmitted will lead to solutions for reducing it and improving mixed-signal circuit's performance. In this paper, an efficient model for substrate is extracted from Green's function in MATLAB environment, and its accuracy is demonstrated. Using a VCO and a multiplier as analog and digital blocks, respectively and connecting them with the proposed model of the substrate, the effects of substrate noise coupled to analog blocks are shown. Finally, some methods for reducing this noise are applied to the circuit, and the results are compared to each other. The results indicate that using P+ Guard Rings is the best method for reducing substrate noise in the mixed-signal circuits.

Key-Words: - Mixes-Signal Circuits, Substrate Noise, Green's Function, VCO, Phase Noise

1 Introduction

Nowadays, VLSI technology makes it possible to have mixed-signal circuits on a single silicon die where fast digital circuits are integrated near high performance analog blocks. Noise isolation is one of the most important problems in these circuits which can be worse as noise increases because of higher integration density and faster digital circuits [1].

Noise coupling problems are a crippling factor in many advanced circuits. Therefore, studying this noise is inevitable in order to find solutions for reducing it.
The aim of this paper is to simulate and analyze the noise transmitted through the common substrate in a mixed-signal circuit. For this purpose, first a VCO is designed to act as the analog block and then a multiplier is chosen as the high frequency digital block. The most important part of this work is modeling the substrate. Substrate should be modeled in a way that it can be used in simulators like SPICE.

After designing analog and digital blocks, substrate model can be used to illustrate the path between them. Thus, switching noise in digital circuits transfers to analog circuits through the substrate. By comparing analog block characteristics after and before relating it to digital block, noise effects can be specified. Therefore, substrate noise in real mixed-signal circuits is simulated. Some methods of reducing substrate noise are applied to the designed circuit and compared to each other.

In section 2, substrate noise and some injection and reception mechanisms are described. Some methods for modeling substrate and the one used in this paper are outlined in section 3. Section 4 discusses analog and digital blocks designed here. Analog and digital blocks are related by the substrate model in section 5, and some simulations are performed. In section 6 some substrate noise reduction methods are applied and the results are compared.

2 Substrate Coupled Noise

A silicon substrate is generally considered to provide a good isolation between devices because of its high resistance. However, in some cases, switching devices can introduce turbulence to the substrate which can be transferred to other devices because of substrate infinite resistance. Figure 1 shows two common substrates: lightly doped or P- and heavily doped or P+ [2].

Each switching node can introduce a noise to the substrate. Infinite resistance of substrate means that this noise can be transferred to adjacent devices. There are several injection and reception mechanisms, some of which are shown in Figure 2.

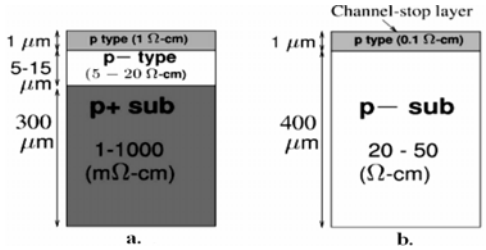
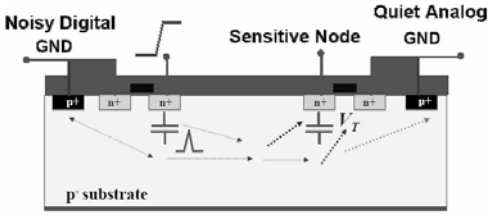


Figure 1. Common substrates for VLSI circuits: a) heavily doped substrate b) lightly doped substrate



Figuire 2. The most important noise injection and reception mechanisms

2.1 Noise Injection Mechanisms

The most important noise injection mechanism is coupling of PN junctions between devices and substrate or wells [3]. Another mechanism is the injection through digital supply lines [1].

2.2 Noise Reception Mechanisms

Junction capacitor also can cause noise reception at the presence of voltage difference between substrate and the sensitive node – mostly drain. Furthermore, threshold voltage depends on the source-body voltage, V_{bs}, so that variations on the $V_{bs,}$ caused by the noise, will cause variations in the threshold voltage. Another mechanism is through analog supply lines [1].

3 Substrate Modeling

Several methods are used for substrate modeling such as approximate methods [2,4,5,6,7] and numerical methods like Finite Element Method (FEM) [1,8] and Boundary Element Method (BEM) based on Green's Function. In this section the process of substrate modeling by using Green's Function is discussed.

3.1 Green's Function

As the resistance varies with different doping values, the substrate with several levels of doping can be modeled as a stack of parallel homogeneous layers [9]. Figure 3 shows that substrate is considered as a dielectric and is demonstrated by several layers with different dielectric constants, ε_k where k is the number of layers [10].

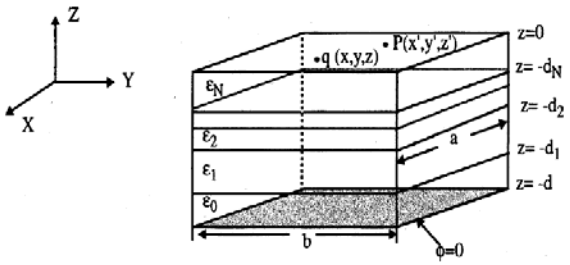


Figure 3. A cross-section of substrate [10]

In most cases, the substrate can be treated as a two layer medium: an epitaxial layer and a substrate. Contacts are placed at the top of this medium. Ground contacts, if desired, can be set at the bottom of the medium.

When the substrate is only resistant, Laplace's equation yields the following equation:

$$\nabla^2 \phi = 0 \tag{1}$$

where ϕ is the Electrostatic Potential. Using the Green theorem in (1), ϕ at an observation point, r, due to a unit current injected in source point, r', will be

$$\phi(r) = \int_S J(r')G(r,r')da \tag{2}$$

where $G(r,r')$ is the Green's Function of the substrate which fits in the substrate boundary conditions, and $J(r')$ is the source current density. Observation and source points are on the defined contacts of substrate which are planar and two dimensional; thus, the integral is on the surface [11].

There are some methods for solving the Green's Function [10, 11]. One of them is Method of Images. Obtaining the Green's Function, (2) will be solved. With discretizing each port on the substrate to small panels, a system of equations is produced which imply the relation between current and potential of each panel (current distribution in each panel is considered as constant). This can be shown in matrix form as

$$\phi = Zi \tag{3}$$

where each zij is computed from (4)

$$z_{ij} = \frac{1}{S_i S_j}\int_{S_i}\int_{S_j} G(r,r')da'da \tag{4}$$

where Si and Sj are the surface areas of panels i and j, respectively. By inverting the impedance matrix, Z, the admittance matrix is obtained. Substrate resistance between each two ports is the sum of corresponding matrix entries [11].

3.2 Method of Images

Method of images is a simple technique for demonstrating the Green's Function. In this method, point charges are distributed in the space in order to match the desired boundary conditions. Method of images can be used for dielectrics, too.

For the substrate shown in Figure 4 which has two media with different permitivities of ε_1 and ε_2 and a ground-plane, the Green's Function is obtained as [12]

$$G(x',y',x,y)=\frac{1}{4\pi\varepsilon_1}\left[\frac{1+\eta}{\sqrt{(x'-x)^2+(y'-y)^2}}+\frac{\eta^2-1}{\eta}\left[\frac{1}{2h}\ln\left(\frac{1}{1-\eta}\right)+\sum_{n=1}^{N}\left[\frac{\eta^n}{\sqrt{(x'-x)^2+(y'-y)^2+(2h)^2n^2}}-\frac{\eta^n}{2hn}\right]\right]\right] \quad (5)$$

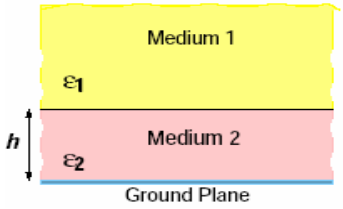


Figure 4. Two mediums with different permitivities and a ground-plane

where h is the substrate height, (x,y) is the observation point, (x',y') is the source point, N is 5 or 10 for lightly doped and heavily doped substrates, respectively and η is defined as

$$\eta=\frac{\varepsilon_1-\varepsilon_2}{\varepsilon_1+\varepsilon_2} \quad (6)$$

3.3 Obtaining Numerical Values

Considered frequency in this paper is about 2GHz. In this frequency, substrate has only resistance effects. In this paper, Green's Function is determined by method of images and the integrals are solved using numerical methods [13]. All the calculations are accomplished in MATALB. Achieved values have been compared to values presented in other papers for evaluating their accuracy.

Considering substrate as a dielectric and a uniform charge distribution on contact i, the mean potential induced to contact j is obtained as

$$\text{This } \phi_{ji}=p_{ji}q_i=\frac{q_i}{S_iS_j}\int_{S_i}\int_{S_j}G(x',y',x,y)ds_jds_i \quad (7)$$

can be rewritten in matrix form as

$$\Phi=PQ \quad (8)$$

It means that $Q=P^{-1}\Phi$ or $Q=C\Phi$. Matrix C is referred to as capacitance-coefficient matrix. Inverting matrix Z, C is obtained. From circuit theorem it is shown that

$$C_{ij}=-c_{ij},\qquad C_{ii}=c_{ii}+\sum_{k=1}^{M}c_{ik},k\neq i \quad (9)$$

Under the quasi-static approximation, the conductance G and the capacitance C between any two contacts are in the same proportion [14] as

$$G^{-1}C=\rho\varepsilon \quad (10)$$

Consequently, the resistance values will be obtained calculating and inverting G_{ii}.

3.4 Results

As discussed above, a program is written in MATLAB. Replacing variable data for substrate and contacts with those of [14] and comparing the results, the accuracy of the program is proven. Comparison is done for three different situations. First, when there is only one contact on the substrate (substrate height, 100μm and contact's dimension, 100μm*100μm). Table 1 compares the results. Second, with two contacts placed on the substrate (substrate height, 400μm and contacts' dimension, 10μm*10μm).

Figures 5 and 6 compare the value of C for different distances between contacts.

Table 1. Comparison of resistant values in [14] and the ones achieved by the program written in MATLAB for one contact

Resistance implied in [14]	342.8 Ω
Resistance achieved in MATLAB	344.1 Ω

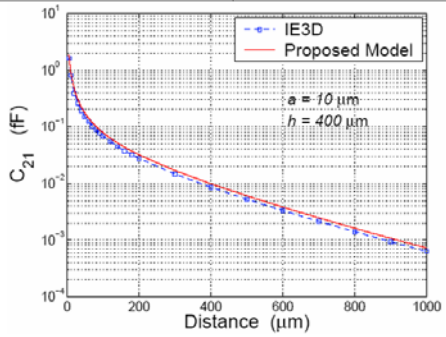


Figure 5. C values for different distances between two contacts in [14]

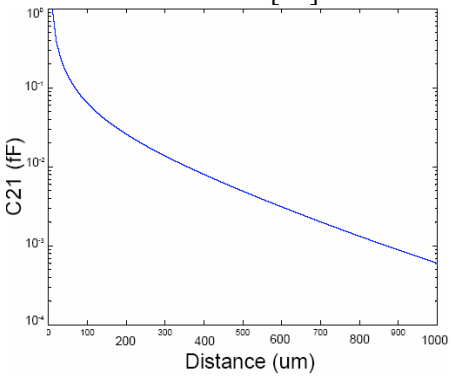


Figure 6. C values for different distances between two contacts achieved in MATLAB

Third, when there are four contacts on the substrate (substrate height, 100μm, contacts' dimension, 20μm*20μm, and distance between contacts, 100μm center to center). Table 2 compares the results.

Table 2. Comparison of resistant values in [14] and the ones achieved by the program written in MATLAB for four contacts

	R1,1	R1,2	R1,3	R1,4	R2,3	R2,4	R3,4
Resistances implied in [14] (kΩ)	2.10	70.07	523.39	2,713.02	70.35	523.91	70.07
Resistances achieved in MATLAB (kΩ)	2.13	74.33	550.57	2,581.4	74.62	550.57	74.33

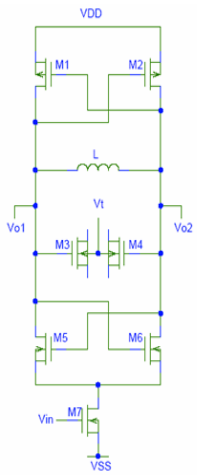
As is shown in tables 1 and 2 and figures 5 and 6, the values achieved in MATLAB are approximately equal to those implied in [14], and in the worst case the difference is about 6%. Consequently, the program written in MATLAB can be properly used for extracting resistant values needed in modeling the substrate for this paper.

4 Analog and Digital Blocks

Mixed-signal circuits have both analog and digital parts. As VCO is one of the most common analog circuits used in mixed-signal and communication circuits, it is chosen as analog block in this paper. On the other hand, a high frequency digital circuit is needed, so multiplier is an appropriate selection.

4.1 VCO

A cross-coupled VCO [15] is designed in this paper and its SPICE model is shown in figure 7. This VCO is designed so that it can oscillate at a frequency of 2GHz; its component values are shown in figure 7.



M1,M2(W/L) (μm/μm)	800/.35
M3,M4(W/L) (μm/μm)	1600/.35
M5,M6(W/L) (μm/μm)	300/.35
M7(W/L) (μm/μm)	2000/1.05
L(nH)	2
Vin(V)	1

Figure 7. Spice model and component values of the designed VCO

4.2 Multiplier

A 2*2 bit parallel multiplier is designed for this paper. 2 bit full adders are used in this design. The multiplier layout in 0.35 micron technology is shown in figure 8 which has 132 transistors. This multiplier has acceptable outputs in frequencies of 2GHz.

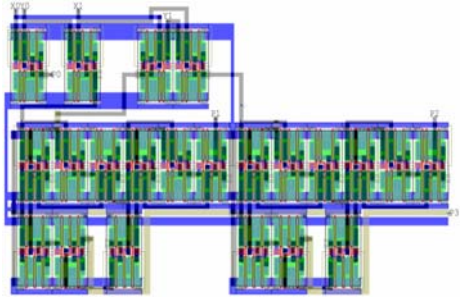


Figure 8. Layout of the designed multiplier

5 Simulations and Results

After designing analog and digital circuits and modeling the substrate in MATLAB, simulations in HSPICE are performed. Simulations are done in 0 to 30ns with 0.05ns steps. The substrate is considered as lightly-doped for this paper. Other substrate characteristics are shown in table 3. The proposed substrate model is located between substrate contacts in NMOS transistors of VCO (3 contacts) and some of NMOS transistors of multiplier (9contacts) and a contact to digital ground. Contacts' dimension is 10μm*10μm, and there is a distance of 800μm between analog and digital blocks.

Table 3. Characteristics of substrate in this paper

Permittivity(ε)	11.8 ε_0
Conductivity(ρ)	10Ω-cm
Substrate Height(h)	400μm

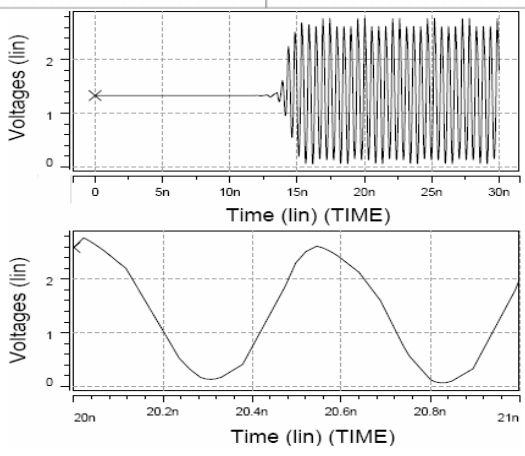


Figure 9. VCO output when multiplier inputs are 0V

Figure 9 shows the VCO output when there is no voltage applied to the multiplier inputs. After applying voltages to the multiplier inputs (figure 10), it is observed that switching in multiplier because of its input voltages will cause distortion in VCO output.

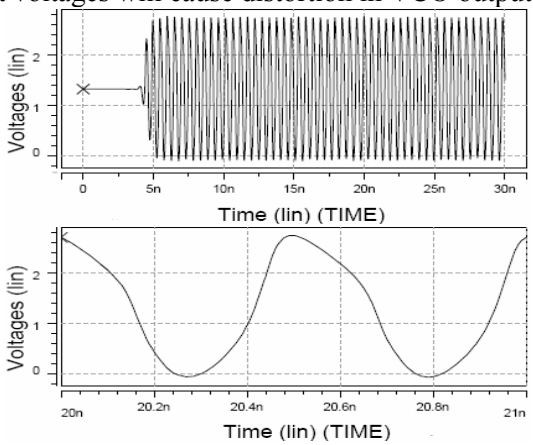


Figure 10. VCO output when voltages are applied to multiplier inputs

6 Applying noise reduction methods

There are a lot of methods for reducing substrate noise in mixed-signal circuits [3,6,7,16,17,18]. Some of these methods, namely back-plane, P+ guard ring and separation (2000µm) between analog and digital blocks are applied in this paper, and simulations are accomplished for each of them. Figure 11 shows the VCO output in 5 configurations: 1. without any input in multiplier, 2. with applying input to multiplier and without using any noise reduction method, 3. by using back-plane, 4. by separating the analog and digital blocks, and 5. by using a P+ guard ring.

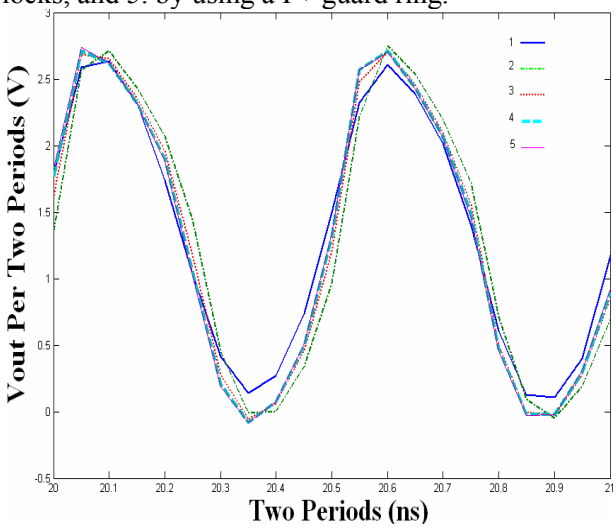


Figure 11. VCO output: 1. without any input in multiplier, 2. with applying input to multiplier and without using any noise reduction method, 3. by using back-plane, 4. by separating the analog and digital blocks, and 5. by using P+ guard ring

Figure 12 shows the VCO output noise in different situations, and Figure 13 compares these noise levels to each other.

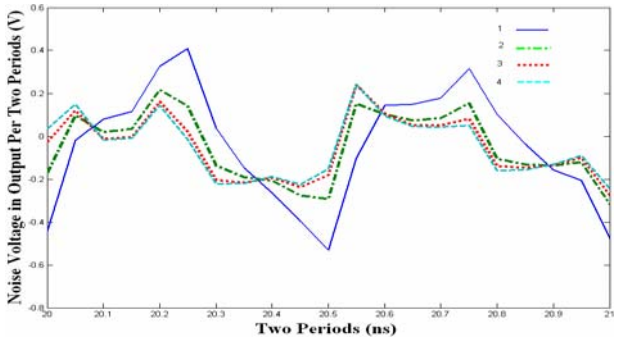


Figure 12. VCO output noise: 1. without using any noise reduction method, 2. by using back-plane, 3. by separating the analog and digital blocks, and 4. by using P+ guard ring

Phase Noise is one of the most important issues of a VCO circuit which can increase by the substrate noise. As is shown in figure 11, phase noise is at its maximum value in case 2 using no noise reduction method, but it reduces when some methods for noise reduction are applied. This is shown in figure 14.

Consequently, it is shown that using P+ guard ring has the best effect in reducing substrate noise.

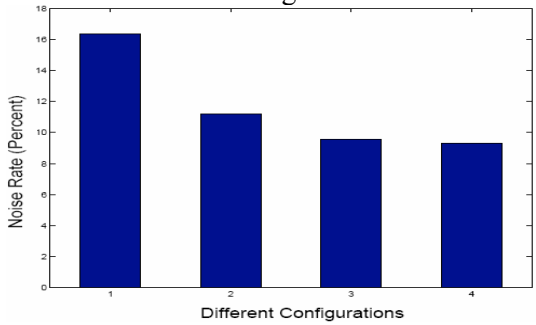


Figure 13. Comparing noise levels: 1. without using any noise reduction method, 2. by using back-plane, 3. by separating the analog and digital blocks, and 4. by using P+ guard ring

7 Conclusions

Substrate coupling is an important problem in mixed-signal circuit designs. This must be considered especially where fast digital blocks are used because fast switching noise in digital circuits is coupled to analog blocks through the common substrate, and reduces the performance.

This paper contains an applicable model, based on Green's Function, for substrate which is computed by a program written in MATLAB. This model has acceptable results for small circuits; it was shown by comparing achieved values in MATLAB by those implied in an IEEE-published paper. In this paper, analog block and digital block are a VCO and a

multiplier, respectively. Effects of switching noise in multiplier which is coupled to VCO through the proposed model for substrate are shown in the VCO output. All simulations are accomplished in HSPICE. Some methods for noise reduction are applied and their effects are compared. Results show that P+ guard ring is the best method in noise reduction. Simultaneous usage of guard rings and back-plane is suggested for obtaining the highest performance in a mixed-signal circuit.

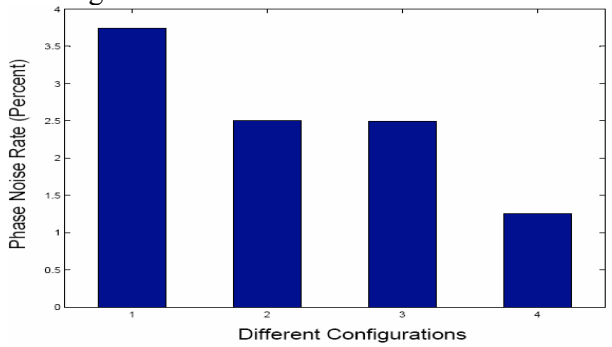


Figure 14. Comparing phase noise: 1. without using any noise reduction method, 2. by using back-plane, 3. by separating the analog and digital blocks, and 4. by using P+ guard ring

Acknowledgments

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References:

[1] Xavier Aragones, Jose Luis Gonzalez and Antonio Rubio, *Analysis and Solutions for Switching Noise Coupling in Mixed-Signal IC'S*, Kluwer Academic Publishers, 1999

[2] N. Masoumi, M. I. Elmasry, and S. Safavi-Naeini, "Fast and efficient parametric modeling of contact-to-substrate coupling," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 11, pp. 1282-1292, Nov. 2000

[3] R. Singh, "A review of substrate coupling issues and modeling strategies," *IEEE Custom Integrated Circuits Conference*, vol. 23, no. 6, pp. 491-498, 1999

[4] P. Miliozzi, L. Carloni, E. Charbon, and A. Sangiovanni-Vincentelli, "Sub-Wave: z methodology for modeling digital substrate noise injection in mixed-signal ICs," *IEEE Custom Integrated Circuits Conference*, vol. 17, no. 3, pp. 385-388, 1996

[5] S. Kristiansson, S. P. Kagganti, T. Ewert, F. Ingvarson, J. Olsson, and K. O. Jeppson, "Substrate resistance modeling for noise coupling analysis," *International Conference on Microelectronic Test Structures*, pp. 124-129, Mar. 2003

[6] K. Joardar, "A simple approach to modeling cross-talk in integrated circuits", *IEEE Journal of Solid-State Circuits*, vol. 29, no. 10, pp. 1212-1219, Oct. 1994

[7] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, pp. 420-430, Apr. 1993

[8] B. R. Stanisic, N. K. Verghese, R. A. Rutenbar, L. R. Carley, and D. J. Allstot, "Addressing substrate coupling in mixed-mode IC's: simulation and power distribution synthesis," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 3, pp. 226-238, Mar. 1994

[9] T. Smedes, N. P. van der Meijs, and A. J. van Genderen, "Extraction of circuit models for substrate cross-talk," *Proc. IEEE International Conference on CAD*, pp. 199-206, 1995

[10] R. Gharpurey and R. G. Meyer, "Modeling and Analysis of Substrate Coupling in Integrated Circuits," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 344-353, Mar. 1996

[11] N. K. Verghese, D. J. Allstot, and M. A. Wolfe, "Verification techniques for substrate coupling and their application to mixed-signal IC design," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 354-365, Mar. 1996

[12] N. Masoumi, S. Safavi-Naeini, and M. I. Elmasry, "Efficient green's function for substrate coupling modeling in VLSI circuits," *in Proceeding of International Conference on VLSI-SOC: Systems on A Chip*, Kluwer Academic Publications, pp. 152-157, Dec. 2001

[13] N. Masoumi, M. I. Elmasry, and S. Safavi-Naeini, "Modeling techniques for substrate coupling for system-on-a-chip," *The 13th International Conference on Microelectronics*, pp. 35-38, Oct. 2001

[14] N. Masoumi, M. I. Elmasry, S. Safavi-Naeini, and H. Hadi, "A novel analytical model for evaluation of substrate crosstalk in VLSI circuits," *Proceeding of the First IEEE International Workshop on Electronic Design, Test and Applications*, pp. 355-359, Jan. 2002

[15] R. Aparicio, and A. Hajimiri, "A CMOS differential noise-shifting colpitts VCO," *IEEE International Solid-State Circuits Conference*, Digest of Technical Papers, vol. 2, pp. 226-227, Feb. 2002

[16] R. J. Welch and A. T. Yang, "Substrate coupling analysis and simulation for an industrial phase-locked loop," *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 6, pp. 94-97, Jun. 1998

[17] R. Singh and S. Sali, "Substrate noise issues in mixed-signal chip designs using SPICE," *10th International Conference on Electromagnetic Compatibility*, pp. 108-112, Sep. 1997

[18] K. Makie-Fukuda, S. Maeda, T. Tsukada, and T. Matsuura, "Substrate noise reduction using active

guard band filters in mixed-signal integrated circuits," *Symposium on VLSI Circuits*, Digest of Technical Papers, pp. 33-34, 1995