Operational Amplifier with Two-Stage Gain-Boost

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Abstract: - In this paper we present a three-stage fully differential operational amplifier in 120nm digital CMOS. To reach high gain gain-boosted cascodes in the first stage are used. The gain-boost amplifiers are realized as two-stage amplifiers with self cascodes. A DC gain of 108dB and an unity-gain frequency of 1.06GHz are achieved at 1.2V supply. The operational amplifier is appropriate for supply voltages from 1.5V down to 1.0V.

Key-Words: - Operational Amplifier, Gain Boost, Self Cascode, 120nm CMOS

1 Introduction

The reduced structure size in deep-sub-µm CMOS implies some restrictions to the analog circuits. The gain of a simple amplifier stage is reduced. The useable supply voltage is limited by breakdown voltages, gate oxide reliability and / or by the available supply voltage in the system as especially in low-power mobile systems. The presented operational amplifier is designed with digital transistors and can also operate at very low supply voltages. To reduce the process steps and thereby the costs no analog options of the technology are used. The operation voltage range is down to 1V. If the gain and the bandwidth of an operational amplifier are high enough, then the behavior of the feedback circuit is given by the feedback circuits and thereby process tolerances in the amplifier have low influence on the circuit performance. The presented operational amplifier reaches high gain and high speed.

Simple gain-boost circuits control the drain-source voltage of the cascoded transistor (= input transistor) to a gate-source voltage. A gain-boost transistor is connected to the cascoded transistor so that the drain-source voltage of the cascoded transistor is the gate-source voltage of the gain-boost transistor. The drain of the gain-boost transistor is connected to a current source and to the gate of the cascode transistor. Examples of such circuits are shown in 0 and 0. So the drain-source voltage is the threshold voltage additional some overdrive voltage. Because of the high drain-source voltage this simple circuit is not suitable for low-voltage circuits.

To overcome the voltage limitation single-stage differential amplifies are used in 0 and 0. To reach sufficient output voltage range the gain-boost amplifiers are realized as folded cascodes. Level shifters are used in some circuits to overcome the voltage limitations as done in e.g. 0. All these mentioned circuits use single-stage amplifiers as gain-boost amplifiers. The differential amplifier has the advantage that the drain-source voltage can be determined directly with a reference voltage.

Two-stage amplifiers are used in 0, 0 and 0. The first stage of the gain-boost amplifier is a common-gate stage. The gate is connected to a reference voltage. This reference voltage is the same as for a conventional cascode. The source is connected to the connection of the cascode and the cascoded transistor. The drain is connected to a current source and to the second gain-boost stage. The second gain-boost stage is a simple common-source amplifier stage. The second stage drives the gate of the cascode transistor.

In the presented operational amplifier we use two-stage gain boost circuits with self-cascodes and cascodes. To get a precise control of the operating point we use a differential input stage in the gain-boost amplifiers.

2 The realisation of the operational amplifier

2.1 The concept of the operational amplifier

The main concept of the operational amplifier is shown in
Fig. 1. For simplicity the differential signal paths are only shown as single wires. All signals from input to output are differential. The compensation components of

each signal part (positive:p and negative:n) are summed

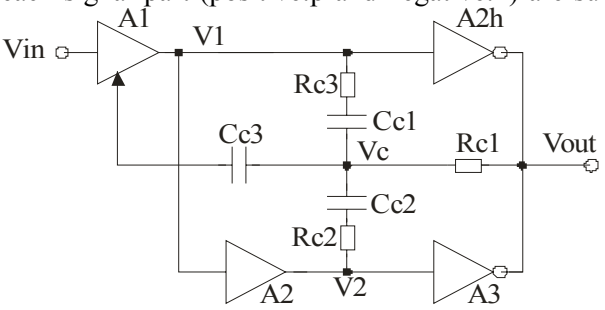

Fig. 1 Block diagram of the operational amplifier

up to one component in the block diagram e.g. the capacitor Cc3 in the block diagram is equal to Cc3p and Cc3n in the schematic of the amplifier stage A1 in **Error! Reference source not found.**.

A two-paths concept for the signal path is implemented. The amplifier stage A2h assures high-frequency performance. The amplifier stages A2 and A3 form the low-frequency path and allow high DC gain.

The three-stage concept (A1-A2-A3) has the advantage that the feedback for differential signals is also a negative feedback for common-mode. The first stage realizes most of the amplifier gain by using cascodes with gain boost.

2.2 The input stage

Fully differential circuits have the advantage that the input voltages of the operational amplifiers are near the middle of the supply voltage. So in many cases a small portion of the supply voltage is sufficient for the input voltage range. Therefore we decided to use a normal cascode circuit. If a larger input-voltage range is necessary the folded cascode would be a better choice. The input stage is realized with gain-boosted cascodes. The gain-boost amplifiers are realized with a differential input stage. The schematic of the input stage is shown in **Error! Reference source not found.**.

The current sources N5 and N7 are for stabilization of the operating point in the case of input voltages near VSS. Without the two current sources the output voltages of the first stage (V1p, V1n) would be near VDD and the common-mode controller would be saturated for low (near VSS) input voltages. The high output voltages of the first stage causes low output voltages of the operational amplifier, and by the external feedback (not in the operational amplifier) the input voltages of the operational amplifier are kept near VSS.

2.3 The gain-boost amplifiers

The gain-boost amplifiers GN and GP are realized very similarly. The schematic of the gain-boost amplifier for the N-cascode transistors is shown in Fig. 3.

The gain-boost amplifier for the P-channel cascode is realized very similar. Only the supply voltage rails and

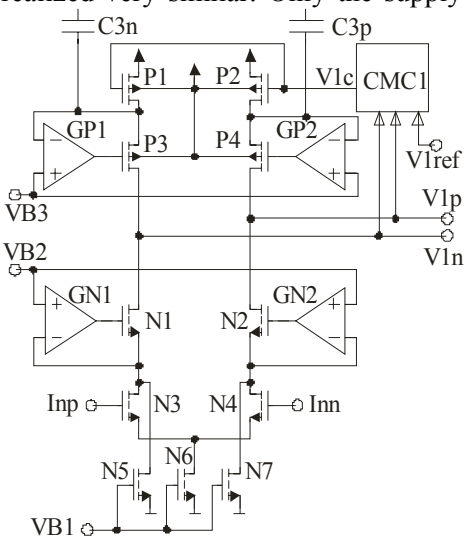

Fig. 2 Schematic of the first stage

the types of the transistors (NMOS - PMOS) are exchanged. The gain-boost amplifiers are realized with self-cascoded transistors, because with self cascodes nearly the same gain can be reached as with cascode circuits but do not need circuitry for biasing. The transistors P6, P8 and P7, P9 are the self-cascoded input transistors. The two-stage design of the gain-boost amplifier is compensated with C1 and R1. The current mirror is compensated with R2 as shown in 0 to avoid the parasitic pole at the gates of N8 to N11. The second amplifier stage overcomes the output voltage limitation of a single amplifier stage and also the additional gain is welcome. The loads N8 to N11 and P10, P11 as well as the amplifying transistors N12, N13 are cascoded or self cascoded to increase the gain of the gain-boost amplifiers.

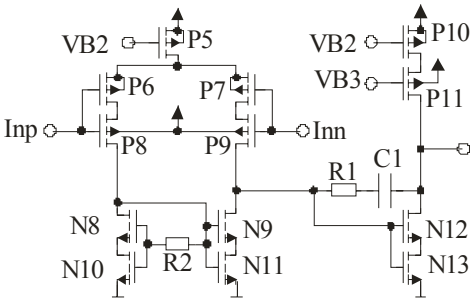

Fig. 3 Schematic of the gain-boost amplifiers GN1 and GN2

2.4 The common-mode controller CMC1

The schematic of the common-mode controller CMC1 is shown in Fig. 4. The common-mode controller is realized as split differential amplifier. At large voltages between V1p and V1n the higher voltage (nearer to

VDD) is controlled, because the input transistor with the lower voltage is switched off. This characteristic leads to the control of the minimum current in the operational amplifier output stage and creates AB behavior of the output stage. The common-mode controller is compensated with C4 to the resistor R5 of the reference voltage V1ref. This compensation reduces the gain at 1/(R5*C4) and leads to sufficient phase margin in the control loop. The compensation is explained in 0.

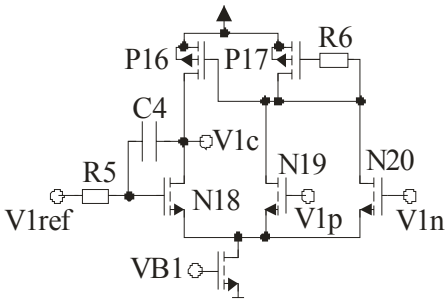

Fig. 4 Schematic of the common-mode controller CMC1

2.5 The amplifier stages A2, A2h and A3

The schematic of the amplifier stages are shown in Fig. 5. The amplifier stages A2h and A3 form the output stage of the operational amplifier. The P-channel output transistors (A2h) are driven directly from the input stage. The N-channel output transistors N16 and N17 are driven by the amplifier stage A2. The amplifier stage A1 controls the current in the P-channel output transistors. The common-mode voltage at the operational amplifier output is controlled by the common-mode controller CMC2 via the amplifier stage A2 and the N-channel output transistors. The feed-forward stage A2h has the opposite common-mode phase of the A2, A3 signal path. This common-mode cancellation improves the common-mode behavior of the operational amplifier.

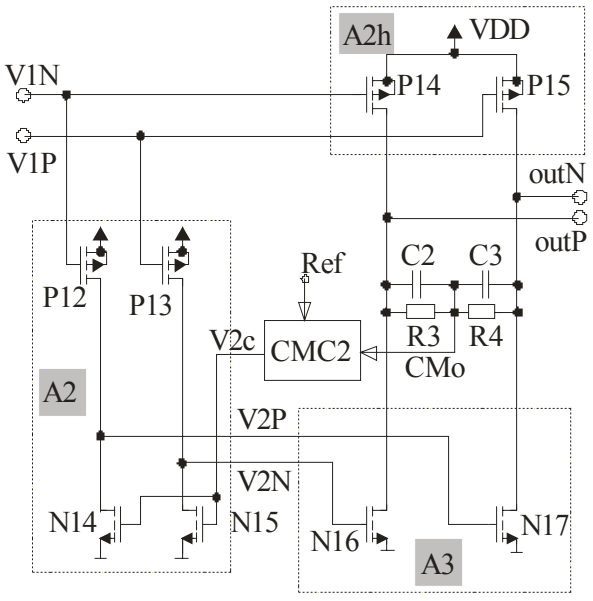

Fig. 5 Schematic of the second and the output stage

2.6 The common-mode controller CMC2

The schematic of the CMC2 is shown in Fig. 6. The common-mode controller is compensated with the capacitors C5 and C6 to the voltage divider which generates the reference voltage. If a reference voltage with low output impedance is used then a series resistance has to be used. The compensation method is the same as for CMC1.

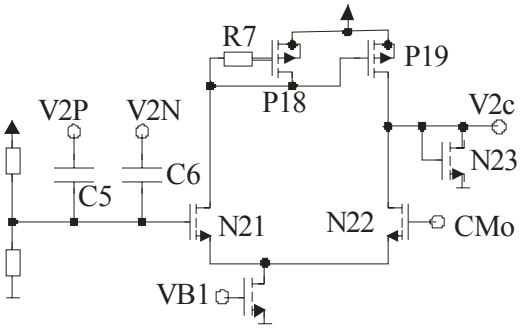

Fig. 6 Schematic of the common-mode controller CMC2

2.7 The compensation of the operational amplifier

The compensation is realized with an adopted nested Miller compensation as shown in
Fig. 1. In the compensation a common nulling resistor Rc2 is used like in 0 for single- ended three-stage operational amplifiers. The amplifier stage A2 is compensated by the R-C combination Cc2 and Rc2. The input stage A1 is compensated by the R-C combination Cc1 Rc3 and the capacitor Cc3 which is connected between Vc and the sources of the P-channel cascade transistors.

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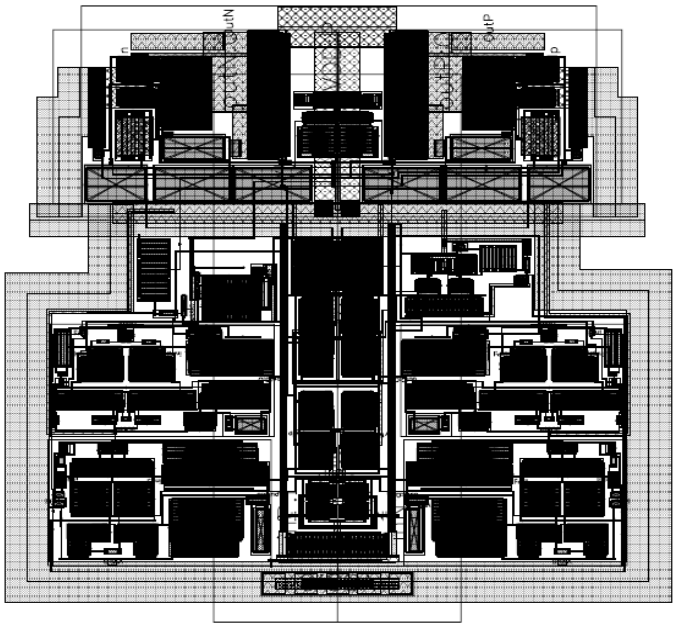


Fig. 7 Layout plot of the operational amplifier

3 Measurement results

The realized operational amplifiers were housed in dual inline packages. The DC and AC measurements were done in this housing. Because of the measurement setup limitations, the results are completed with simulation results.

3.1 DC measurement

The DC measurement shows the rail-to-rail behavior of the output stage (Fig. 8). High gain is reached over a wide supply voltage range. The measured DC gain for VDD=1.0V is 95dB, for VDD=1.2V it is 109dB and for VDD=1.5V it is 87.3dB. The degradation of the DC gain at VDD=1.5V can be corrected in a redesign to improve the definition of the operating point.

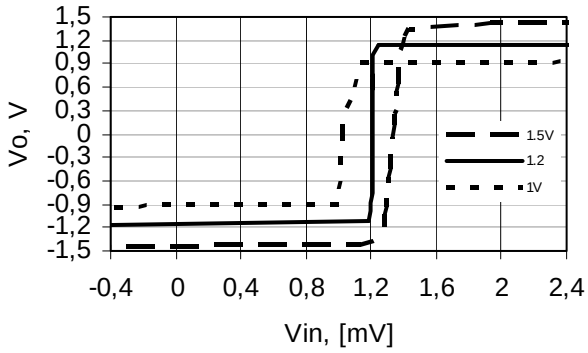


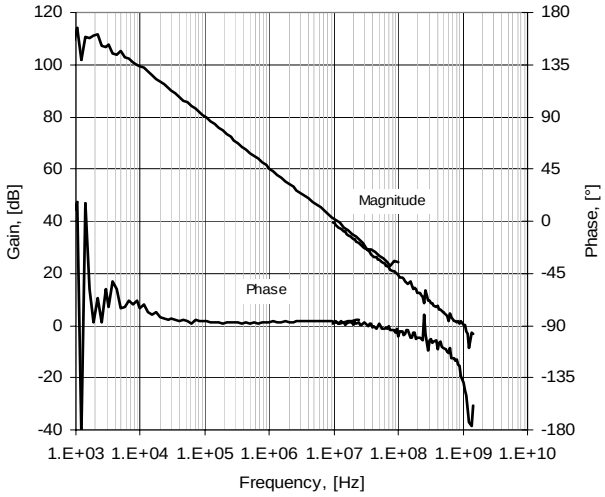
Fig. 8 DC measurement results with supply voltages of 1V, 1.2V and 1.5V

3.2 AC measurement

The AC measurement was done in two parts to overcome the frequency limitations of the network analyzers. In the frequency range from 10 Hz to 100MHz the measurement was done with the Agilent 4395A network analyzer. For the frequency range from 10MHz to 2 GHz the Agilent 8753E network analyzer was used. Both measurements show good agreement in the overlapping frequency (10MHz to 100MHz) range (Fig. 9).

Fig. 9 AC measurement result for VDD=1.2V

The measured unity-gain frequency is 1.06GHz at VDD=1.2V, whereby the phase margin is 35° for loads of 3.5pF at both outputs due to the probe heads used for the measurements and the additional capacitance (about 2pF) of the ESD protection implemented. For a capacitive load of 4pF, the phase margin is 60° according to circuit simulation. Table 1 lists additional results. Slew rate and settling time had to be simulated due to the large inductances of bond wires and package pins of the dual inline package.



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n 0 also an operational amplifier with gain-boost in the first stage is reported. This amplifier has a class A output stage and reaches simulated 80dB DC gain at 1.5V, an unity-gain frequency of 500MHz and a phase margin of 30°. In 0 we presented an operational amplifier with similar gain but with much smaller unity-gain frequency of 57MHz with 5.5pF load. Compared to the operational amplifier with a DC gain of 40dB in 0, the presented amplifier reaches a much higher gain at a comparable unity-gain frequency. In 0 a five-stage operational amplifier is shown which uses cascading to reach high gain. In this paper we demonstrate a different way to reach high gain and transit frequency with less stages in the signal path.

Technology	120nm digital CMOS
Supply voltage	1V .. 1.5V
DC gain	108dB @ 1.2V
Unity-gain frequency	1.06 GHz @ 1.2V
Phase margin	35° (3.5pF and ESD load)
Offset voltage	<1.4 mV
Power consumption	19.2mW @ 1.2V
Active area	140 µm * 140 µm
Slew rate (simulated)	863V/µs
Settling time (sin gain = 1 and 3.2	0.1%: 7.6 ns 0.01%: 14 ns
swing @ supply voltage load between outputs: 200kΩ	± 0.92 V @ 1V ± 1.16 V @ 1.2V ± 1.45 V @ 1.5V

Table 1: Summerized results

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