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Modelling analysing and feedback control of nine-level NPC PWM rectifier - clamping bridge - nine-level NPC inverter cascade

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Abstract: Voltage source multilevel inverters have become very attractive for power industries in power electronics applications during last years. The main purposes that have led to the development of the studies about multilevel inverters are the generation of output voltage signals with low harmonic distortion; the reduction of switching frequency. A serious constraint in a multilevel inverter is the capacitor voltage–balancing problem. In order to stabilize these DC voltages, we propose in this paper to study the cascade constituted by three phases nine–level PWM rectifier–filter–nine–level NPC voltage source inverter–PMSM.
In the first part, the authors present a topology of nine–level NPC VSI, then we propose a model of this converter and an optimal PWM strategy to control it using eight bipolar carriers. Then in the second part, we study a new high voltage cascade nine-level PWM current rectifier–filter–nine–level NPC VSI–PMSM. In the last part of this paper, the authors study the stability problem of the input DC voltages of the inverter. The results obtained with this solution confirm the good performances of the proposed solution, and are full of promise to use the inverter in high voltage and great power applications as electrical traction.

Key-Words: - Multilevel, inverter, rectifier, PWM, Clamping bridge, feedback, control, regulation.

1 Introduction

Multilevel are based on the neutral point clamped (NPC) inverters topology and were proposed firstly by Nabae and al [1]. Multilevel inverter structures provide an attractive solution for high power and high voltage applications. While the multilevel topology lets higher voltages using devices of lower ratings, the link DC voltage balancing problem is a serious drawback which limits the applicability of multilevel topology for motor drives. One of the major limitations of the multilevel inverters is the instability of the input DC voltages [2] [3].

The variable speed control of electrical machines has great advantages in industrial process. Mainly, it improves their static and dynamic performances. The apparition of new power components controllables in the opened and closed (GTO and IGBT) has led to the conception of new and fast converters for high power applications.

In this work, the authors study a new AC/DC/AC converter nine–level NPC PWM rectifier. It synthesis the staircase voltage waveform several levels of DC voltages.

In the first part, the knowledge model of this inverter is developed and also the used PWM strategy which requires eight bipolar carriers. After that, we clearly show up the stability problem of the eight input DC voltage sources by studying a Nine-level PWM current rectifier–Nine level NPC VSI–PMSM cascade. In the last part of this paper, we study the stability problem of the input DC voltages source inverter, For this, we propose a solution to this problem by using linear feedback loops to regulate the total DC voltages by using proportional-Integral regulator and equalising the DC link voltages in all the levels by using a clamping bridge. The results obtained with this solution shows that the proposed solution is very efficient to solve the instability problem of this multilevel inverter.

2 Modelling and control of nine-level NPC VSI

Three phases nine-level NPC VSI is a new structure of power conversion used to feed with variable frequency and voltage, a great power alternative current machine. In this paper, we study the neutral point clamping (NPC) structure (Fig.1). This

converter is constituted by three arms and eight DC voltages sources. Every arm has sixteen bi-directional switches, ten in series and six in parallel and two diodes DD_{i0} and DD_{i1} Which let to have zero voltage for V_{KM} (V_{KM} is the voltage of the phase K relatively to the middle point M) [3].

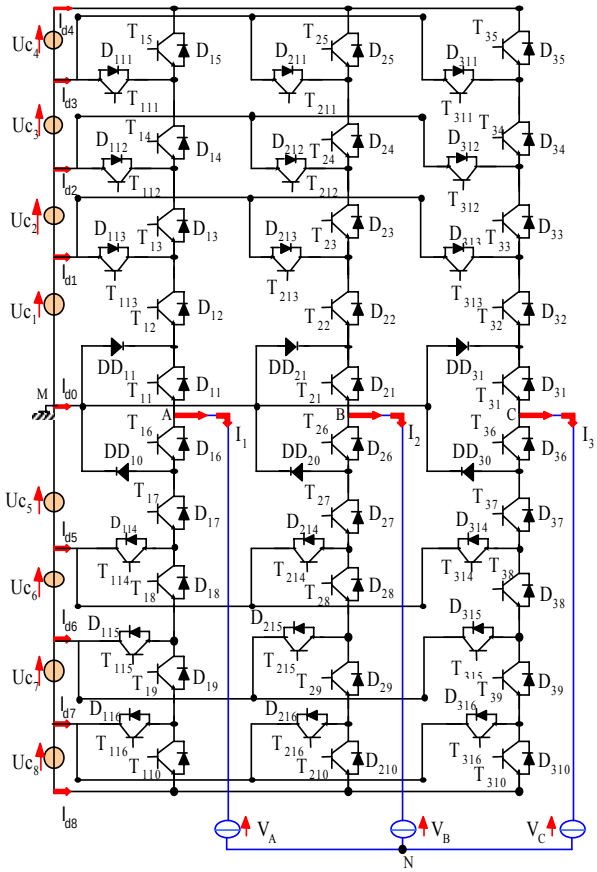

Fig.1 A nine-level NPC voltage source inverter

Several complementary laws are possible for nine-level NPC VSI. The optimal complementary law used for this converter is presented below:

$$\begin{cases} B_{i1} = \overline{B}_{i7} \\ B_{i2} = \overline{B}_{i6} \\ B_{i3} = \overline{B}_{i8} \\ B_{i4} = \overline{B}_{i9} \\ B_{i5} = \overline{B}_{i10} \end{cases} \quad (1)$$

B_{is}: control signal of the semiconductor TD_{is}

In a controllable mode using the proposed complementary law, we define for each semi-conductor TD_{is} a connection function F_{is} as fellow:

$$F_{iS} = \begin{cases} 1 & \text{if } TD_{iS} \text{ is closed} \\ 0 & \text{if } TD_{iS} \text{ is opened} \end{cases} \quad (2)$$

Where:
i: number of the arm.
s: number of the semi-conductor.

The input voltage of the inverter relatively to the middle point M, is given by the following system:

$$\begin{aligned} V_{KM} = {} & F_{i1}.F_{i2}(1-F_{i3}).U_{C1} \\ & +F_{i1}.F_{i2}.F_{i3}(1-F_{i4}).(U_{C1}+U_{C2}) \\ & +F_{i1}.F_{i2}.F_{i3}.F_{i4}(1-F_{i5}).(U_{C1}+U_{C2}+U_{C3}) \\ & +F_{i1}.F_{i2}.F_{i3}.F_{i4}.F_{i5}.(U_{C1}+U_{C2}+U_{C3}+U_{C4}) \\ & -F_{i6}.F_{i7}(1-F_{i8}).U_{C5} \\ & -F_{i6}.F_{i7}.F_{i8}(1-F_{i9}).(U_{C5}+U_{C6}) \\ & -F_{i6}.F_{i7}.F_{i8}.F_{i9}(1-F_{i10}).(U_{C5}+U_{C6}+U_{C7}) \\ & -F_{i6}.F_{i7}.F_{i8}.F_{i9}.F_{i10}.(U_{C5}+U_{C6}+U_{C7}+U_{C8}) \end{aligned} \quad (3)$$

Where k=A, B, C and i=1, 2, 3.

The system (3) shows that a nine-level NPC VSI is equivalent to eight two-level. In order to reduce the above equation and to define a control model of the converter, we define the half arm connection function F_{i1}^b and F_{i0}^b associated respectively to the upper and lower half arms.

$$\begin{cases} F_{i1}^b = F_{i11}.F_{i12}.F_{i13}.F_{i14}.F_{i15} \\ F_{i0}^b = F_{i16}.F_{i17}.F_{i18}.F_{i9}.F_{i110} \end{cases} \quad (4)$$

We define a global half arm connection function:

$$\begin{cases} F_{i1}^{bT} = F_{i13} + 2F_{i12} + 3F_{i11} + 4F_{i11}^b \\ F_{i0}^{bT} = F_{i14} + 2F_{i15} + 3F_{i16} + 4F_{i10}^b \end{cases} \quad (5)$$

When F_{i1}^{bT} equal to 0, the upper half arm is opened, and if F_{i0}^{bT} equal to 0, the lower half arm is opened too. The simple voltages of the three phases nine-level NPC VSI are given by the following system:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}.\begin{pmatrix} F_{11}^{bT} - F_{10}^{bT} \\ F_{21}^{bT} - F_{20}^{bT} \\ F_{31}^{bT} - F_{30}^{bT} \end{pmatrix} U_C \quad (6)$$

The current i_{d0} is defined by the following relation:

$$\begin{aligned} i_{d0} = {} & \left[1-\left(F_{111}+F_{112}+F_{113}+F_{114}+F_{115}+F_{116}+F_{11}^b+F_{10}^b\right)\right]i_1 \\ & +\left[1-\left(F_{211}+F_{212}+F_{213}+F_{214}+F_{215}+F_{216}+F_{21}^b+F_{20}^b\right)\right]i_2 \\ & +\left[1-\left(F_{311}+F_{312}+F_{313}+F_{314}+F_{315}+F_{316}+F_{31}^b+F_{30}^b\right)\right]i_3 \end{aligned} \quad (7)$$

2.1 Optimal PWM strategies method

Other authors have extended two-level carrier-based PMWM techniques to multilevel inverters by making the use of several triangular carrier signals and one reference signal par phase. For N-level inverter, (N-1) carriers with the same frequency f_c and same peak to peak amplitude A_c are disposed such that the bands they occupy are contiguous. The reference, or modulation, wave form has peak to peak amplitude A_m and frequency f_m, and its centred in the middle of the carrier set. The reference is continuously compared with each of the carrier

signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active corresponding to that carrier is switched off [2]. In multilevel inverters, the amplitude modulation index, m_a, and the frequency ratio, m_f, are defined as [3]

$$\begin{cases} m_a = \dfrac{A_m}{A_c} \\ m_f = \dfrac{f_c}{f_m} \end{cases} \tag{8}$$

The principle of this strategy optimal PWM which is similar to subharmonic PWM except that a zero sequence (triple harmonic) voltage is added to each of the carrier waveforms. This method takes the instantaneous average of the maximum and minimum of the three reference voltages $V_{sref} = (V_a^*, V_b^*, V_c^*)$ and subtracts this value from each of the individual reference voltages to obtain the modulation waveform [3].

The voltage V_{offset} is given by the following equation:

$$V_{offset} = \frac{[\max(V_{Sref}) + \min(V_{Sref})]}{2} \tag{9}$$

The new reference vectors are defined as follows:

$$\begin{cases} V_{aref}^* = V_a^* - V_{offset} \\ V_{bref}^* = V_b^* - V_{offset} \\ V_{cref}^* = V_c^* - V_{offset} \end{cases} \tag{10}$$

In this parts, the different DC input voltages of the inverter are supposed constant and equals $Uc_{i(i=1\div8)}$=Uc.

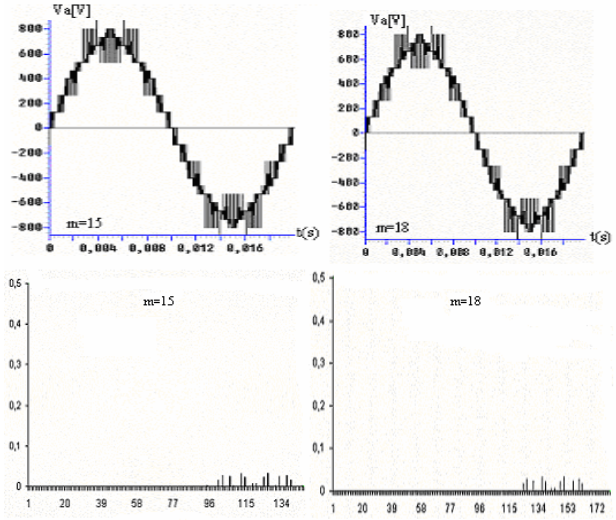

Fig.2. Optimal PWM strategy of the nine-level NPC VSI (simple and spectrum voltage)

Figure 2 represents the simple output voltage of the nine-level NPC VSI controlled by the proposed PWM strategy for m=15,18 and r=0.9. We note that, for even values of m, the output voltage present symmetry relatively to the quarter of the period. Then, only odd harmonics exist. But for odd values of m, the output voltages don't present any symmetry relatively to the quarter of the period. Then, all harmonics (even and odd) exist. They together by families centred around frequencies multiple of 8mf.

3 Permanent magnet synchronous machine drive

The Park model of the permanent magnet synchronous machine, with P pairs of poles, is defined by the following equations system.

$$\begin{bmatrix} V_{ds} \\ V_{qs} \end{bmatrix} = \begin{bmatrix} R & -L_q.\omega \\ L_d.\omega & R \end{bmatrix} \begin{bmatrix} I_{ds} \\ I_{qs} \end{bmatrix} + \begin{bmatrix} L_d & 0 \\ 0 & L_q \end{bmatrix} \frac{d}{dt} \begin{bmatrix} I_{ds} \\ I_{qs} \end{bmatrix} + \omega\Phi_f \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tag{11}$$

The electromagnetic torque is given by the following expression.

$$T_{em} = P\left[\Phi_d I_{qs} - \Phi_q I_{ds}\right] = P\left[\left(L_d - L_q\right) I_{ds} + \Phi_f\right] I_{qs} \tag{12}$$

The control strategy often used consists to maintain the current i_{ds} to zero, and to control the speed by the current i_{qs} via the voltage V_{qs}. Regulating the current i_{ds} to zero lets have, for a given stator currents magnitude, a maximum torque. In this paper, we use the algorithm i_{ds}=0 [4].

4 Nine-level PWM rectifier-nine-level NPC-VSI-PMSM cascade

Until now, we have supposed the input DC voltages of nine–level NPC VSI constants. In this part, we study a generation input DC voltages manner. For this, we propose a cascade constituted by nine-level PWM rectifier-filter-nine-level inverter-PMSM. This cascade lets to absorb, in network, sinusoidal input currents with unity power factor.

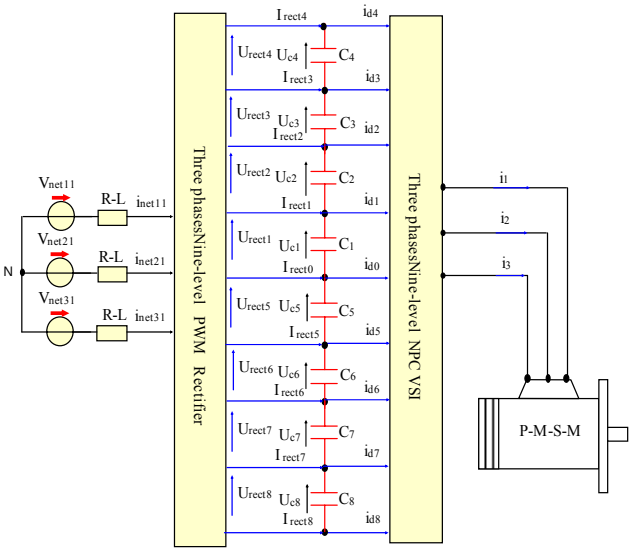

Fig.3. Nine-level PWM rectifier-filter-nine-level NPC VSI-PMSM cascade

4.1 Simulation results

We note the instability of the output voltages (fig.4). The upper input DC voltages of the inverter $U_{ci(i=1\div8)}$ are practically not equals to the lower one. This fact accentuates the problem of unbalance of different input DC voltages sources of nine-level NPC VSI.

Figure 4 shows that the different input voltages of the VSI are not equals by pairs ($U_{c1}\neq U_{c5}$, $U_{c2}\neq U_{c6}$, $U_{c3}\neq U_{c7}$ and $U_{c4}\neq U_{c8}$) but their differences (U_{c1}-U_{c5}, U_{c2}-U_{c6}, U_{c3}-U_{c7} and U_{c4}-U_{c8}) are weak.

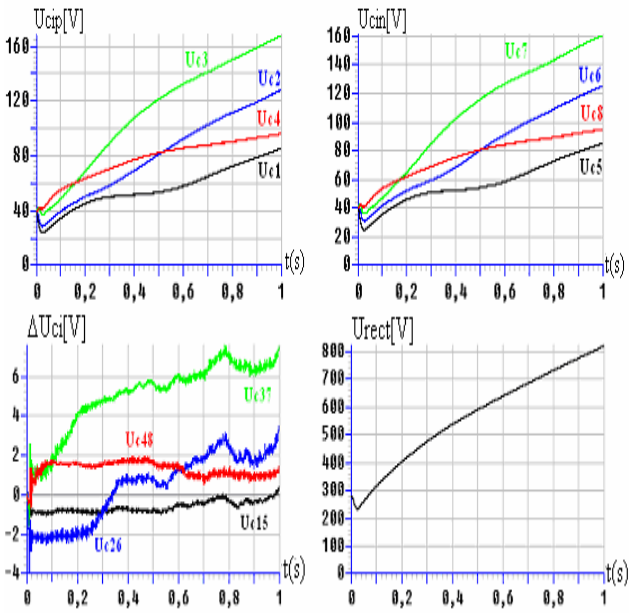

Fig.4.The different input and output DC voltages source intermediate of the nine-level PWM rectifier

5 Regulation of input DC voltages of multilevel NPC inverter

To remedy to the problem of the instability of output DC voltages of the PWM rectifier [6], we propose to use a clamping bridge and regulation of these voltages [7].

5.1 Modelling and control of clamping bridge

The clamping bridge cell is a simple circuit constituted by a transistor and a resistor in series linked in parallel with capacitor (fig.5). The transistors are controlled in order to maintain the different voltages equal [5] [7].

The model of the intermediate filter is defined by the following equation:

$$C_i \frac{dUci}{dt} = Irecti + ir_{(i+1)} + ic_{(i+1)} - idi - iri \qquad (13)$$

With

$$ir_i = Ti.\ \frac{Uci}{Rpi} \qquad (14)$$

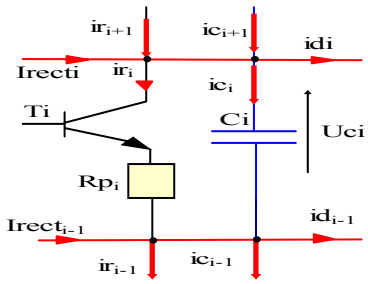

Fig.5. Clamping bridge cell

5.2 DC link and current controller with using PI regulator

In this part, we propose to enslave the input DC voltages of multilevel inverter by using feedback linear control as shown in figure 6. The synoptic diagram of nine-level PWM current rectifier control is given in figure 6. As we can see on this scheme, this control is composed by two loops [3] [8]. The first is the network current I_{neti} The second one concerns the voltage loop control of the voltage U_{cm}.

5.2.1 Current controllers

Each phase k(k=1,2 or 3) of three phases network feeding the rectifier can be represented by a R_s, L_s circuit (fig.7) [3] [7] [8].

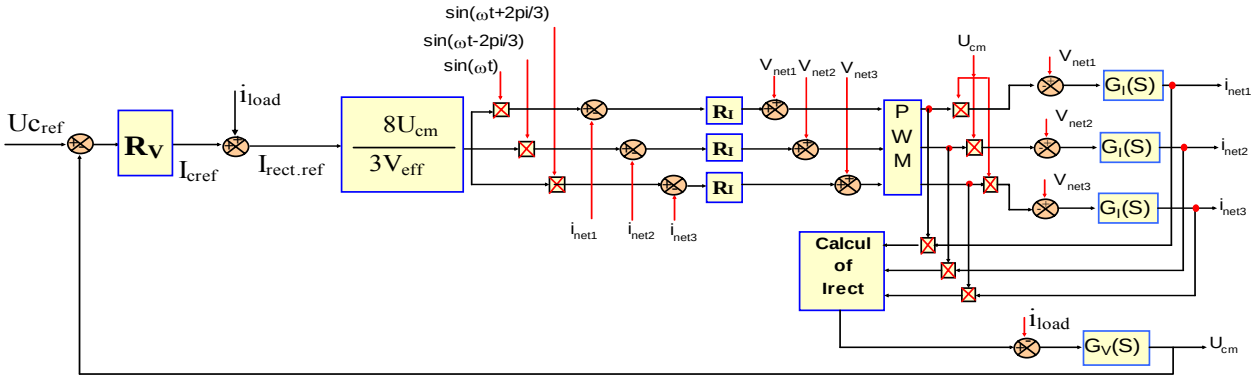

Fig.6. Synoptic diagram of the nine-level PWM rectifier

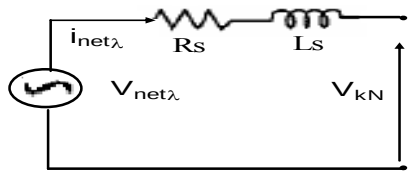

Fig.7. Equivalent circuit of a rectifier phase

We control the network current of the phase 1,2 and 3 by proportional- Integral regulator [3,8]. The algorithm of this current loop is given in figure 8. In this scheme, the transfer function $G_I(S)$ is expressed as follows:

$$G_I(S) = \frac{I_{net\lambda}}{V_{net\lambda}} = \frac{\frac{1}{R_S}}{1 + \frac{L_S}{R_S}.S} \qquad (15)$$

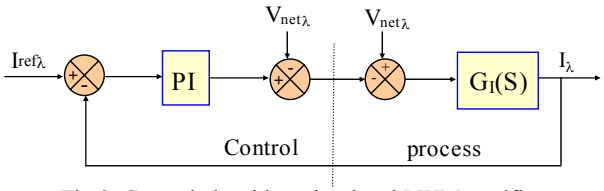

Fig.8. Control algorithm nine-level PWM rectifier of network current

5.2.2 DC Voltage control loop

The modelling of this loop is based on the instantaneous power conservation principle with no loss hypothesis. This loop imposes efficient network reference current [3] [5] [7] [8].

Input power and output power:

$$P_e = \sum_{\lambda=1}^{3}(V_{net\lambda} i_{net\lambda} - R_S . i_{net\lambda}^2 - \frac{L_S}{2}.\frac{di_{net\lambda}^2}{dt}) \qquad (16)$$

$$P_s = \sum_{i=1}^{8}(U_{recti}\ I_{recti}) = (N-1) U_{cm} (i_c + i_{load}) \qquad (17)$$

Using of the power conservation principle and neglecting Joule losses and assuming sinusoidal grid currents, we get:

$$3V_{eff}\ I_{eff} = (N-1).U_{cm} (i_c + i_{load}) \qquad (18)$$

We use a regulator PI for voltage. The general principle enslavement of nine-level rectifier is given by figure 9.

5.3 Application of feedback control algorithm of rectifier for the proposed cascade

We practice the algorithm enslavement elaborate previously (fig.9) to control the rectifier of the cascade. We note that, the output voltage of PWM rectifier follows perfectly its reference which is constant (fig.10). The different input DC voltages of the NPC VSI are constant and practically equal by pairs too (fig.11). In consequence the output voltage of the nine-level NPC VSI is symmetrical. The inverter current i_{d0} and the rectifier current I_{rect0} have a mean value practically null (fig.12). The network currents i_{neti} feeding rectifier follow perfectly their sinusoidal references (fig.13).The network voltage and current are in phases then the power factor of network is uniting (fig.13).

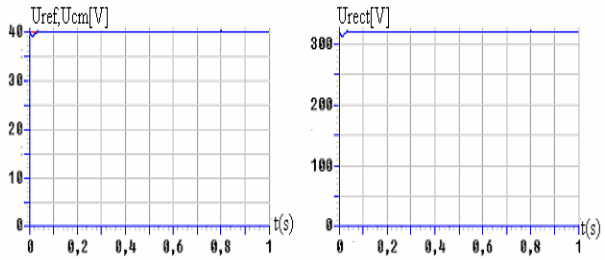

Fig.10. Output voltage of nine-level PWM rectifier and its reference

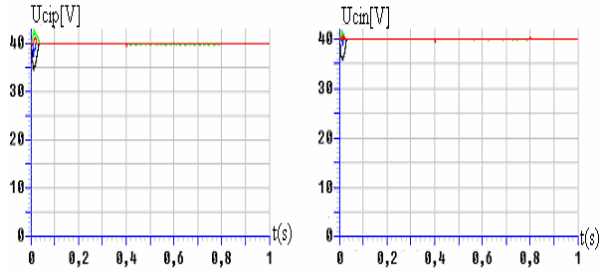

Fig.11. Output DC voltages of nine-level PWM rectifier

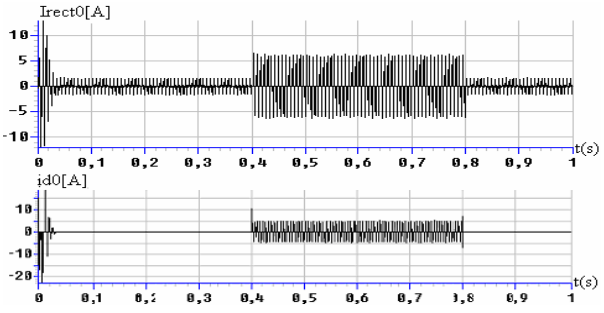

Fig.12. The inverter middle input current i_{d0} and rectifier output current I_{rect0}

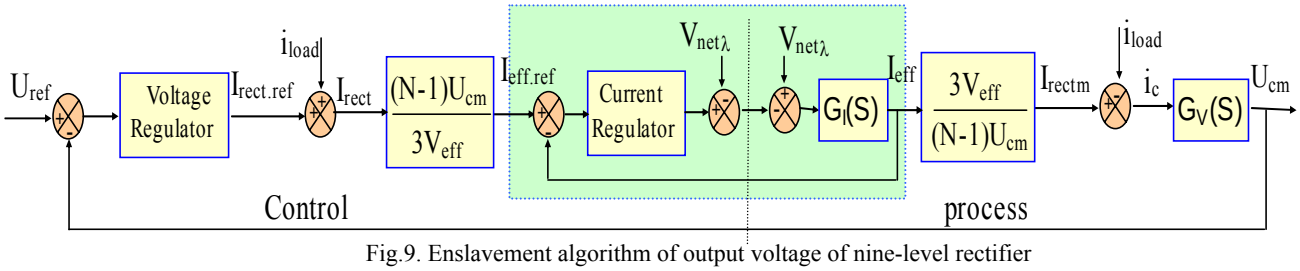

Fig.9. Enslavement algorithm of output voltage of nine-level rectifier

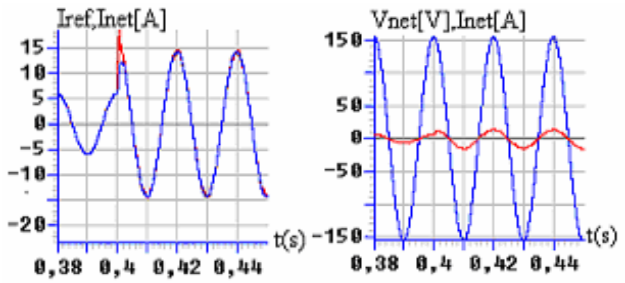

Fig.13. The network currents I_{net}, its reference and his voltage V_{net}

The performances of the speed control algorithm of the PMSM (fig.14) show that the current of the machine is sinusoidal, where as the output voltage of the inverter is nearly sinusoidal. The PMSM is drived using vector control with direct current reference null.

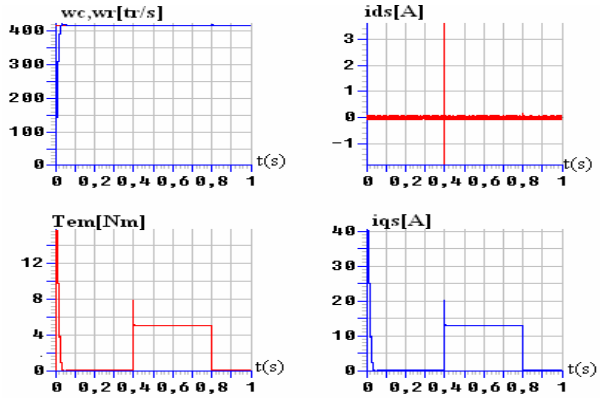

Fig.14. The PMSM performances fed by nine-Level NPC inverter Cascade

6 Conclusion

In this paper, we have studied the stability problem of the input voltages of the nine-level NPC VSI. The modelling of the nine-level NPC inverter shows that is equivalent to eight two-level inverters in series. The study of the stability problem of the input DC voltages of nine-level NPC VSI shows that the different input voltages of this VSI are not stables and their differences are not equals and different of zero. To solve this problem, we propose to use clamping bridge, because this bridge allows to improve the input voltage of nine-level inverter. In spite of this solution, the output voltages of rectifiers are not constants. To remedy to this problem, we propose the feedback linear control of the input voltages of the nine-level.

The application of the proposed feedback control algorithm to the rectifiers of the studied cascade shows a good following of the output voltages of this rectifier to this reference. Then, they are more stables. The cascade studied absorbs network currents with minimum harmonics and unity power factor. The results obtained shows that the proposed solution is very efficient to solve the instability problem of the multilevel inverter.

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