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Control and Enslavement of Input DC Voltages of multilevel NPC inverter cascade

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Abstract- This paper describes the control and enslavement of input DC voltages of nine-level NPC voltage source inverter. The analysis and simulation of a cascade constituted by three phase's three-level PWM rectifier-nine levels NPC voltage source inverter (VSI). This cascade is used to feed a permanent magnet synchronous machine with a speed control. In the first part, the authors present the speed control of the permanent magnet synchronous machine (PMSM) by using the field oriented control. Then, in the second part, we study the three-level PWM rectifier controlled by hysteresis strategy. After, we present a topology of nine levels NPC VSI for then they propose a model of this inverter and the PWM strategy which uses eight bipolar carriers to control it. The study of this cascade shows that the input DC voltages of the inverter are not stable and not equals. To remedy to this problem, the authors propose to introduce in the cascade a clamping bridge and regulation using PI regulator. The use of this strategy has let to stabilize the input DC voltages. The results obtained are full of promise to use the inverter in high voltage and great power applications as electrical traction.

Key-Words: - NPC inverter, clamping bridge, rectifier multilevel, current hysteresis, PWM strategy, input DC voltages, power factor unit, regulation.

1 Introduction

The apparition of new power components controllable in the opened and closed states (GTO and IGBT) has let to the conception of new and fast converters for high power applications. Thus, the speed variator (static converter-AC machines) has seen its cost decreasing considerably. The progress accomplished in the micro-computer tools has let the synthesis of more performant and robust control algorithms for sets of converter-machine [1]. The authors propose a new cascade constituted by three-level PWM rectifiers-nine-level NPC VSI. The performances of this cascade show the instability problem of the input DC voltages of the inverter. As solution to this problem, the authors propose the introduction of a clamping bridge and regulation of the input DC voltages of multilevel NPC inverter structure using PI regulator. This cascade lets to absorb, in network, sinusoidal currents with unity power factor. The results obtained confirm the good performances of the proposed solution. This cascade can find applications in high voltage and field's great power [1,2].

2 Permanent magnet synchronous machine drive

The Park model of the permanent magnet synchronous machine, with P pairs of poles, is defined by the following equations system [2].

$$\begin{bmatrix} V_{ds} \\ V_{qs} \end{bmatrix} = \begin{bmatrix} Rs & -L_q\omega \\ L_d\omega & Rs \end{bmatrix} \begin{bmatrix} I_{ds} \\ I_{qs} \end{bmatrix} + \begin{bmatrix} L_d & 0 \\ 0 & L_q \end{bmatrix} \frac{d}{dt} \begin{bmatrix} I_{ds} \\ I_{qs} \end{bmatrix} + \omega\Phi_f \begin{bmatrix} 0 \\ 1 \end{bmatrix} \quad (1)$$

The control strategy often used consists to maintain the current i_{ds} to zero, and to control the speed by the current i_{qs} via the voltage V_{qs}. In this paper, we use the algorithm i_{ds}=0 (fig.1) [3,4].

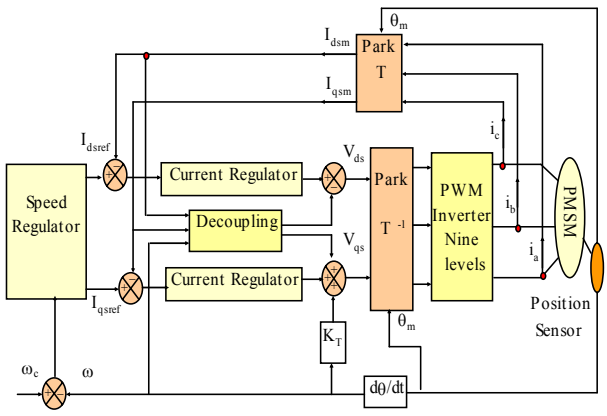

Fig.1. The speed control using the algorithm ids=0

3 Modelling and control of three-level PWM rectifier

The advantages of three-level Voltage Source Inverter topology (fig.2) are well known and have been applied in medium and high power applications in the last years [5]. The reduction of switching frequency and the increasing of the voltage supported by each device are very attractive features.

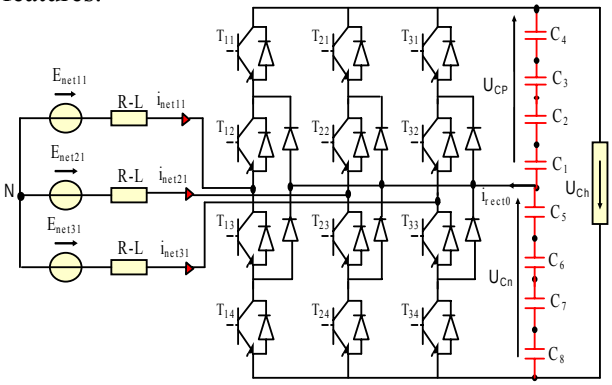

Fig.2. Three-level VSI converter topology

3.1 Modelling of three-level PWM rectifier

The reversibility of the three-level source inverter allows it to work as current rectifier [5,6]. The optimal control of this rectifier is:

$$\begin{cases} B_{i3} = \overline{B}_{i2} \\ B_{i4} = \overline{B}_{i1} \end{cases} \quad (2)$$

With i=1,2 and 3.

The input voltages of three-level PWM rectifier are defined as follow:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\left\{\begin{bmatrix} F^b_{11} \\ F^b_{21} \\ F^b_{31} \end{bmatrix} U_{rect1} - \begin{bmatrix} F^b_{10} \\ F^b_{20} \\ F^b_{30} \end{bmatrix} U_{rect2}\right\} \quad (3)$$

The rectifier output current is given as follows:

$$\begin{cases} irect1 = F^b_{11}.i_{net1} + F^b_{21}.i_{net2} + F^b_{31}.i_{net3} \\ irect2 = F^b_{10}.i_{net1} + F^b_{20}.i_{net2} + F^b_{30}.i_{net3} \end{cases} \quad (4)$$

With: $i_{rect0} = -(i_{rect1} + i_{rect2})$

3.2 Double Hysteresis-Band Current Control

The basic principle of the double hysteresis-band current control is based on the classical hysteresis control applied to conventional two-level inverters. We define two hysteresis bands (Upper and Lower Commutation Bands) around the current reference [4,5,6]. The hysteresis bands are actually super imposed but to differentiate them, they will be named as Upper and Lower band [5].

4 Modelling and control of nine-level NPC VSI

The three phases nine levels NPC VSI is a new structure of power conversion used to feed with variable frequency and voltage, a great power alternative current machine. Several structures are possible for nine level inverters. In this paper, we study the neutral point clamping (NPC) structure (Fig.3) [5]. This structure is constituted by three arms and eight DC voltages sources. Every arm has sixteen bi-directional switches, ten in series and six in parallel and two diodes DD_{i0} and DD_{i1} Which let to have zero voltage for V_{kM} (V_{KM} is the voltage of the phase K relatively to the middle point M) [6,7].

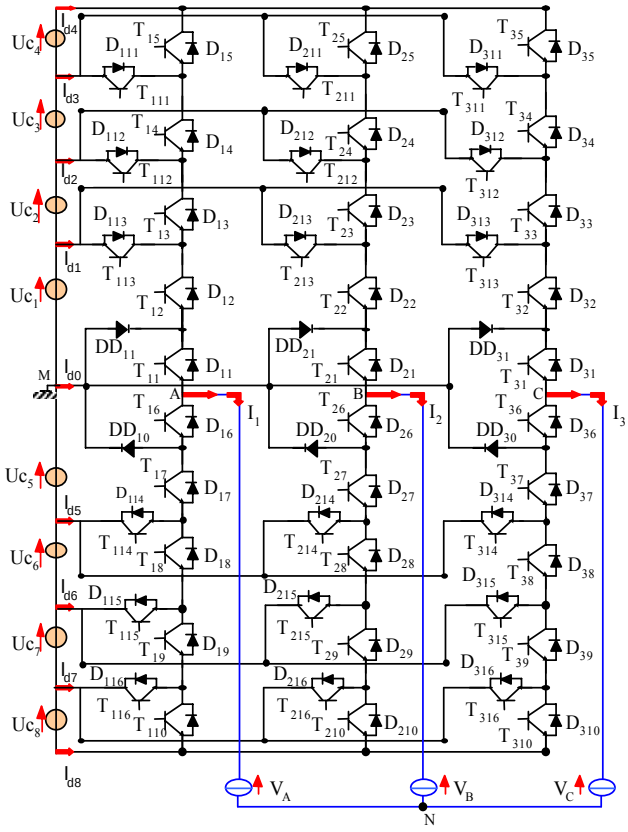

Fig.3. A nine-level NPC voltage source inverter structure

4.1 A working model

Several complementary laws are possible for nine-level NPC VSI. The optimal complementary law used for this converter is presented below:

$$\begin{cases} B_{i1} = \overline{B}_{i7} \\ B_{i2} = \overline{B}_{i6} \\ B_{i3} = \overline{B}_{i8} \\ B_{i4} = \overline{B}_{i9} \\ B_{i5} = \overline{B}_{i10} \end{cases} \quad (5)$$

B_{is}: control signal of the semiconductor TD_{is}.

4.2 Knowledge model

In a controllable mode using the proposed complementary law, we define for each semi-conductor TD_{is} a connection function F_{is} as fellow [6]:

$$F_{iS} = \begin{cases} 1 & \text{if } TD_{iS} \text{ is closed} \\ 0 & \text{if } TD_{iS} \text{ is opened} \end{cases} \quad (6)$$

(i: number of the arm and **s**: number of the semi-conductor).

The input voltage of the inverter, relatively to the middle point M, is given by the following system:

$$\begin{aligned} V_{KM} = {} & F_{i1}.F_{i2}(1-F_{i3}).U_{C1} \\ & +F_{i1}.F_{i2}.F_{i3}(1-F_{i4}).(U_{C1}+U_{C2}) \\ & +F_{i1}.F_{i2}.F_{i3}.F_{i4}(1-F_{i5}).(U_{C1}+U_{C2}+U_{C3}) \\ & +F_{i1}.F_{i2}.F_{i3}.F_{i4}.F_{i5}.(U_{C1}+U_{C2}+U_{C3}+U_{C4}) \\ & -F_{i6}.F_{i7}(1-F_{i8}).U_{C5} \\ & -F_{i6}.F_{i7}.F_{i8}(1-F_{i9}).(U_{C5}+U_{C6}) \\ & -F_{i6}.F_{i7}.F_{i8}.F_{i9}(1-F_{i10}).(U_{C5}+U_{C6}+U_{C7}) \\ & -F_{i6}.F_{i7}.F_{i8}.F_{i9}.F_{i10}.(U_{C5}+U_{C6}+U_{C7}+U_{C8}) \end{aligned} \quad (7)$$

Where k=A,B,C and respectively i=1,2,3.

The system (7) shows that a nine-level NPC VSI is equivalent to eight two-level or four three-level or two five-level NPC VSI in series.

In order to reduce the above equation and define a control model of the converter, we define the half arm connection function F_{i1}^{b} and F_{i0}^{b} associated respectively to the upper and lower half arms.

$$\begin{cases} F_{i1}^{b} = F_{i11}.F_{i12}.F_{i13}.F_{i14}.F_{i15} \\ F_{i0}^{b} = F_{i16}.F_{i17}.F_{i18}.F_{i9}.F_{i110} \end{cases} \quad (8)$$

We define a global half arm connection function:

$$\begin{cases} F_{i1}^{bT} = F_{i13} + 2F_{i12} + 3F_{i11} + 4F_{i11}^{b} \\ F_{i0}^{bT} = F_{i14} + 2F_{i15} + 3F_{i16} + 4F_{i10}^{b} \end{cases} \quad (9)$$

The simple voltages of the three phases nine-level NPC VSI are given by the following system:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{pmatrix} F_{11}^{bT} - F_{10}^{bT} \\ F_{21}^{bT} - F_{20}^{bT} \\ F_{31}^{bT} - F_{30}^{bT} \end{pmatrix} U_C \quad (10)$$

The input current i_{d0} of the inverter are given as follow:

$$\begin{aligned} i_{d0} = {} & \left[1-\left(F_{111}+F_{112}+F_{113}+F_{114}+F_{115}+F_{116}+F_{11}^{b}+F_{10}^{b}\right)\right]i_1 \\ & +\left[1-\left(F_{211}+F_{212}+F_{213}+F_{214}+F_{215}+F_{216}+F_{21}^{b}+F_{20}^{b}\right)\right]i_2 \\ & +\left[1-\left(F_{311}+F_{312}+F_{313}+F_{314}+F_{315}+F_{316}+F_{31}^{b}+F_{30}^{b}\right)\right]i_3 \end{aligned} \quad (11)$$

4.3 PWM strategies

In this part, we present one PWM algorithm of nine-level NPC voltage source inverter.

Figure 4 represents the simple output voltage of nine-level NPC VSI controlled by the proposed PWM strategy with eight bipolar carriers for m=15, 18 and r=0.9 [7]. We notice that, for even values of m, the simple output voltage has symmetry relatively to the quarter of the period, and we have only odd harmonics. But for odd values of m, we have no symmetry, and then even and odd harmonics exist (fig.4). The voltage harmonics gather by families centred around frequencies multiple of 8mf (fig.4). The adjusting characteristic is linear from r=0 to r_{max}=1 and the harmonics rate decreases when r increases (fig5).

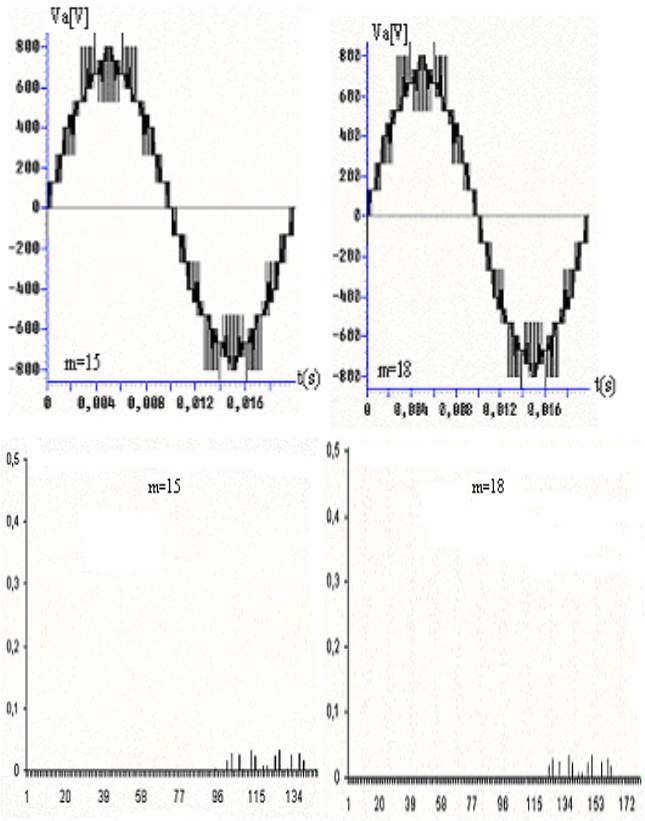

Fig.4. PWM strategy of nine-level NPC VSI (simple and spectrum voltage)

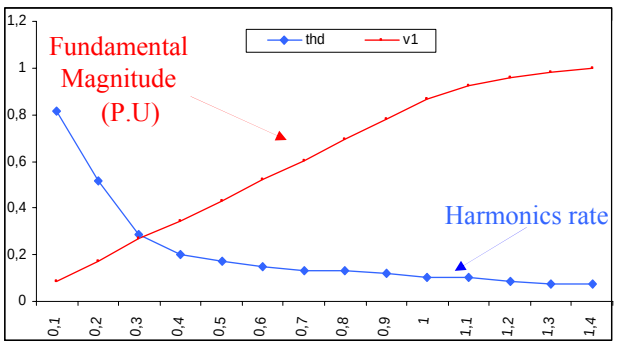

Fig.5. Adjusting characteristic of output voltage m=15

5 Three-level PWM rectifier-nine-level NPC VSI-PMSM cascade

Until now, we have supposed the input DC voltages of nine-level NPC VSI constants. In this part, the authors study a generation input DC voltages manner. For these we propose a cascade presented in the figure 6. This cascade is constituted by a three-level PWM rectifier-filter-nine-level inverter-PMSM.

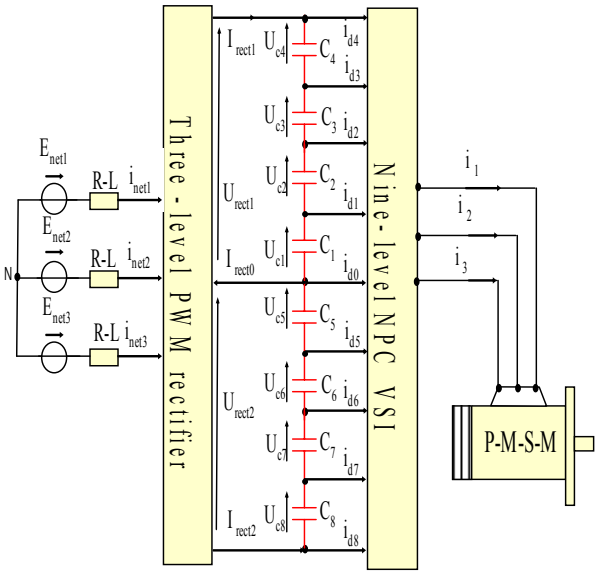

Fig.6. Three level PWM rectifier-filter-nine-level NPC VSI-PMSM cascade

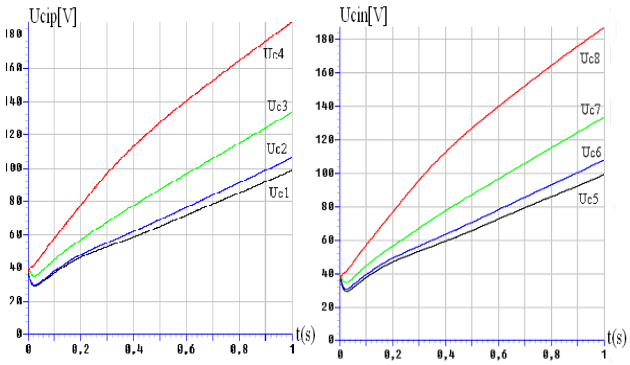

Fig.7. The different input DC voltage source intermediate

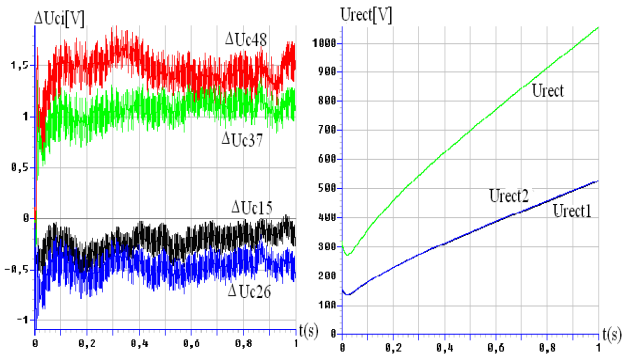

Fig.8. Difference ΔU_{Ci} of different input DC voltages and Output DC voltages of three-level PWM rectifier

We note the instability of the output voltage (fig.7). The upper input DC voltages of the inverter $Uci_{(i=1\div8)}$ are practically not equals to the lower one. This fact accentuates the problem of unbalance of the different input DC voltages sources of nine-level NPC VSI.

Figure 8 shows that the different input voltages of the VSI are not equals by pairs and their differences are weak. We note the instability of the output voltage of three-level PWM rectifier (fig.8).

6 Enslavement of input DC voltages of multilevel NPC inverter

To remedy to the problem of the instability of the output DC voltage of the PWM rectifier [7,8], we propose to use a clamping bridge, and regulation of the input DC voltages of multilevel inverter.

6.1 Modelling and control of clamping bridge

The clamping bridge cell is a simple circuit constituted by a transistor and a resistor in series connected in parallel of capacitor as shown in figure 9. The transistors are controlled in order to maintain an equality of the different voltages.

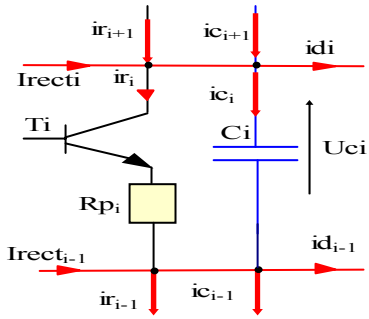

Fig.9. The clamping bridge cell

In this part, the model of intermediate filter with clamping bridge is defined by following equation:

$$C_i \frac{dUci}{dt} = Irecti + ir_{(i+1)} + ic_{(i+1)} - idi - iri \qquad (12)$$

With:

$$ir_i = Ti.\frac{Uci}{Rpi} \qquad (13)$$

6.2 DC link voltage controller

In the second part, we propose to enslave it using integrator-proportional regulator. We have observed that the application of the enslavement algorithm for a cascade constituted by three-level PWM rectifier-clamping bridge-nine levels NPC VSI.

The modelling of this loop is based on the instantaneous power conservation principle with no loss hypothesis. This loop imposes efficient network current [9].
Input and output power:

$$\begin{cases} P_e = \sum_{k=1}^{3} (V_{netk} i_{netk} - R\, i_{netk}^2 - \frac{L}{2}\frac{di_{netk}^2}{dt}) \\ P_s = \sum_{i=1}^{2} (U_{recti} I_{recti}) = 2.U_{cm}(i_c + i_{load}) \end{cases} \quad (14)$$

We define the different grandeurs, I_{rectm}, i_{load}, i_c and U_{cm} as follow:

$$\begin{cases} i_C = \frac{i_{c1} + i_{c2}}{2} \\ i_{load} = \frac{i_{load1} + i_{load2}}{2} \\ U_{cm} = \frac{U_{rect1} + U_{rect2}}{2} \\ i_{rectm} = i_{load} + i_C \end{cases} \quad (15)$$

Using of the power conservation principle and neglecting joules loss in the resistor R, we suppose the network currents sinusoids and in phase with corresponding voltage V_{netk}, we can write:

$$3V_{eff} I_{eff} = 2U_{cm}(i_c + i_{load}) \quad (16)$$

The voltage loop model of three-level rectifier, deduct from the relation (16), is shows by figure 10.

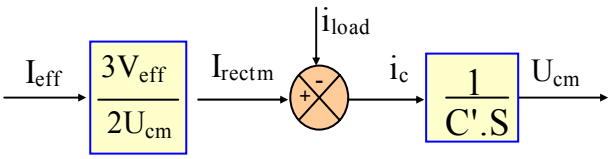

Fig.10. Three-level rectifier voltage model

We use a regulator PI for voltage. The general principle enslavement of three-level rectifier is given by figure 11.

6.3 Simulation results

We use the algorithm enslavement elaborated previously (fig.11) to control the rectifier of the cascade we apply load variation between two instants t=0.4s and t=0.8s.

We note that, the output voltage of PWM rectifier follows perfectly its reference which is constant (fig.12). Therefore the different input DC voltages of the nine-level NPC VSI are constant and practically equal by pairs too (fig.13).

The current i_{d0} has a mean value practically null (fig.14). The rectifier current I_{rect1} is respectively the opposite of the current I_{rect2}, and the current I_{rect0} has a mean value practically null (fig.15).

We remark that the network currents i_{neti} feeding rectifier follow perfectly their sinusoidal references (fig.16).The network voltage and current are in phases then the power factor of network is uniting.

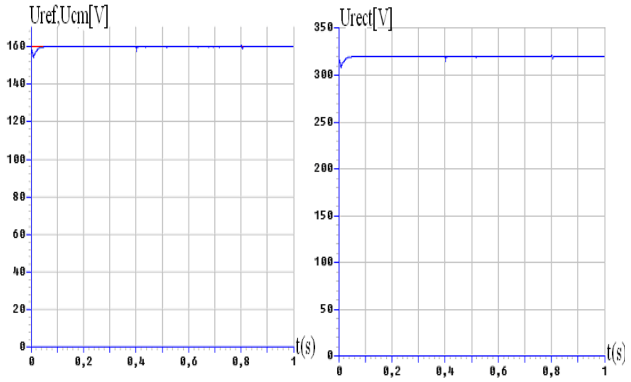

Fig.12. Output voltage of three-level PWM rectifier and its reference

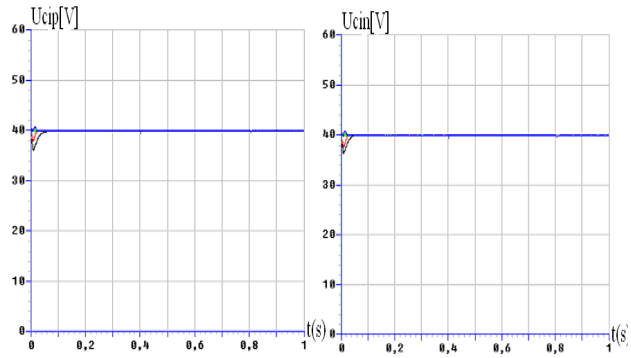

Fig.13. The DC voltages of intermediate filter

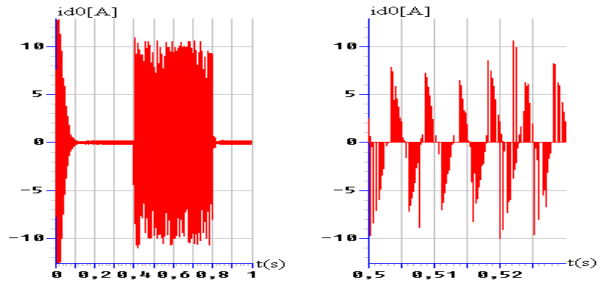

Fig.14. The input current i_{d0} of nine-level NPC VSI

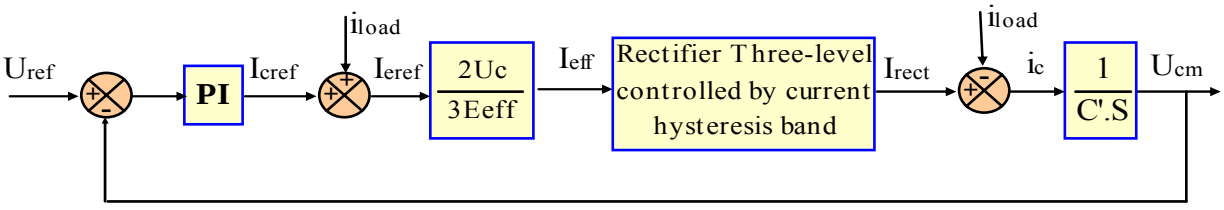

Fig.11. Enslavement algorithm of output voltage of three-level rectifier

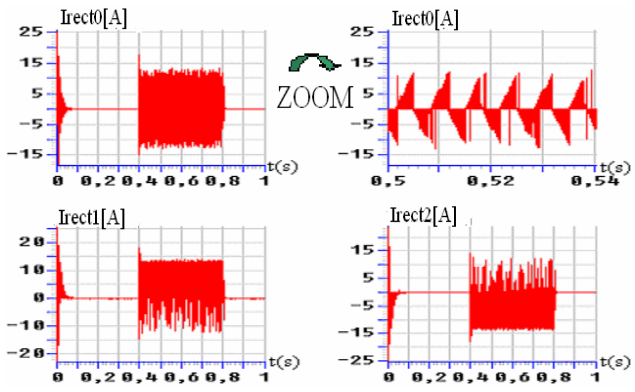

Fig.15. Output currents of the rectifier

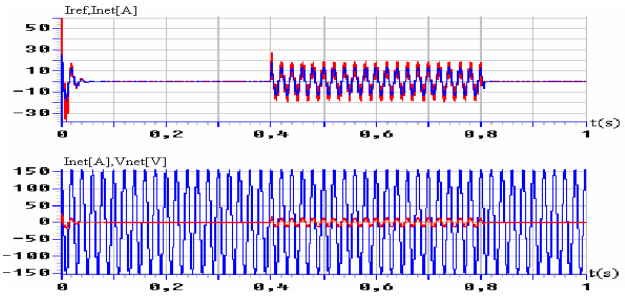

Fig.16. The network currents I_{net}, its reference and its voltage V_{net}

6.4 Application of feedback control algorithm of rectifier for the proposed cascade

In this part, we will study the performances of the speed control of the PMSM fed by nine-level NPC inverter controlled by the proposed PWM strategies. Figure 17 shows the driver of the PMSM fed quietly its reference and the torque effect for the charge variation between two instants t=0.4s and t=0.8s.

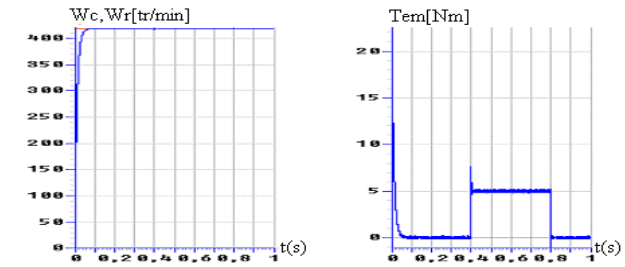

Fig.17. Three-level PWM rectifier-nine-level NPC inverter-clamping bridge-PMSM Cascade

7 Conclusion

In this paper, we have studied regulation and control of the stability problem of the input DC voltages of nine-level NPC inverter. The study of the stability problem of the input voltages of nine-level NPC inverter using a cascade constituted by three-level PWM rectifier-filter-nine-level NPC VSI.

The application of the linear feedback and introduce the clamping bridge in the cascade, shows parfait following of the output of rectifier and his reference and the stability of the input voltage of nine-level NPC inverter. So, now is possible to conceiver with frequency charger using in output the nine-level inverter, PMSM variator with feeble rate of harmonics, a power factor of network unity and great charge dynamics performance.

The results obtained with this solution confirm the good performances of the proposed solution. This study shows the effect of the stability of the DC voltages on the PMSM performances. The results obtained are full of promise to use the inverter in high voltage and great power applications as electrical traction.

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