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Low Power Amplifier Design Using CMOS Active Inductor

MING-JEUI WU, PEI-JEN YEN, CHING-CHUAN CHOU, JENN-TZER YANG

Department of Electronics Engineering
Ming Hsin University of Science and Technology
1. Hsin-Hsing Rd., Hsin-Fong, Hsin-Chu 304
Taiwan

Abstract: - In this paper, a CMOS low power amplifier based on a high-quality active inductor and implemented by using 0.25-μm 1P5M CMOS standard technology is presented. The amplifier achieves power gain (S21) of 18dB within the -3dB cutoff frequency, bandwidth of 1.3GHz, and power consumption of 18mW under 2.5V power supply in $188 \times 174 \mu m^2$ silicon area. The input third-order intercept point (IIP3) and the noise figure (NF) are -13dBm and 10dB, respectively.

Key-Words: - Amplifier, Bandwidth, S-parameter, Noise Figure, and Power Consumption.

1 Introduction

There are many applications using higher frequency circuits for the past two decades. These applications include TV cable modem, multi-band mobile communication, wireless communication systems, instrumentation, and optical communication. The traditional high frequency circuits were implemented using high speed GaAs MESFETs and MMIC technologies [1]-[4]. However, the producing costs of such devices are higher than that of the CMOS devices available today. Moreover, the coming advancement in state-of-the-art electronic systems and future system-on-chip solutions will comprise the digital, the analog and the high frequency circuits with a huge demand for low-cost, high-speed, and mixed-signal integrated systems. It is essential that high frequency circuits can be implemented in low-cost CMOS technology. Recently, there are considerable efforts working on the migration of the high frequency elementary circuit blocks from GaAs to CMOS process [5-8]. Unfortunately, such circuit migration has not been able to achieve directly. One major obstacle of the migration is that it is difficult to implement high frequency circuits in CMOS because of the deleterious substrate coupling effects. The highly doped substrate causes substantial losses especially when on-chip passive spiral inductors operate above GHz frequency during CMOS manufacturing process.

Most of the previous reports in CMOS high frequency circuits were implemented by using on-chip passive spiral inductors to achieve better matching, higher wide bandwidth, higher power gain, and lower power consumption [9-14]. However, the low quality-factors of an on-chip passive spiral inductor cause the degrading of the gain/bandwidth performance and larger power consumption. Furthermore, obtaining a high quality factor of spiral inductor often requires additional processing steps to compensate the quality factor and these additional processing steps also require extra cost [15-16]; moreover the inductance value is dependent on the size of the inductor [17]. The die area of an integrated passive inductor is usually larger than other components.

An alternative method called active inductor is to use the CMOS active devices as an inductor, where the equivalent inductive impedance can be implemented. The above difficulties can be overcome by using an active inductor. The active inductor is an alternative technique, which is implemented by using circuit configurations, called gyrator. The quality-factor and the inductance value obtained by this active technique are high enough to overcome the value exhibited by conventional spiral inductors. Depending on the chosen topology, the loss of an active inductor caused by the active devices can be greatly reduced and the area of an active inductor is totally independent of the desired inductance values [18-21]. Most of the active inductor circuits were applied in low noise amplifiers, band-pass filters, and voltage control oscillator and they produced impressive results [22-26]. Although, the active inductor approach has not been applied on the low power amplifiers with wider bandwidth and the smaller die area, it is possible that we can apply the characteristics of

high-quality factor, amplifier configuration, and negative feedback topology of a high-quality active inductor on the amplifier design of lower power consumption, wider bandwidth, and smaller die area.

A simple grounded active inductor configuration is a very popular inductor, where two transconductors are connected in back-to-back configuration [27]. However, the non-desirable characteristics of active devices among drain, source of MOSFET and DC bias circuits will limit the performance of the active inductor circuits such as the Q-value and the operating frequency [28]. These limitations degrade the performance of application circuits using active inductors. In this paper, a CMOS amplifier circuit based on a high-quality active inductor is presented in section **2**. In section **3**, the measuring characteristics of the implemented amplifier using 0.25-μm CMOS technology is introduced. Finally, the conclusion is summarized in section **4**.

2 Circuit Design

The prototype of the inductor-less low power amplifier circuit based on the proposed high-quality active inductor is shown in Fig. 1. This circuit consists of three different stages, including common gate configuration, high-quality active inductive load and buffer stage. Transistors M_{S1} and M_{S2} comprise the input common gate amplifier stage. This common-gate configuration provides low input impedance, expressed in Eq. (1), and achieves a simple input matching, and higher linearity without source degeneration inductor. This common-gate approach also helps to increase the effective reverse isolation.

$$Z_{in} \approx \frac{1}{g_{ms2}} // \frac{1}{g_{dss1}} // \frac{1}{g_{dss2}} \approx \frac{1}{g_{ms2}} \qquad (1)$$

A high-quality active inductor is constructed by transistors M_1~M_3, M_P, resistance R_G, and capacitance C_N. The high-quality active inductor is employed to fulfill the load of the common-gate amplifier. High-quality active inductive load is applied mainly for three reasons. Firstly, the high quality-factor active inductive load consumes less die area than on-chip passive spiral inductor does; secondly, the amplifier can obtain higher power gain, and requires less dc bias current. Thus, the power consumption of the amplifier can be saved. Finally, the architecture of the active inductor has the topology of the negative feedback; hence it can improve the frequency response of the amplifier. Output buffer stage is designed as common-drain stage, which comprises transistors M_B and R_B. This common-drain configuration minimizes the loading effect and provides a simple output impedance matching. Therefore, the overall gain of the amplifier can be expressed as Eq. (2).

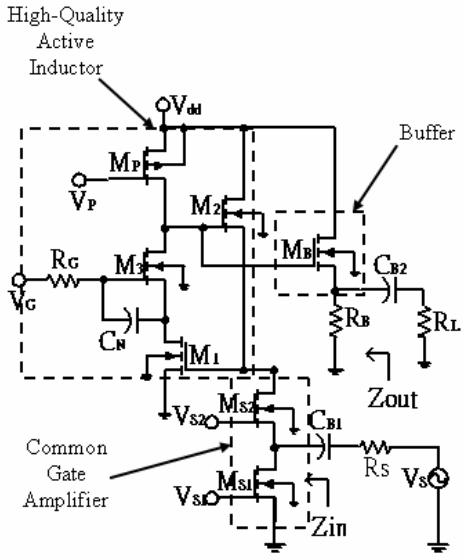

Fig. 1 Proposed amplifier circuit

$$A_{V,overall} \approx A_{v,C.G.} \times [(g_{dsp} + g_{mp} + g_{ds1}) + sC_{gs1} + \frac{g_{m1}g_{m2}g_{m3}}{(sC_{gs2}+g_{ds1}g_{ds3})} \frac{g_{m1}g_{m2}/g_{dsp}+g_{mB}+sC_N}{g_{mB}+sC_N} g_{m2})^{-1}] \times (\frac{C_N g_{m1} g_{m3}}{C_{gd1} g_{d3}} \frac{\frac{sC_{gs2}(sC_{gd1}+g_{m3})}{g_{m1}g_{m3}}+1}{s+\frac{sC_{gs2}(sC_{gd1}+g_{m3})}{C_{gd1}g_{ds1}}}) \times A_{v,buffer} \qquad (2)$$

where $A_{v,C.G}$ and $G_{m,C.G.}$ are the voltage gain and the transconductance of the common-gate amplifier, respectively. $Z_{load,\ active\_inductor}$ is the equivalent input impedance of the high-quality active inductor. $A_{v,buffer}$ is the gain of the buffer stage. In Eq. (2), the quality-factor improvement of the active inductive load will improve the performance of the amplifier such as die area, power consumption, and bandwidth. Furthermore, this characteristic of the amplifier is sensitive to the parasitic components and the following stage loading. Tuning the external biases of V_{S1}, V_{S2}, V_G and V_P can modify these effects of the overall circuit response. Therefore, it is easy to tune the variation because of the process or other factors. Capacitors C_{B1} and C_{B2} are used as a DC blocking capacitor of the input and output to isolate DC voltage of the previous stage and the following stage.

3 Measurement Results

All transistors in this amplifier have the same

dimensions. The minimum length and width are 0.24um and 40um. Resistance R_G, and R_B are 750Ω and 120Ω respectively and capacitance C_N is 0.7PF. The biasing values are V_{S1}=V_{S2}=1V, V_G=1.7V, V_P=1.4V and the normal supply voltage is 2.5V. Fig. 2 shows the die photo with a die area of 188 × 174μm^2 and the bonding pads are not included. The die area is much less than the one using the on-chip passive spiral inductor. Note that the dc power supplies separating the RF input and output pad is for reducing mutual coupling. In order to measure the circuit, a PCB board is built. All dc bias pads are bonded with PCB board. The RF input/output pads are measured directly through probe station.

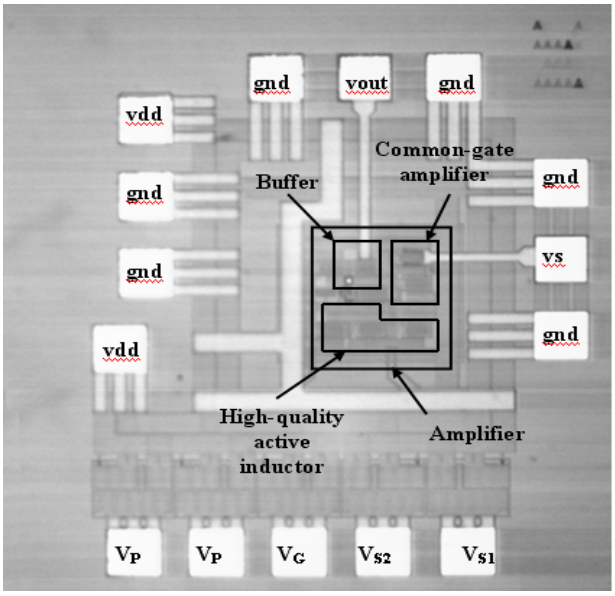

Fig. 2 Micrograph of the proposed amplifier

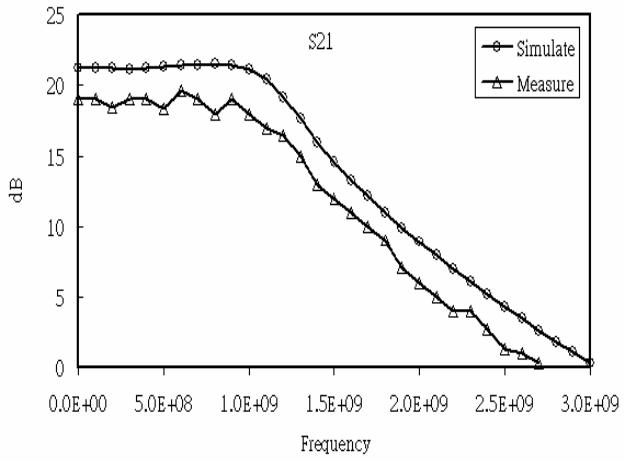

Fig. 3 Measured and simulated of power gain (S21) of proposed amplifier

A network analyzer carries out the measurement of the S-parameters. Capacitors C_{B1} and C_{B2} are used by the external DC blocking capacitor and the effects between the probe and the connector of network analyzer are calibrated into the network analyzer in which it only considers the internal characteristics of the amplifier. Fig. 3 shows the power gain (S21) of this CMOS amplifier. The amplifier demonstrates the flat power gain of 18dB and 0 to 1.3 GHz bandwidth in the –3dB cutoff frequency. The total dc power consumption is only 18 mW under 2.5V dc power supply.

Unlike the passive inductor where the damping resistor is the main noise producer, the noise in active inductor originates from the thermal noise and the flick noise of MOS transistor channel while the damping resistor is a fictitious one without any noise contribution. In this amplifier's design shown in Fig. 1, the first stage is a common-gate configuration, and the load of the common-gate amplifier is a high-quality active inductor. The final stage is a common-drain configuration. To have a fully understand of noise characteristic of amplifier, the noise analysis of active inductors is therefore important. Eq. (3) derived the noise factor of the high-quality active inductor and is show in Fig. 1.

$$NF \approx 1+\frac{2R_G}{3C_N}\left(\frac{1}{g_{m2}}+\frac{1}{g_{m1}}+\frac{g_{m3}+g_{dsp}}{g_{m1}^{\ 2}}\right) \quad (3)$$

Generally, the noise effects in a common-gate topology include the thermal noise and the flick noise. Thus, the noise factor of the common-gate amplifier can be expressed as Eq. (4).

$$NF \approx \frac{K_N}{C_{ox} f g_{ms2}}\left[\frac{g_{ms1}^{\ 2}+g_{ms2}^{\ 2}}{(WL)_{s2}}+2\frac{g_{m2}^{\ 2}}{(WL)_{m2}}\right]+\frac{2}{3}\left[\frac{g_{ms1}+g_{ms2}+2g_{m2}}{g_{ms2}^{\ 2}}\right] \quad (4)$$

where K_N, Cox, and f are a process-dependent constant on the order of 10^{-25} V^{2}F, a gate capacitance, and the operating frequency of MOSFET, respectively. The final stage is a common-drain configuration. The noise factor of this stage is derived in Eq. (5).

$$NF \approx \frac{2}{3}\left(\frac{1}{g_{mB}}+\frac{1}{g_{mB}^{\ 2}R_B}\right) \quad (5)$$

Thus, the total noise factor of the proposed amplifier is the effect of Eq. (3)-(5). Assuming all transistors' dimension is identical and $g_{m1}=g_{m2}=g_{m3}=g_{mp}=g_{mB}=g_m=\frac{1}{2}g_{ms1}=\frac{1}{2}g_{ms2}$, so the noise factor cab be rewritten as Eq. (6).

$$NF \approx \frac{1}{f}\left(\frac{5K_N}{2C_{ox}WL}\right)+\frac{1}{g_m}+\frac{2}{3}\left(\frac{1}{g_m}+\frac{1}{g_m^{\ 2}R_B}\right)+\left(1+\frac{2}{3}\frac{3+R_G g_{ds}}{C_N g_m}\right) \quad (6)$$

From Eq. (6), the first term in Eq. (6) indicates the noise is significantly affected by flick noise at low frequency. As the frequency is increased, the noise factor can be affected mainly by the thermal noise. Furthermore, a higher g_m can minimize the noise factor of the amplifier. However, in an amplifier design, the used transistor size is the tradeoff between noise factor and total power consumption. The measured noise figure of this amplifier is shown in Fig. 4, and the frequency range is from 0Hz to 3GHz. It indicates that the noise figure is around 10dB in the frequency range of 100MHz and 3GHz, and this noise factor is reasonable in some applications. Fig. 5 shows the two-tone testing results to evaluate the linearity of the amplifier. The injected signals are 0.9GHz and 1.1GHz respectively. The input third-order intercept point (IIP3) is -13dBm. The comparison of this design and other designs is shown in TABLE I and the proposed amplifier has better performance using the proposed high-quality active inductor.

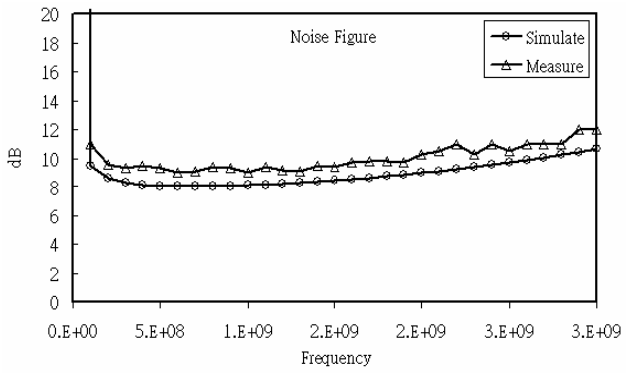

Fig. 4 Measured and simulated of noise figure (NF) of proposed amplifier

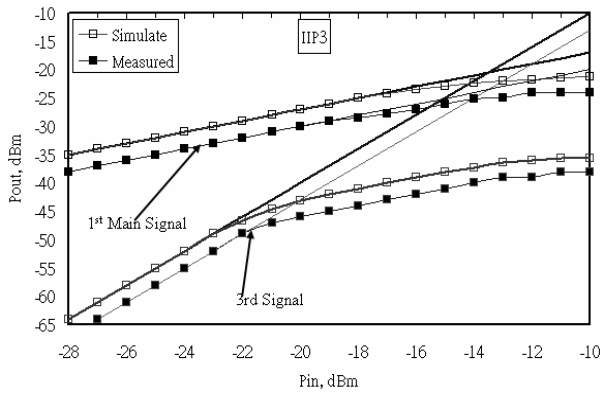

Fig. 5 Measured and simulated of input third-order intercept point (IIP3) of proposed amplifier

TABLE I COMPARISON WITH OTHER AMPLIFIER DESIGNS

	A. Worapishet[15]	W. Sansen [8]	C. K. Wang [14]	Y. C. Chen [7]	This Work
Gain (dB)	21	39	14	10.5	18
Power Consumption (mW)	132	240	30	25	18
Bandwidth (GHz)	5	0.8	0.185	1.7	1.3
Processing (μm)	0.35	1.2	0.8	0.25	0.25

4 Conclusion

In this study, based on the high-quality active inductor, a low power amplifier can achieve 18dB high power gain, 1.3GHz wide bandwidth, 188 × 174μm^2 small die area, and 18 mW low power consumption under 2.5V dc power supply.

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