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DC-Free Turbo Coding Scheme Using MAP/SOVA Algorithms

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Abstract :- A useful tool in the design of reliable digital communication systems is channel coding. Turbo codes have been shown to yield an outstanding coding gain close to theoretical limits in the Additive White Gaussian Noise (AWGN) channel. In this paper, a novel DC-free turbo coding scheme using Maximum A Posteriori algorithm (MAP)/ Soft Output Viterbi Algorithm (SOVA) for the turbo decoder is presented. The proposed scheme achieves the DC-free coding and error-correcting capability simultaneously. The scheme has a simple cascaded structure of the running digital sum (RDS) control encoder and the turbo encoder. A given sequence becomes DC-free if and only if the absolute RDS value of the sequence is bounded by a constant for any time instant. The RDS control encoder generates a sequence which gives the turbo coded sequence with a bounded RDS value. The structure allows us to exploit efficient soft-decision decoding which attains additional coding gains compared with hard-decision decoding over an additive white Gaussian noise (AWGN) channel.

Key-Words: - Turbo Code – DC-free Codes – MAP algorithm – SOVA algorithm – Convolutional Code

1 Introduction

DC-free codes can be used in wired transmission systems to decrease the degradation due to the use of coupling components and/or isolating transformers [1],in magnetic-tape recoding to prevent write-signal distortion caused by transformer coupling in the write electronics [2], in optical recoding to reduce interference between servo signals and data [2], and in wireless systems to assist with the insertion of pilot tones [3]. In these applications, error-control (EC) codes are also employed to overcome impairments in the channel. The conventional method of incorporating both EC coding and dc-free coding into a digital communication system is through concatenation of an EC code as the outer code and a dc-free code as the inner code [4]. In general, dc-free codes have little or no EC ability, and their decoders exhibit error extension, expect binary input, and output hard decisions. To avoid the impact of error extension of dc-free decoding on a subsequent EC decoder, and to enable the use of soft decision decoding and iterative algorithms during EC decoding, it is desired that in the receiver, dc-free decoding follow EC decoding [4]. Concatenation schemes with a partially reversed order of conventional dc-free and EC coding have been proposed in [5], [6]. Constructions for some integrated binary dc-free EC codes have been presented in [7] .[8]. In [9], a method was introduced for integrating dc-free codes and EC block codes that fully reverses the conventional order of dc-free decoding and EC decoding.

There are several works on DC-free error-correcting codes based on convolutional codes. Deng, Li, and Herro [10] presented a DC-free error-correcting convolutional coding technique.

In their method, the all 1's vector in the generator matrix of a convolutional code is exploited to control the running digital sum (RDS) of encoded sequences. Nasiri-Kenari and Rushforth [11] investigated DC-free subcodes of convolutional codes. Recently, Chiu [12] showed DC-free error-correcting codes based on convolutional codes. In Chiu's scheme, a codeword of a convolutional codes with a small RDS value is chosen with the Viterbi algorithm. These methods seem promising and further investigation on binary DC-free coding schemes with a simple trellis structure, or equivalently, with small decoding complexity is hoped for.

In this paper, we present a novel DC-free Turbo coding scheme with an error correcting capability. Fig. 1 represents the architecture of our proposed scheme. First, the user message sequence *($u_0u_1u_2$……)* is encoded to the *intermediate sequence* by an *RDS control encoder*. The convolutional encoder then converts an intermediate sequence to the coded sequence *($x_0x_1x_2$……)*. After the ordinary binary-bipolar conversion, the coded sequence is transmitted over a noisy channel such as the additive white Gaussian noise (AWGN) channel. The term "RDS" means the running digital sum of a (bipolar) coded sequence. It is well known that the DC-free property is achieved if and only if the absolute value of the RDS is bounded by a constant value for any time instant [13]. The RDS control encoder must generate an intermediate sequence which gives a coded sequence with a desired RDS constraint. In other words, an intermediate sequence should be determined in such a way that it generates coded sequences with a bounded RDS.

Fig. 1 presents the cascaded structure of the RDS control encoder/ decoder and the turbo encoder/decoder.

With this architecture, we are able to exploit soft-decision decoding with the Viterbi algorithm. Moreover, the dashed box part in Fig. 1 is exactly identical to a turbo coding system. The RDS control encoder and decoder can be regarded as a front-end and a back-end of the turbo coding system. Thus, we can use a ready-made CODEC to implement the proposed scheme.

The proposed scheme is based on the following three major ideas: 1) *additive encoding* using a binary linear block code, 2) upper and lower bounds on the RDS for an additive encoder, and 3) splitting a convolutional code into infinite sequences of a linear block code, which is called a *window code*. In the following, we shall explain these ideas in order.

2. DC-Free Coding Scheme Based On An Additive Encoder

In this section, firstly, the necessary notations and definitions will be introduced. Then, a DC-free coding scheme based on an additive encoder is presented. The scheme has a close relationship to the idea of additive coding.

2.1 Notation and Definition

For $v = (v_0, v_1, v_2, \ldots\ldots v_{n-1}) \in \{0,1\}^n$, the vector RDS of v is given by

$$S(v) \cong \sum_{j=0}^{n-1} f(v_j) \qquad (1)$$

The binary- bipolar conversion mapping f is defined by

$$f(L) \cong \begin{cases} -1 & L = 0 \\ +1 & L = 1 \end{cases} \qquad (2)$$

The upper and lower RDS of v are defined by

$$U(v) \cong \max_{0 \le t \le n-1} \sum_{j=0}^{t} f(v_j) \qquad (3)$$

$$L(v) \cong \min_{0 \le t \le n-1} \sum_{j=0}^{t} f(v_j) \qquad (4)$$

For binary linear block code C (n ,k ,d) where n, k, and d denote the length, the dimension, and the minimum distance, respectively. If two binary linear codes C_0 and C_1 satisfy

$$C = \{c_0 \oplus c_1 : c_0, \in C_0, c_1 \in C_1\}$$

and

$$C_0 \cap C_1 = 0,$$

then the pair of codes *(Co, C_1)* is called the direct sum decomposition of C. The code C is called the direct sum code based on C_0 and C_1. Let k_0 and k_1 be the dimensions of C_0 and C_1, and G_0 and C_1 be the generator matrices of C_0 and C_1, respectively. From the definition above, it is obvious that the equality $k = k_0 + k_1$ holds. Assume one to one mappings called encoding mappings:

$$\psi_0 : F_2^{K0} \rightarrow C_0$$

$$\psi_1 : F_2^{k1} \rightarrow C_1$$

where F_2 is the Galois field with two elements {0, 1} and the addition over F_2 is denoted by $\oplus$.

3 Additive Encoder

Assume an infinite length binary message sequence *{a_0, a_1....}*. Each vector a_i *(i=0, 1, 2 ...)* belongs to $F_2^{K_i}$. An additive encoder encodes a message block a_i to *ci* $\in$c for each block index. The code C is a binary linear code of length n. The resulting sequence *{c_a , c_1...}* is called a coded sequence. The additive encoder appends redundancy $k_0=k-k_1$ bits per block and

thus the coding rate becomes k_1/n. After the binary-bipolar conversion, the bipolar sequence $\{f(c_0), f(c_1)...\}$ is transmitted over the-noisy channel.

For achieving DC-free transmission, the additive encoder has to generate the coded sequence with a RDS constraint.

An additive encoder encodes a message block a, into c, in such a way:

$$C_i = \psi_0(b_i) \oplus \psi_1(a_i) \quad (5)$$

where $b_i \in F_2^{k_0}$ F™ is called control vector. In other words, the additive encoder has freedom to select a control vector and should specify a control vector so as to obtain a code sequence which keeps the RDS value bounded.

4. Proposed DC-Free Error Correcting Codes

4.1. Introduction.

Assume that a turbo code C together with the parameter α, β, γ, and a decomposition matrix M are given. The code C is called the base turbo code.

The following is the detail of the DC-free turbo coding such as encoding and decoding,

4.2. Encoding

The message sequence $(u_0u_1u_2\ldots\ldots)$ is divided into blocks of length β. The i-th (i=0, 1, 2 …) message block is denoted by

The message sequences are encoded to the intermediate sequences by the RDS control encoder. The intermediate sequence $(x_0x_1x_2...)$ is divided into the intermediate block of length L. The i-th intermediate block is defined by

$$u_i = (u_{i\beta}, u_{i\beta+1}, u_{i\beta+2}, \mathrm{K}, u_{(i+1)\beta-1})$$

where O_i is the first pm-tuple of x_i and n_i is the last $\gamma+\beta$-tuple of x_i such that

$$x_i = (x_{(\gamma+\beta)i}, x_{(\gamma+\beta)i+1}, \mathrm{K}\ x_{(\gamma+\beta)i+L-1})$$

$$x_i = (0_i \setminus n_i)$$

We obtain a coded sequence $(y_oy_1...)$ by encoding the intermediate sequence with the turbo encoder. The coded sequence is divided into the coded blocks of length r. The i-th (i = 0, 1, 2,) coded block has the form

$$y_i = (y_{ri+qm}, y_{ri+1+qm}, \mathrm{K}\ y_{r(i+1)-1+qm}$$

$$y_0 = (y_{qm}, \mathrm{K}, y_{r-1+qm})$$

Note that the relation between the message, intermediate and coded sequences is shown in figure 2

Notice that the intermediate blocks x_i and x_{i+1} are overlapping. The overlapping part corresponds to o_i. By applying the additive encoder to a window code, the overlapping is taken into account. Within the intermediate block x_i, only the vector n_i can be assigned freely without any influence of the previous block. The overlapping part o_i is determined by the previous intermediate block x_{i-1}. As shown in figure 2, the RDS control encoder adds redundancy (a control vector) to the message sequence and thus the coding rate defined between the message and intermediate sequence becomes $\beta / (\gamma + \beta)$. The turbo encoder appends redundancy to the intermediate sequence. Consequently, the overall rate becomes $R \cong (p\beta)/(q(\gamma+\beta))$. The rate loss can be considered as a price for obtaining a RDS constraint.

4.3. Decoding

The decoding issue for the proposed scheme is discussed in this section. The received sequence is first decoded by the MAP/SOVA decoder for the base turbo code C. let the set of all allowable sequences generated by the proposed scheme be C_{RDS}. The minimum free Hamming distance defined on C_{RDS} is denoted by d'_{free}. From the cascaded structure of the proposed scheme, evidently, C_{RDS} is contained in C and the inequality $d'_{free} \geq d_{free}$ holds. The symbol d_{free} denotes the minimum free hamming distance of C.

As a consequence of this property, we can use the MAP decoder for the base Turbo code to decode C_{RDS}. It can be considered as a kind of a super code decoding. The decoding of the intermediate sequence is straight forward from the definition of the RDS control encoder.

Let b_i^*, n_i and u_i be the estimated blocks corresponding to b_i^*, n_i and u_i respectively.

Multiplying the inverse matrix of M to n'_i from left, we have

$$n_i M^{-1} = (b_i^* / u_i) \quad (6)$$

Where output $\hat{u}_i$ is the i-th estimated message block.

5. Simulation Results

As discussed before, DC-free codes are usually required in digital transmission and recording systems to reduce the effect of baseline wander and match spectra of the transmitted signals to frequency characteristics of the transmission media. A given sequence becomes DC-free if and only if the absolute Running Digital Sum (RDS) value of the sequence is bounded for any time instant.

Fig.3. shows degree of performance improvement according to RDS value of the sequence.
The simulation results shows that turbo code which has bounded running disparity of code sequence gives better performance than turbo code which has sequence of all ones or all zeros or any other sequence that does not have RDS=0.
In this section, simulation results of BER versus E_b/N_o were plotted to show the influence of various parameters. The channel model used is An (AWGN) channel. The DC-Free Turbo decoder is used in an iterative fashion until we achieved the 7^{th} iteration. The component decoder based on the MAP algorithm.

Fig. 4 shows the performance improvements when we apply the dc-free property to the turbo code using MAP decoder algorithm and 3^{rd} iterations with rate 1/3, frame size 400 bits and 64-state DC-free coding scheme with the overall rate 6/16 and the minimum free distance 10 has been obtained compared with turbo code using decoder based on SOVA algorithm with the same specifications.

Fig. 5 shows the performance improvements when we apply the dc-free property to the turbo code using MAP decoder algorithm and 3^{rd} iterations with rate 1/3, frame size 400 bits and 64-state DC-free coding scheme with the overall rate 6/16 and the minimum free distance 10 has been obtained compared with covolutional code with 8-state dc-free coding scheme with the overall rate 3/7 and the minimum free distance 5 has been obtained and this scheme satisfies a bounded RDS constraint (from -9 to +9).
This scheme satisfies a bounded RDS constraint (from 18 to +18).

5.1. Influence of number of iterations

In fig 6. BER verses E_b/N_o curve is shown parameterized by the number of decoding iterations. The results show that, the BER decreases as the number of iterations increases for the same frame size and code rate.

5.2. Influence of Frame Size

In fig 7., the simulated performance results of DC-free turbo codes with the same component code but different frame size is shown parameterized by the frame size.
We can notice that at the same E_b/N_o DC-Free Turbo code gives the most efficient BER than the Turbo code.

6 Conclusion

A new construction of DC-free codes based on turbo codes which can simultaneously meet the dc constraint and error-correcting requirement is proposed. The presented scheme divided into two parts: the RDS control encoder/decoder and the turbo encoder/decoder. The RDS control encoder generates several codewords of a window code for selecting a control vector. The decoding requires simpler tasks than the encoder, also, BER performance for DC-free turbo code is investigated for many different cases: performance of 7 decoding iterations for fixed code rates and constraint lengths but different frame sizes, performance of 7 decoding iterations for fixed frame sizes but different code rates, and performance improvement between 1 decoding iteration and 7 decoding iterations for fixed code rates and constraint lengths but different frame sizes.

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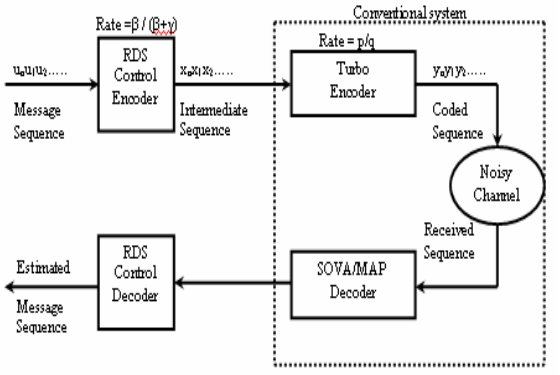

FIG 1. Architecture of DC-free TURBO coding scheme

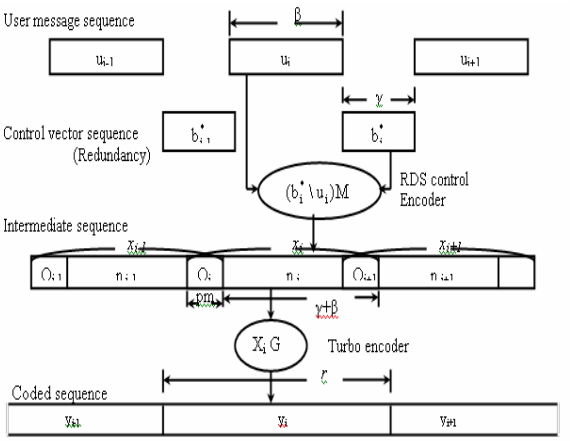

FIG.2. Relations among message, intermediate and coded sequences

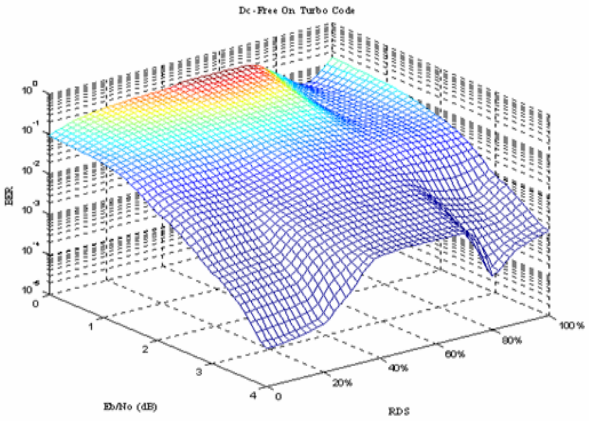

Fig. 3. DC-Free Turbo Code

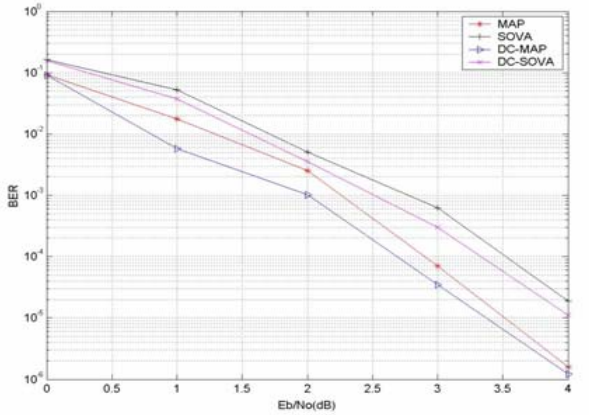

Fig. 4. DC-free Turbo code using MAP/SOVA algorithms

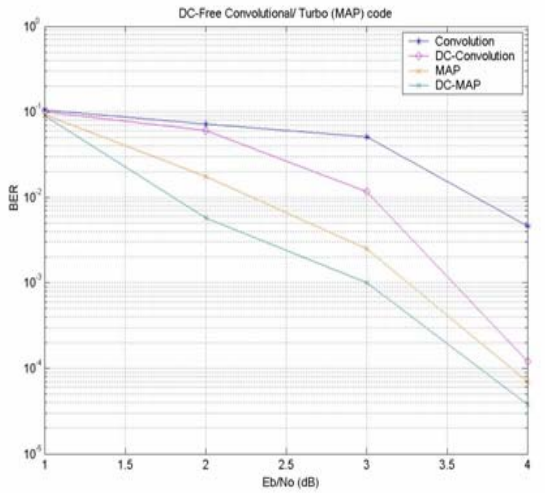

Fig. 5. DC-free Convolution code and DC-free Turbo code using MAP algorithm

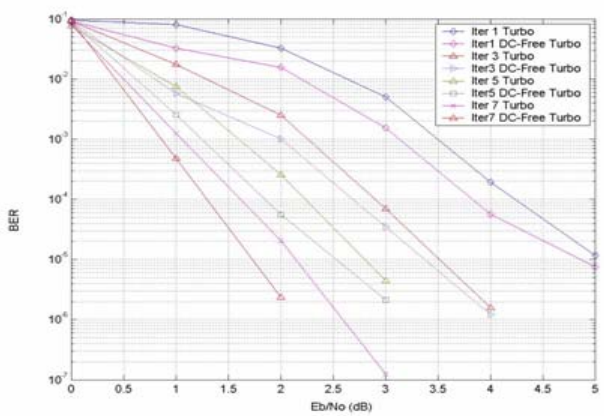

Fig. 6. DC-free Turbo code using 1, 3, 5 and 7 iterations.

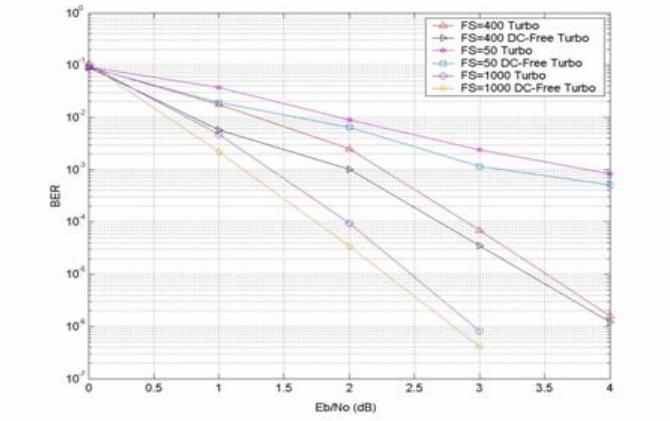

Fig. 7. DC-free Turbo code using 50, 400 and 1000 bits frame sizes