Proceedings of the 5th WSEAS International Conference on Telecommunications and Informatics, Istanbul, Turkey, May 27-29, 2006 (pp176-180)

Design and Implementation of a Switched Bus-based Home Network Interconnection System

YANG-KEUN AHN, KWANG-SOON CHOI, YOUNG-CHOONG PARK,
KWANG-MO JUNG, and SEONG-DONG KIM
Ubiquitous Computing Research Center
Korea Electronics Technology Institute,
68, Yatap-Dong, Bundang-Gu, Sungnam-Si, Kyunggi-Do 463-816
KOREA

Abstract: - In this paper, we present the design of a Home Network System using a HomeStation-Chipset based on Serial Switched Bus Technology. We describe the features of HomeStation-Chipset, a Serial Switched Bus Technology. The Home Network System Bus, which is newly designed, consists of a Switch Board and Bridge Boards. For their verification, we compose a Home Network environment and measure the performance of a Serial Switched Bus by the designed Switch Board and Bridge Board. Finally, the suitability of the Serial Switched Bus to a Home Network System is discussed.

Key-Words: - Switched Bus, Home Network, Interconnection Networks, SerDes, LVDS

1 Introduction

The PCI bus developed in the early 1990s was an epoch-making standard bus that overcame several shortcomings of a local bus such as an ISA bus. This bus can exchange data mutually by a PCI standard irrelatively to the kind of I/O device or CPU. With the advent of high speed semiconductor technology and increased amount of information, the PCI bus has advanced accordingly. In order to solve the problem of bandwidth, buses such as AGP and PCI-X have been developed. Because several I/O devices consist of a parallel bus that share buses, a bottle-neck problem occurs in the case of several host CPUs.

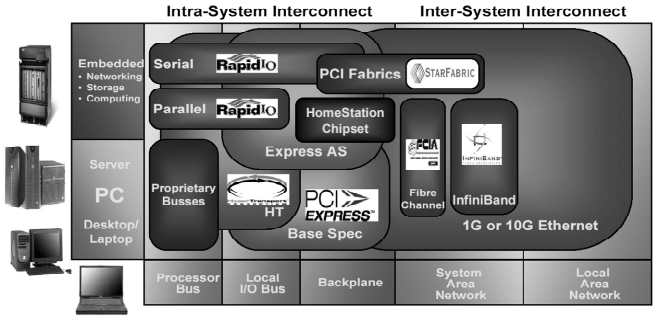

Fig. 1. System Interconnection Technologies

Presently, PCI buses are utilized in various applications such as set top boxes, communication systems, real-time systems, factory automation systems, and PCs. Also, the PCI bus can be used in Home Network Systems. To exchange high-capacity data such as multimedia data at high speed in a Home Network system, a higher speed bus is required.

A serial switched bus can solve the problems of a parallel bus such as a PCI. Because a Serial Switched Bus exchanges data into the switching, it does not suffer from a decline in speed. Fig. 1 displays the most recently developed interconnection technologies. While RapidIO and PCI Express are switched buses, they can be used within a system[1,2]. On the other hand, StarFabric can extend to several meters by a LVDS signal because it can maintain distance physically to networks between several systems. In this paper, we present the design and verification of a Home Network System using HomeStation-Chipset, a type of Serial Switched Bus.

2. Features of HomeStation Chipset

HomeStation Chipset, a kind of Switched Bus, is a powerful technology that will be applicable to a high-performance Home Network System. Because PCI is a shared parallel bus, it inherently entails a decrease of efficiency. Fig. 2 shows the traditional shared bus architecture. In contrast, HomeStation Chipset guarantees a bandwidth in each I/O device by use of switching architecture, as illustrated in Fig.3 [3,4].

HomeStation-Chipset significantly raises bandwidth and operability with unique Home Network Protocol. New systems such as Home Network Systems need higher performance and

inter-operability. HomeStation-Chipset is the best solution that supports these requirements. HomeStation-Chipset supports CCP (Common Communication Protocol for Generic Linkage on Heterogeneous Networks) for Home Network. The CCP is one of the unique Home Network Protocols and the standard of IEC (International Electro technical Commission) TC (Technical Committee) 100[8]. The Home Station-Chipset consists of HS5000 Switch Chip and HS1000 Bridge Chip. HomeStation-Chipset and CCP are designed by KETI (Korea Electronics Technology Institute).

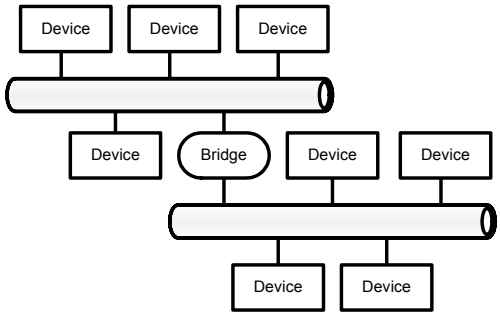

Fig. 2. Traditional Shared Bus Architecture

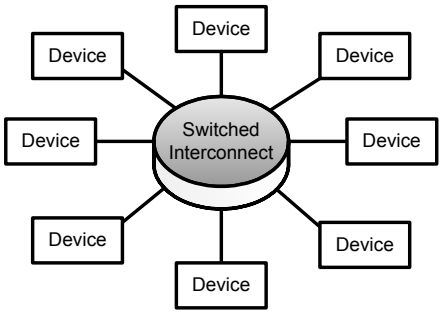

Fig. 3. Switched Bus Architecture

3. Design of HomeStation Switch Board

Fig. 4 presents a hardware block diagram of the designed HomeStation Switch Board. The Switch Board is composed of a Switch Part, a LVDS SerDes Interface Part and a High Speed Connector Part. A packet with a LVDS interface is transmitted to the destination port through the routing method of the HomeStation Switch. In order to compose 5 HomeStation links, one HS5000 Switch Chip is used. High-speed switching is possible by two links between the switch chip.

3.1 Switch Part

The Switch Part is composed of one HS5000 HomeStation Switch Chip. As Fig. 5 shows, the HS5000 HomeStation Switch facilitates the design of high-performance and reliable HomeStation based switching systems. System designers can develop high performance systems that deliver voice, video, and data. The HS5000, a single-chip solution, offers five 2.5Gbps full duplex parallel links, which deliver 25Gbps of aggregate, non-blocking, full duplex switching capacity.

Along with its high performance, the HS5000 can handle CCP packet through its extensive functionality. The HS5000 is designed to work with other HomeStation bridge chip that employs protocols such as CCP. System designers can build system architectures that combine control, voice, cell and packet data.

The HS5000 allows CCP based designs to be easily migrated to HomeStation, yet maintain their investments in software and applications.

The HS5000 allows system designers to cost effectively engineer highly reliable and available systems.

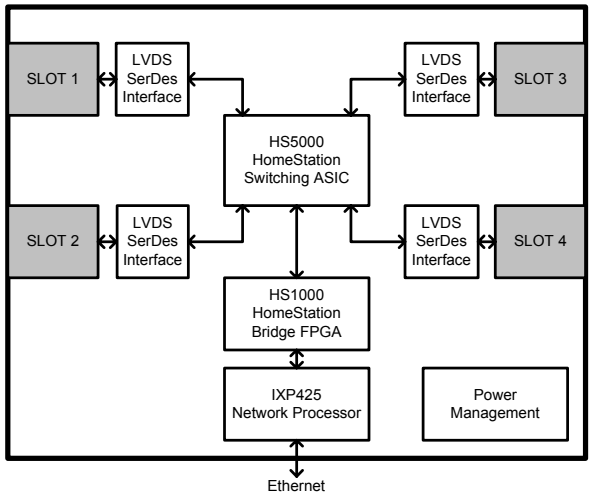

Fig. 4. Switch Board hardware block diagram

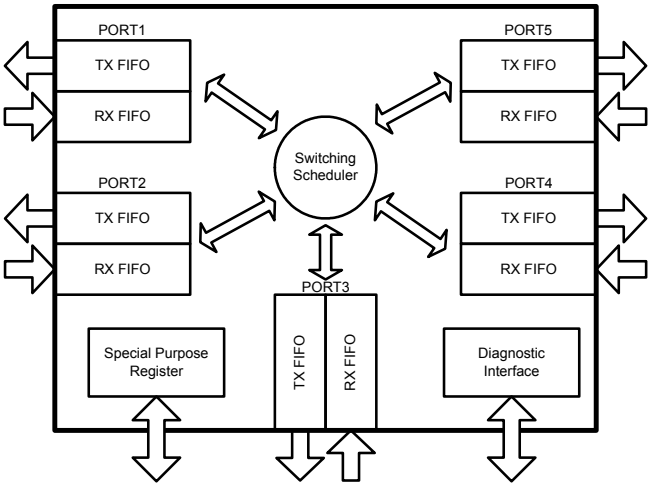

Fig. 5. HS5000 block diagram

3.2 LVDS SerDes Interface Part

As Fig. 7 shows, the Physical Layer of HomeStation Switch Board Slot is 2.5Gbps LVDS. The LVDS interface is designed by DS92LV16[6].

The DS92LV16 is a member of National's robust and easy-to-use Bus LVDS serializer/deserializer (SerDes) family already popular in a wide variety of telecom, datacom, industrial, and commercial backplane/cable interconnect applications. The DS92LV16 is similar to the original 10-bit Bus LVDS SerDes products, but provides a wider, 16-bit data bus payload.

The DS92LV16 Serializer/Deserializer (SerDes) pair transparently translates a 16–bit parallel bus into a BLVDS serial stream with embedded clock information. This single serial stream simplifies transferring a 16-bit, or less bus over PCB traces and cables by eliminating the skew problems between parallel data and clock paths. It saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.

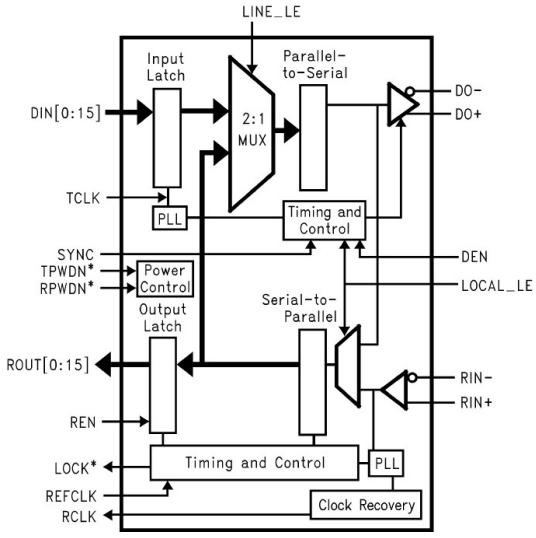

Fig. 6. DS92LV16 Block Diagram

The DS92LV16 is very flexible and performs over a wide, 25-80 MHz frequency range. Both the transmit clock and receiver reference clock have high jitter tolerance, allowing the use of low cost clock sources. The serializer and deserializer sections are fully independent and can be operated at different frequencies. This is useful when upstream and downstream rates are not balanced. In addition, the serializer and deserializer blocks can be powered down independently if only one transmission direction is needed.

The following list summarizes the LVDS routing recommendations:

-The distance between differential pairs should be a minimum of 2S. 20 mil separation or more is recommended.

-The LVDS portion/layers of the circuit board must be constructed with a controlled transmission line impedance of 50Ω (100Ω differential).

-Trace impedance should be controlled within +/- 10%, but +/- 5% control is recommended.

-A minimum distance of ~30 mils should be maintained between the digital signals and the LVDS signals.

-The maximum recommended skew between the + and - signals within each differential pair should be no more than 25ps.

-There should be a maximum time skew of 300ps between the four differential pairs that comprise an SG1010 link.

-LVDS routing should be completed before digital CMOS and TTL routing.

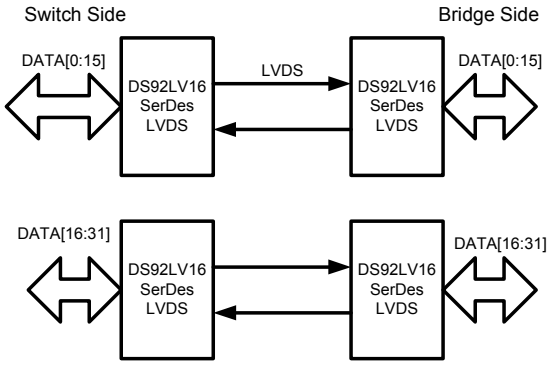

Fig.7. LVDS SerDes Interface

3.3 High Speed Connector Part

We used a ERNI ERmet ZD high speed connector [7] for LVDS board-to-board interface. The ERmet ZD is specifically designed for high speed differential signaling in telecom applications at data rates of up to 5 gigabits/second. This robust, high performance, modular connector system is also designed to be used in conjunction with the 2mm hard matric (IEC 61076-4-101) family of connectors. It shares the chassis and board design features along with common layout references.

The connector meets the electrical performance requirements of high speed, low voltage differential signaling. The ERmet ZD connector family is available in pressfit versions. The backplane module is a male pin header that has three mating levels. The

ground shield and signal pins mate sequentially at 1.5mm intervals.

The robust mechanical design and excellent signal integrity are a result of the internal differential shielding scheme and the "L" shaped male shield blades. The inherently rigid male shields stand higher than the signal pins and surround each pair. An improved guidance feature completes the rugged mechanical design.

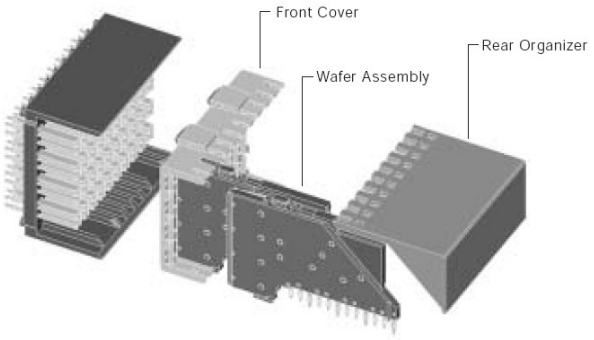

Fig. 8. ERmet ZD Connector

The design of today's high speed differential connectors is limited primarily by the electrical characteristics of the termination via geometry. The ERmet ZD utilizes an optimum grid design which significantly reduces noise within the pattern and allows generous clearance for easier routing.

3.4 Designed HomeStation Switch Board

Fig. 9 represents an experimental prototype of a Switch Board for switching 5 links.

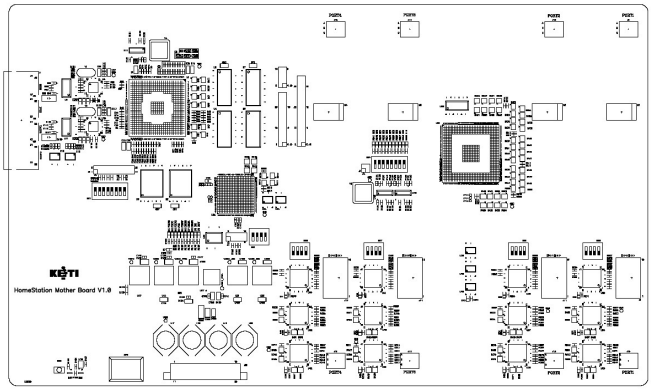

Fig. 9. Designed Switch Board

4. Design of HomeStation Bridge Board

Fig. 10 shows a hardware block diagram of the implemented HomeStation Bridge Board. The Bridge Board is composed of a HS1000 Bridge Chip Part, a IXP425 [5] Network Processor Part, a LVDS Interface Part, and a PCI Interface Part. As Fig.10 shows, a HS1000 Bridge Chip provides an interface between the Network Processor and HS5000 HomeStation Switch Chip. The bridge translates CCP traffic into a serial frame format for transmission through LVDS SerDes. Fig. 12 represents an experimental prototype of a Bridge Board for bridging HomeStation Switch to the Network Processor.

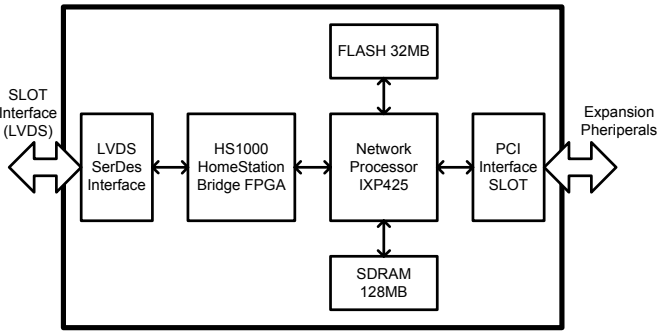

Fig. 10. Bridge Board hardware block diagram

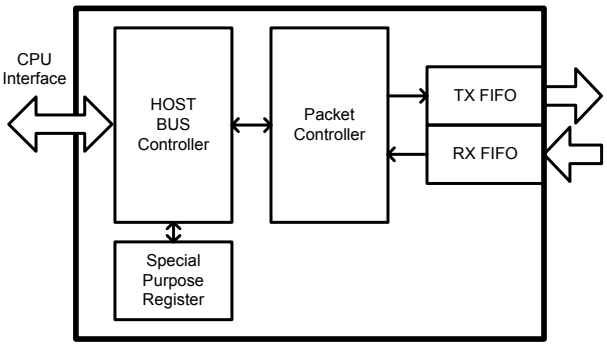

Fig. 11. HS1000 block diagram

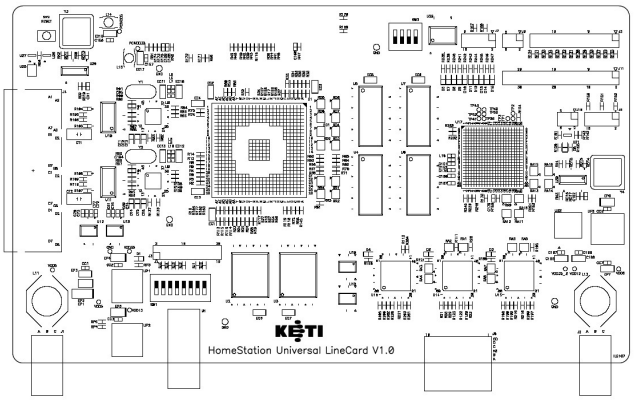

Fig. 12. Designed Bridge Board

5. Experiment

We tested the implemented Switch Board and Bridge Board using IXP425 Processor embedded in

Bridge Board. In order to verify the performance of the Serial Switched Bus, we connected a Bridge Board to the PC with serial console cable for monitoring and the IXP425 Processor in Bridge Board transmitted maximum traffic. Bridge Boards should be installed in HomeStation Switch Board first, and then the HomeStation HS1000 driver software is installed so as to allow the embedded-linux to recognize Bridge Chip. The Bridge Board is connected to the Switch Board with ERmet ZD Connector. We built custom software using HS1000 API and transmitted and received user data. We transmitted random packets and measured transmit throughput.

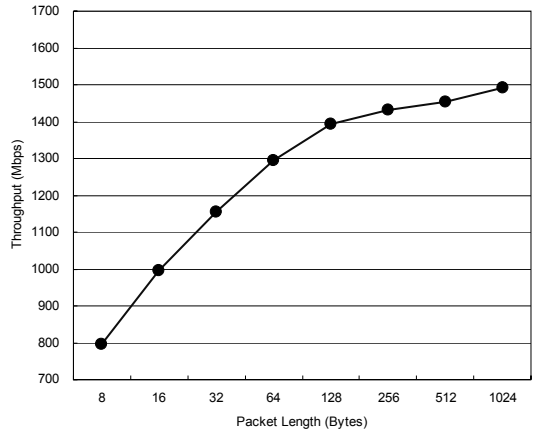

Fig. 13. Result 1

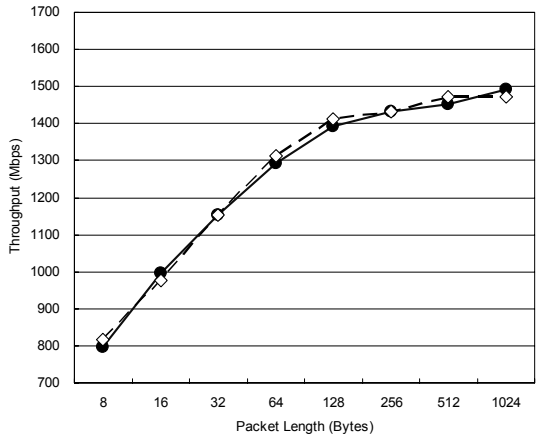

Fig. 14. Result 2

HomeStation data payloads can be up to 8Kbytes per frame and there are a processor overhead and a link overhead between a 12 bytes header and frame. Therefore, the speed of one physical HomeStation link is 2.5Gbps. To transmit 128 byte data frames, the real throughput is about 1.4 Gbps because of processor and link overheads. Fig. 13 shows the result of a throughput test between two Bridge Boards. Fig. 14 is the result of a throughput test using four Bridge Boards. There is no difference in throughput between the two Bridge Boards test and the four Bridge Boards test. These results show the characteristics of the switch fabric architecture.

6. Conclusion

In this paper, we proposed a Serial Switched Bus as a high-speed Home Network System and an evaluation method for testing the implemented system. The proposed Serial Switched Bus is designed using HomeStation-Chipset. In order to evaluate performance, the Switch Board and Bridge Board designed and implemented herein were tested by transmitting high-speed traffic.

It was verified that the HomeStation-Chipset based Serial Switched Bus is more suitable than a Parallel Bus such as PCI for construction of a high-speed Home Network System.

References:

[1] G. Shippen, " RapidIO Technical Deep Dive 1: Architecture & Protocol," *Motorola Smart Network Developers Forum*, 2003.

[2] David Bueno, Virtual Prototyping and Performance Analysis of RapidIO-based System Architectures for Space-Based Radar, *HCS Research Laboratory, University of Florida, HPEC 2004*

[3] Tom Shanley and Don Anderson, *PCI System Architecture*, Mindshare, 1999

[4] Serial Switched PCI: Expanding Architectural Capabilities.pdf, http://www.stargen.com/technology/starfabric_technology.shtml

[5] Intel IXP425 Network Processor Overview, http://www.intel.com/design/network/products/npfamily/ixp425.htm

[6] National Semiconductor LVDS Interface, http://www.national.com/appinfo/lvds/

[7] ERNI ERmet ZD Hard Metric High Speed Connector, http://www.erni.com/ermetzdfront.htd

[8] Common communication protocol for generic linkage on heterogeneous networks, *IEC TC 100 / PT 62295*, http://www.iec.ch/cgi-bin/procgi.pl/www/iecwww.p?wwwlang=E&wwwprog=dirwg.p&ctnum=2811