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Design and Analysis of a Second Order Phase Locked Loops (PLLs)

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Abstract: - This work concerns with the design and analysis of phase locked loops (PLLs). In the last decade a lot of works have been done about the analysis of PLLs. The phase locked loops are analyzed briefly, second order, third order, and fourth order. In practically the design of 1.3 GHz, 1.9V second order PLL is considered. SPICE simulation program results confirm the theory.

Key-Words: - Phase Locked Loop (PLL), Charge Pump PLL (CPPPL), Loop Filter (LF).

1 Introduction

Phase locked loops (PLLs) are extensively used in microprocessors and digital signal processors for clock generation and as a frequency synthesizers in RF communication systems for clock extraction and generation of a low phase noise local oscillator [1].

The phase PLLs was first described in early 1930s, where its application was in the synchronization of the horizontal and vertical scans of television. Later on with the development of integrated circuits, it found uses in many other applications. A PLL is a feedback control circuit, and is operates by trying to lock to the phase of a very accurate input through the use of its negative feedback path [2]. A basic form of a PLL consists of three fundamental functional blocks namely:

A Phase Detector (PD), a Loop Filter (LF), and a Voltage Controlled Oscillator (VCO).

With the circuit configuration shown in figure 1 [1,3]:

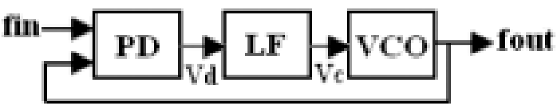

Figure 1. A basic PLL block diagram

The phase detector compares the phase of the output signal to the phase of the reference signal, and generates an output voltage, which is proportional to the phase error of the two signals. This output voltage passes through the LF and then as an input to the VCO to control the output frequency. Due to this self-correcting technique, the output signal will be in phase with the reference signal. When both signals are synchronized, the PLL is said to be in lock condition. PLL make the phase error between the two signals to be zero at this time [4].

If the difference between the input signal and the VCO is not too big, the PLL eventually locks onto the input signal. This period of frequency acquisition, is referred as pull-in time, this can be very long or very short, depending on the bandwidth of the PLL. The bandwidth of a PLL depends on the characteristics of the PD, VCO, and on the LF [2].

2 PLL Components

Phase Detector (PD)

The role of a PD in a PLL circuit is to provide an error signal, which is some function of the phase error between the input signal and the VCO output signal. Let θ_d represents the phase difference between the input phase and the VCO phase. In response to this phase difference the PD produces a proportional voltage v_d. The relation between voltage v_d, and the phase difference θ_d is shown in figure 2, The curve is linear and periodic, it repeats every 2π radians. This periodicity is necessary as a phase of zero is indistinguishable from a phase of 2π [1,2,5].

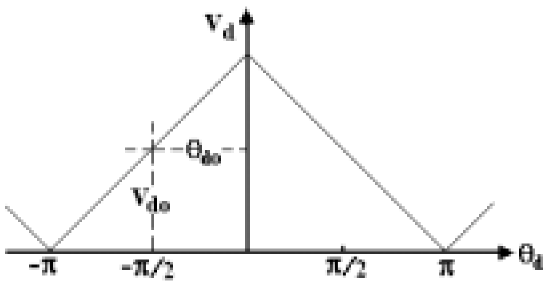

Figure 2. Phase detector characteristics

The phase difference of zero should correspond to the free running voltage v_{do} of the PD. Thus, considering this approach the phase error can be defined as [3,5]:

$$\theta_e = \theta_d - \theta_{do} \quad \cdots (1)$$

And the shifted characteristic of the phase detector is shown in figure 3:

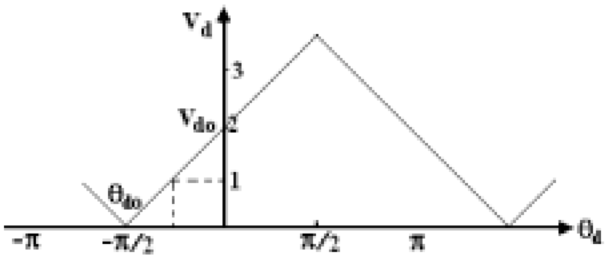

Figure 3. PD's shifted characteristic

The characteristic of PD is linear between -π/2 and π/2. The slope of the curve is constant and is equal to:

$$K_d = dv_d / d\theta_e \quad \cdots (2)$$

So for the above case $K_d = 4v/\pi$ (radian) =2.54 v/rad. Then the general model of a PD can be represented by the following equation [1]:

$$v_d = K_d\,\theta_e + v_{do} \quad \cdots(3)$$

According to equation 3, the signal flow graph of the PD can be shown as in figure 4 [4,6]:

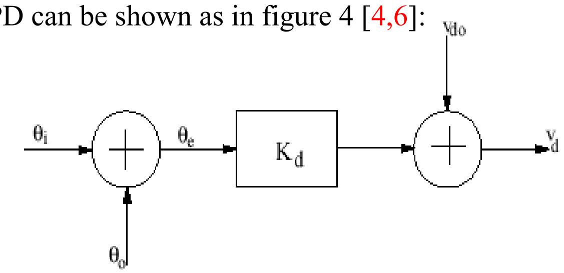

Figure 4. Signal flow model of PD

Voltage Controlled Oscillator (VCO)

A VCO is a voltage controlled oscillator, whose output frequency ω_o is linearly proportional to the control voltage v_c generated by the PD, a typical characteristic of a VCO is shown in figure5 [2,5]:

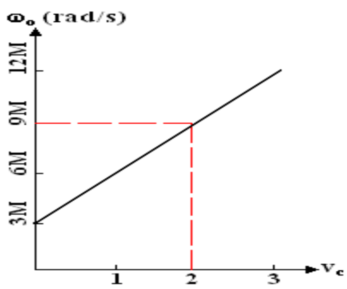

Figure 5. VCO characteristic

The slope of the curve is constant. As the v_c varies from 0 to 2 volts, the output frequency of the VCO varies from 3 Mrad/s to 12 Mrad/s. Outside this range the curve may not be linear and the VCO performance become non-linear.Depending on the specific requirements of a circuit. When the PLL is in the lock condition, the output frequency $\omega_o=\omega_i$. For an example suppose the output frequency of the VCO (ω_i) is 6 Mrad/s, from figure 5, this frequency requires that the control voltage v_c should be 1 Volts. Which means v_d=1 volts. A v_d=1requires a phase error of θ_e= -0.79 rad. This average value of the phase error is called the static phase error. The basic approach is that the static phase error should remain near zero and must not increase beyond the PD linear range of ±π/2 radians. Based on these constraints, the general strategy is that v_c should correspond to $\Delta\omega_o$, the difference between ω_o and ω_i. This result in a shifted characteristic of the VCO as shown in figure 6 [4,6]:

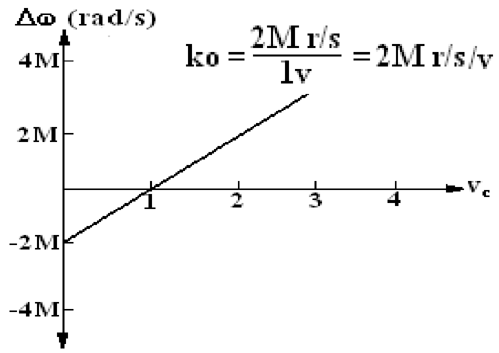

Figure 6. VCO's shifted characteristic

The plot is $\Delta\omega_o$ vs v_c. So $\Delta\omega_o$=0 corresponds to v_c = Vco. The slope of this curve is the VCO gain K_o and is given by [5]:

$$K_o = d\Delta\omega_o / dv_c \quad \cdots(4)$$

Then the general mode of VCO is given by:

$$\Delta\omega = K_o\,(v_c - v_{co}) \quad \cdots(5)$$

And the VCO signal flow graph is shown in figure 7, (where V_{co} is the control voltage, when PLL is in lock)

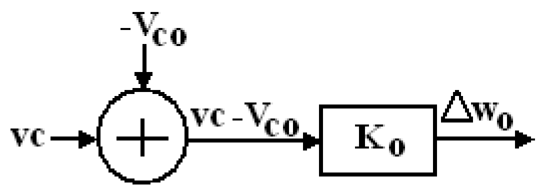

Figure 7. Signal flow model of VCO

Loop Filter (LF)

The filtering operation of the error voltage (coming out from the PD) is performed by the loop filter (LF). The output of PD consists of a dc component superimposed with an ac component. The ac part is undesired as an input to the VCO; hence a low pass filter is used to filter out the ac component. LF is one of the most important functional blocks in determining the performance of the loop. A LF introduces poles to the PLL transfer function, which in turn is a parameter in determining the bandwidth of the PLL. Since higher order loop filters offer better noise cancellation, a loop filter of order 2 or more are used in most of the critical application and PLL circuits especially in RF communication systems [5].

3 PLL with “divider” block

Figure 8 shows a basic PLL block diagram with an additional block called divider has been added in the feed back loop. Dividers are frequently used in PLLs circuits especially in frequency synthesizer PLLs [2]. With the divider-by-N in the feed back path, the output frequency is equal to N times the reference frequency. For applications without a divider, N is set to be one.

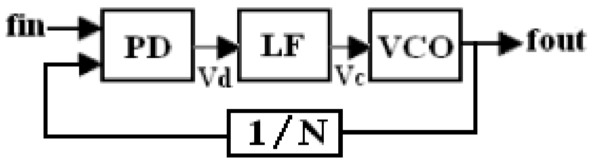

Figure 8. A basic PLL block diagram with divider block

4 Charge Pump PLLs

Charge pump based PLLs (CPLL) are widely used as clock generators in a Varity of applications including microprocessors, wireless receivers, serial link transceivers, and disc drive electronics [7]. One of the main reasons for the widely adopted use of the CPLL in most PLL systems is because it provides the theoretical zero static phase offset, and arguably one of the simplest and most effective design platforms. The CPLL also provides flexible design tradeoffs by decoupling various design parameters such as the loop bandwidth, damping factor, and lock range. A typical implementation of the CPLL consists of a phase detector (PD), a CP, a loop filter (LF), and a (VCO). Figure 9 shows the CPPL block diagram [6]:

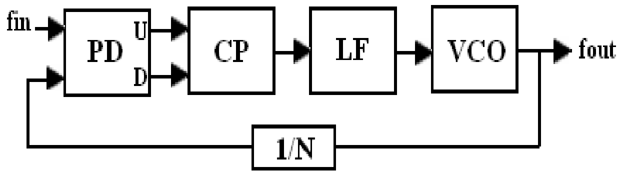

Figure 9. PLL with charge pump (CPLL)

A charge pump serves to convert the two digital output signals Q_A and Q_B of the PD into charge flows whose quantity is proportional to the phase error. A passive filters then shape the output current signal of the charge pump to suppress the useless messages buried in that signal [7,8].

A PD together with a charge pump and a single capacitor C_P as the loop filter are shown in figure 10, with the corresponding time-domain response shown as well. As ‘A’ has a higher frequency than ‘B’ or has the same frequency as B but with a leading phase, the charge pump sources a constant- valued current I_1 through switch S_1 into the capacitor, and the output voltage increases steadily. Similarly, if the frequency of input A is lower or the phase is lagging, the output waveform will be a steadily downward one [1,8].

At the time when the inputs are equal or same, both Q_A and Q_B will have pulses of short duration. In this case, if the currents of the two current sources are the same in quantity, as indicated in Figure 10, at the time that both S_1 andS_2 are on, the current sourced by I_1 is exactly sunk by I_2. Thus no net current will flow through CP and V_{out} remains unchanged as in the case when both S_1 and S_2 are off. [2,8]:

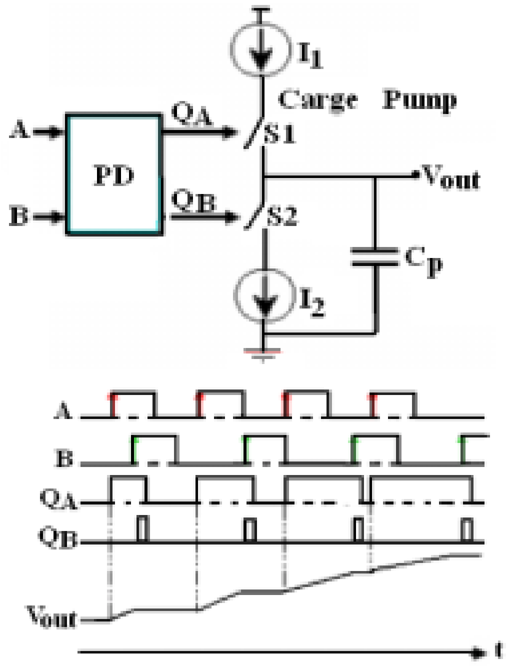

Figure 10. Block diagram of PD with CP, and the timing diagram

The PD and the CP can be together characterized as:

$$I_{PUMP} = I.\ \theta_e / 2\pi \quad \cdots (6)$$

Where I_{PUMP} is the output current of CP, $\theta_e=\theta_A-\theta_B$ represents the phase error between two PD inputs and $I = I_1 = I_2$ is the current value of the two current sources in the charge pump, and this is an approximate representation. We note that the charge pump is a discrete-time system, and it provides good approximation only when the loop bandwidth is much less than the input reference frequency [5,8].
The single-capacitor unstablilize the closed-loop. To avoid instability, a resistor R_P in series with C_P is added (Figure11). The transfer function of the resultant loop is [2,7]:

$$F(S) = R_P + \frac{I}{SC_P} \quad \cdots (7)$$

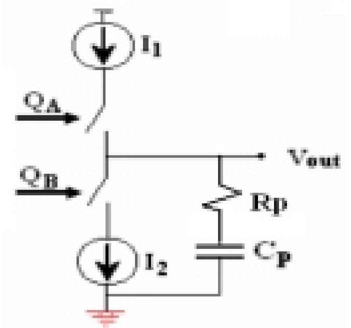

Figure 11. CP with additional zero.

5 Charge Pump PLL Design

The first-order loop filter in figure 11 yields to a second-order loop transfer function, it may not be adequate if more strict noise performances are requested. Loop parameter and component values for the second-order PLL are introduced and determined. By the same way the required value of components for higher-order loop filters can be determine.

Second-Order PLL

The noise transfer function equation 8 is the loop transfer function of the second order PLL [5.9]

$$H(S) = \frac{\Phi_{out}(S)}{\Phi_{in}(S)} = \frac{\frac{I_p}{2\pi}.F(S).\frac{2\pi K_{vco}}{S}}{1+G(S)}$$

$$= M.\frac{2\xi\{\frac{S}{\omega_n}\}+1}{\{\frac{S}{\omega_n}\}^2+2\xi\{\frac{S}{\omega_n}\}+1} \quad \cdots (8)$$

M is the nominal modulus value.

K_{VCO} and M are usually predetermined. If the used VCO is a discrete commercial IC, we can find the value of K_{VCO} in data sheets, otherwise, K_{VCO} can be found from experimental or simulation results.
M is determined by the operating frequency and the channel bandwidth. This leaves us only three parameters to determine: I_P, C_P and R_P [4,9]
Here, a part of equation 8 is restarted here:

$$\xi = \frac{R_p}{2}\sqrt{\frac{I_pK_{VCO}C_p}{M}}, and \omega_n = \sqrt{\frac{I_pK_{VCO}}{MC_p}} \quad \cdots (9)$$

I_p is set to the order around 100 µA to 1mA if external passive filters are used [9]. For on-chip filters, where capacitance values should be limited for chip area concerns, I_p decreased by about a order since the pump current will not flow outside the chip in case that the package parasitic influence the effective filter component values. The natural frequency ω_n is usually chosen to be about or less than 1/10 of the input frequency for the sake of stability [1,10]. With ω_n, I_P, K_{VCO} and M known, the capacitance value C_p can be determine. The damping factor ζ is also set to 0.707 for the flat loop response, and thus the resistor value R_P could be found.

The 2nd order charge-pump PLL (CPLL) design methodology is summarized in the following points:
a) The VCO gain (K_{VCO}) can be found from simulation results, experimental results or data sheets. b) The natural frequency should (ω_n) is set to be about or less than 1/10 of the input frequency. C) The pump current (I_P) should be set to be around 100 µA to 1mA if the filter is off-chip. An on-chip filter decreases the value of I_P so that reasonable trade-off between chip area and pump current is reached. d) A nominal modulus value M can be select according to the system to be applied to. e) The damping factor ζ is set to be 0.707. f) The values of C_P and R_P can be calculated according to Equation 9 [3,11,12].

6 Simulation Results

In this paper a 1.3-GHz second-order phase locked loop, with 1.9-V power supply are simulated, and the block diagram is shown in figure 12:

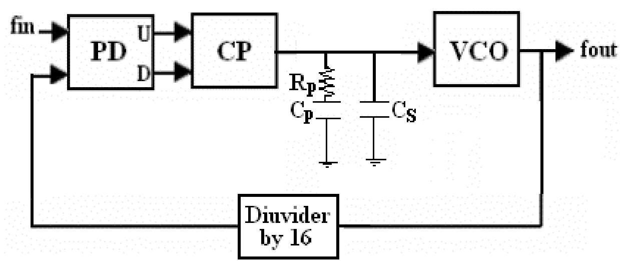

Figure 12. The simulated CPLL block diagram

Table1 shows the loop parameters of the phase-locked loop. The capacitor is at the value of 100pF, the charge pump current is at the value of tens of micro Ampere. The divider divide-ratio should be as small as possible to suppress the jitter. The damping factor ζ is set to 0.7 [11,12] to acquire the open loop phase margin of 68° .The ω_n should be as large as possible if the reference clock is ideal [1,12].

R_p	2.1KΩ	I_p	20μA
C_p	200pF	Divider N	16
C_s	20pF	ω_n	3.72Mrad/s
K_{VCO}	20μA	ζ	0.7

Table 1. PLL loop parameters

6.1 Phase detector simulation results

Fig. 13 shows the simulation results of the phase detector. The phase supplied by two clocks with little phase difference, and the CP output is measured. The charge pump output is connected to 1pF capacitor and the initial voltage is set at 0.74V. The current of the charge pump is 20μA. After 58 pumps the voltage variance is measured of the charge pump output. The deadzone of this charge pump is zero. Although the deadzone is zero, there exists a phase offset, which is 1.5ps.

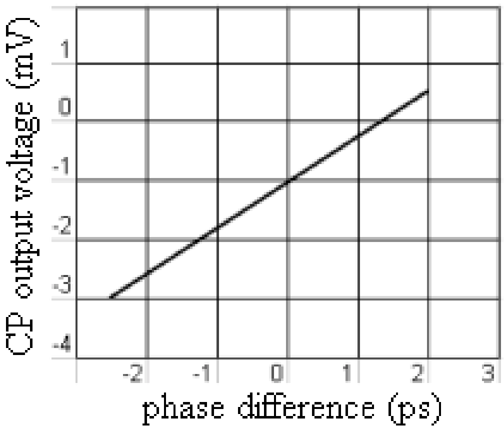

Figure 13. Deadzone of the phase detector

6.2 Charge pump simulation results

Figure 14 shows the simulation result of the CP and the LF. The current of the CP is 20μA and the smaller MOS capacitor in the loop filter is about 20pF. In the duration of 200ps charging time the voltage is rise by 0.2mV. It means that the equivalent capacitance of the smaller MOS capacitor is 20pF

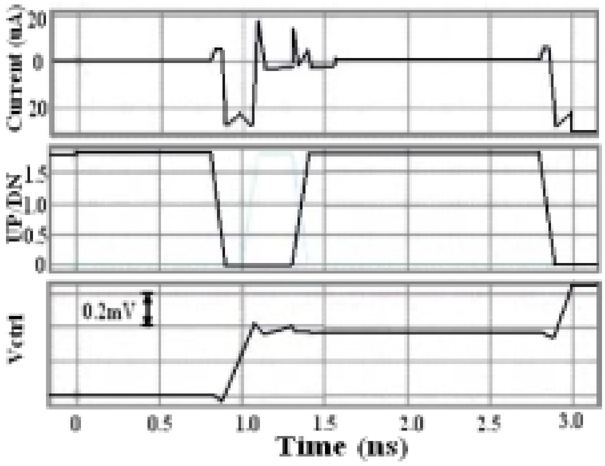

Figure 14. Simulation results of CP and LF

6.3 VCO simulation results

The operation range of the VCO is shown in Table2. For the VCO three cases are simulated as shown in Table 2. In the case of A/1.98v/30oC, the oscillating frequency is above 1.35GHz. In the case of C/1.7/55oC, the oscillating frequency is below 1.35GHz. The table also shows the gain of voltage-controlled oscillator in the case of B/1.9V/36oC.

Vctrl / Tech.	1.1V	0.7V	0.3V
A/30°C /1.98V	0.67GHz	*	*
B/36°C /1.9V	0.32GHz	1.3GHz	2.51G Hz
C/55°C /1.7V	*	*	1.27G Hz

Table 2. The frequency of VCO vs.process variation

6.4 Divider simulation results

Fig. 15 shows the simulation results of the divider. The divider can successfully divide the frequency of 1.3 GHz to 75MHz.

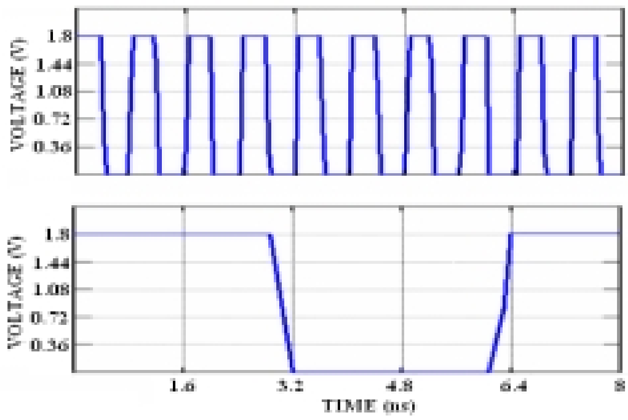

Figure 15. Simulation results of the divider

6.5 PLL simulation results

Figure 16 shows the simulation results of the designed phase locked loop. The specifications are shown in table 3:

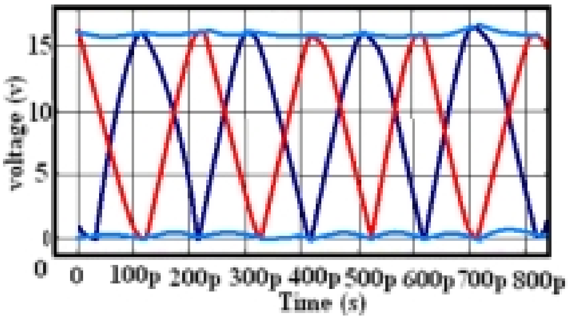

Figure 16. PLL simulation results (Clock jitter)

Operating Frequency	1.3GHz
Supply voltage	1.9V
Power consumption	30.1 mW

Table 3. PLL design specification

7 Conclusion

PLLs are widely used in communication systems, microprocessors and digital designs. Designing and analysis of PLLs is very important because a number of performance metrics have to be taken into account simultaneously such as VCO gain (K_{VCO}), natural frequency (ω_n), charge pump current (I_p), damping factor (ζ), and the loop filter parameters. The design is complicated because these metrics are effect on the improvement and PLLs applications. The charge pump gain and the loop filter resistance are the two parameters that can be utilized to improve the noise at low frequency offsets and large frequency offsets respectively. In this work the PLLs are analyzed mathematically and graphically, with the steps to a proper 2nd order PLL design.

The PLL design by this method has a high performance due to accuracy in progress, and can significantly improve the PLL applications such as frequency synthesizer which is widely used in high-speed data processing, and it usually implemented by PLLs because of low implementation cost and excellent noise performance. [2]

Spice simulation program shows the satisfactory results of this work.

Therefore, this technique to analysis and design of PLLs can be considered as a critical performance constraint for any PLL applications.

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