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Noise Analysis of Phase Locked Loops

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Abstract: - This paper analyzes phase locked loops (PLLs) from the noise point of view. It is important to now how different noise sources affect the noise performance of the output signal. The sources of noise may be classified into two types, the noise at input, and the noise of VCO. Since a number of performance metrics have to be taken into account simultaneously for the design of low noise PLLs, so the design is very complex because these metrics are not independent of each other. This paper addresses the problem of noise and its reduction to improve the design and operation of PLLs, the simulation results show the effect of the components in both time and frequency domain.

Key-Words: - phase locked loop, charge pump, phase noise.

1 Introduction

Phase and delay locked loops (PLL and DLL) are extensively used in microprocessors and digital signal processors for clock generation and as frequency synthesizers in RF communication systems for clock extraction and generation of a low phase noise local oscillator signal from an on-chip voltage controlled oscillator (VCO) which might have a higher open-loop noise performance [1].

PLLs are also used to maintain a well defined phase and hence frequency relation between two independent signal sources. The general block diagram of a PLL is shown in figure 1, which is consisting of a phase detector (PD), a loop filter with transfer function H(s), a voltage controlled oscillator (VCO) and a frequency divider denoted as 1/N [2]. The PD generates an output proportional to the phase difference between its two inputs. The first input, V_{in}, is usually generated by an external or reference oscillator, while the second input is directly related to the output of the VCO, V_{out}. Under locked condition the negative feedback adjusts the dc value of the VCO control voltage in such a way that the two inputs of the phase detector have a constant phase difference and hence are exactly at the same frequencies. This occurs when the VCO output frequency, f_o is N times the input frequency f_{in} [2].

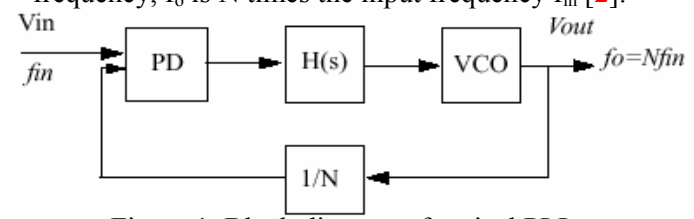
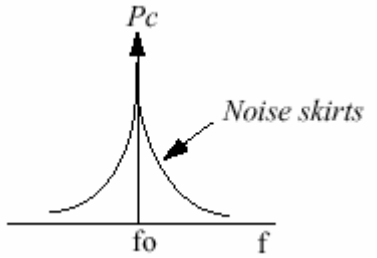


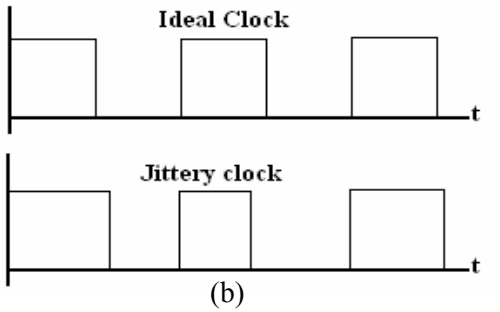
Figure 1. Block diagram of typical PLL

The proper selection of PLL parameters ensure that the PLL locks to an integer multiple of the input frequency, noise sources in the circuit cause perturbations in the VCO control voltage, resulting in variations in output frequency. Hence the output power spectrum will contain other frequency components in the vicinity of f_o. This is shown in figure 2, where the output spectrum exhibits 'skirts' around f_o [1,3].

The ratio of the output power at a frequency offset Ef to the power at f_o is defined as phase noise. In the time domain, the noise sources disturb the regularity in zero crossings of the output signal causing it to exhibit jitter. Due to negative feedback, the PLL inherently corrects the drift in output frequency thus limiting the jitter. As a result, the jitter cannot increase definitely with time as in open loop oscillators. However, noise sources at different points in the PLL dominate at different offset frequencies, thus complicating the PLL design for low noise [2,3,4].



(a)



(b)

Figure 2. Frequency and time domain effects of noise sources in PLLs. (a) Phase noise in output power spectrum. (b) Jitter in time domain.

2 Noise Performance of PLLs

PLLs are suffers from noise introduced at input or generated by the other building blocks. It is important to now how different noise sources affect the noise performance of the output signal. The sources of noise may be classified into two types, the noise at input, and the noise of VCO [5,6].

Noise at input is due to the reference oscillator, the phase frequency detector and the frequency divider. The model shown in Figure 3 characterizes the noise due to the reference oscillator and the frequency divider. With the open-loop transfer function, the closed-loop transfer function with a first-order loop filter can be expressed as [7]:

$$H(s)=\frac{\theta_{out}(s)}{\theta_{in}(s)}=\frac{\frac{I_P}{2\pi}\cdot F(s)\cdot\frac{2\pi K_{VCO}}{s}}{1+G(s)}$$

$$=\mathrm{N}\cdot\frac{2\xi\left(\frac{s}{\omega_n}\right)+1}{\left(\frac{s}{\omega_n}\right)^2+2\xi\left(\frac{s}{\omega_n}\right)+1}$$

… (1)

$$where\quad \xi=\frac{R_P}{2}\sqrt{\frac{I_P K_{VCO} C_P}{\mathrm{N}}}$$

$$and\quad \omega_n=\sqrt{\frac{I_P K_{VCO}}{\mathrm{N}C_P}}$$

Equation 1 is a standard form of a second-order low-pass system where damping factor ζ and natural frequency ω_n are very clear and ω_n does not equal to the unity-gain frequency K. In a physical sense, the low-pass characteristic not only suppresses high-frequency noises but also tracks low- frequency fluctuations in phase at input, which is just the sense of "phase- locked". If the former is to be optimized, which is usually the case in practice, the loop band width K and the divider modulus N must be minimized [6,7].

As for the noise generated at the phase detector, the result is similar as to the loop transfer function, with the noise source regarded as pump current EI_p will be added to the input of the loop filter, and it can be represented by [8]:

$$H(s)=\frac{\theta_{out}(s)}{\Delta I_P}=\frac{F(s)\cdot\frac{2\pi K_{VCO}}{s}}{1+G(s)}$$

$$=\frac{2\pi}{I_P}\cdot\mathrm{N}\cdot\frac{2\xi\left(\frac{s}{\omega_n}\right)+1}{\left(\frac{s}{\omega_n}\right)^2+2\xi\left(\frac{s}{\omega_n}\right)+1}$$

… (2)

Where ζ and ω_n are the same as those in Equation 1. The only difference is the dc gain whose value implies that the pump current must be maximized in order to have large attenuation at high frequencies.

Figure 3 shows the PLL noise transfer function from VCO to output [6,9].

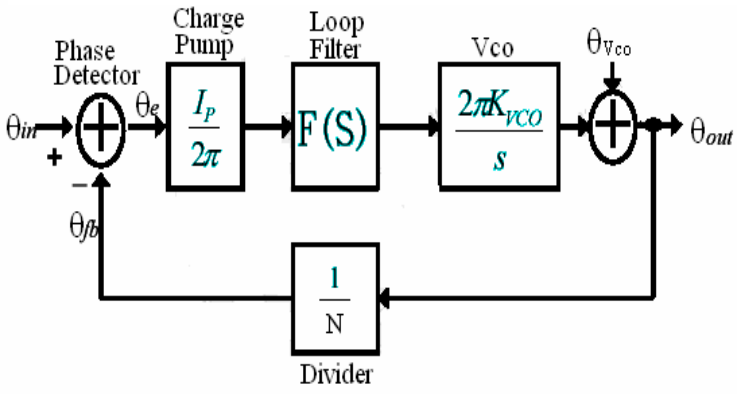


Figure 3. PLL noise transfer function from VCO to output.

The phase noise of the VCO can be modeled as an additive component ρ_{VCO} as shown in Figure 3. With ρ_{in} and ρ_{VCO} uncorrelated, ρ_{in} is set to zero to compute the transfer function from ρ_{VCO} to ρ_{out}. Then we have [10],

$$H(s)=\frac{\theta_{out}(s)}{\theta_{VCO}(s)}=\frac{1}{1+G(s)}$$
$$=\frac{\left(\frac{s}{\omega_n}\right)^2}{\left(\frac{s}{\omega_n}\right)^2+2\xi\left(\frac{s}{\omega_n}\right)+1} \quad \ldots (3)$$

This is a high-pass transfer function with two zeros at zero frequency and two poles at the same frequencies as those of Equations 1and 2. This transfer characteristic is completely opposed to that of the noise at input, which implies that the requirements for better noise performance may contradict those stated earlier. To be more precisely, for high frequency noise to be attenuated, the loop band width should be as large as possible [11].
These analyses bring out the trade-off between the suppression of noise at input and of VCO. A rough decision of the loop bandwidth might go as: If the VCO employed has bad noise performance, the loop bandwidth should be maximized; if the VCO provides a good intrinsic noise performance, the loop bandwidth should be minimized to suppress the noise at the reference oscillator [6,13].

3 Simulation Results

The schematic diagram of the phase locked loop simulation circuit is shown in the Figure 4, and the overall simulation results are as shown below:

Design analyzed at 01/13/06 12:32:28

PLL Chip is ADF4107
VCO is V637MC02
Reference is custom

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 561MHz

Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
100	-87.86	-116.3	--	-87.97	-104.2
1.00k	-83.25	-98.26	--	-86.66	-86.15
10.0k	-92.34	-104.4	--	-97.52	-94.31
100k	-124.5	-126.0	--	-134.8	-131.6
1.00M	-145.8	-145.8	--	-174.8	-171.5

Reference Spurious
Noise and Jitter Calculations include the first 10 ref spurs
First three spurs: -300 dBc -300 dBc -300 dBc

Phase jitter using brick wall filter
From 10.0 kHz to 100 kHz
Phase Jitter 0.13 degrees rms

----End of Frequency Domain Results ----

Transient Analysis of PLL
Frequency change from 500MHz to 630MHz
Simulation run for 1.49ms

Frequency Locking
Did not lock to within 1.00 kHz
Did not lock to within 10.0 Hz

Phase Locking (VCO Output Phase)
Did not lock to within 10.0 deg
Did not lock to within 1.00 deg

Lock Detect Threshold
Lock Detect output did not pass 2.50 V

---- End of Time Domain Results ----

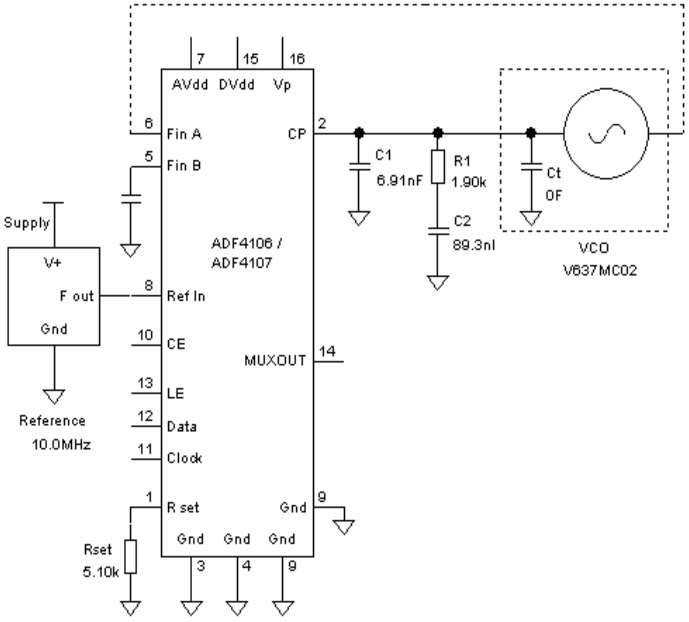


Figure 4. Schematic diagram of the PLL simulation circuit

Components simulation results:

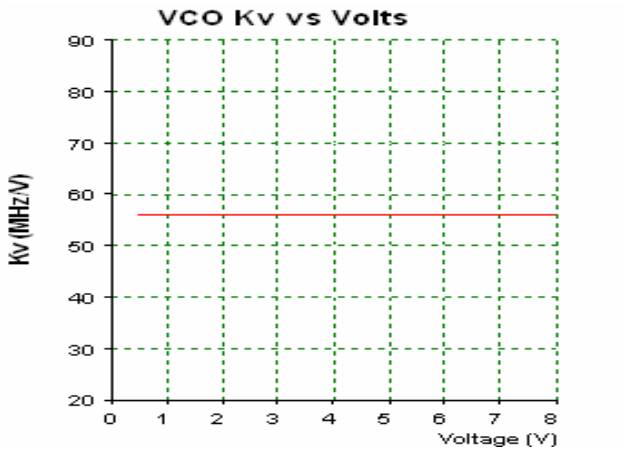


Figure 5.VCO (kv) vs Volts

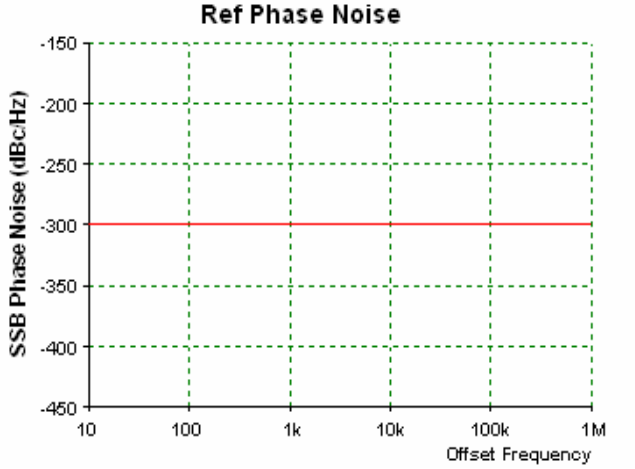


Figure 8. Reference phase noise

Time Domain Simulation Results:

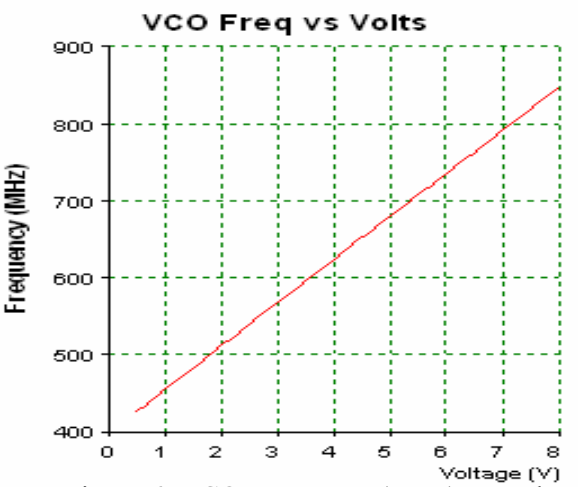


Figure 6. VCO Frequency (MHz) vs Volts

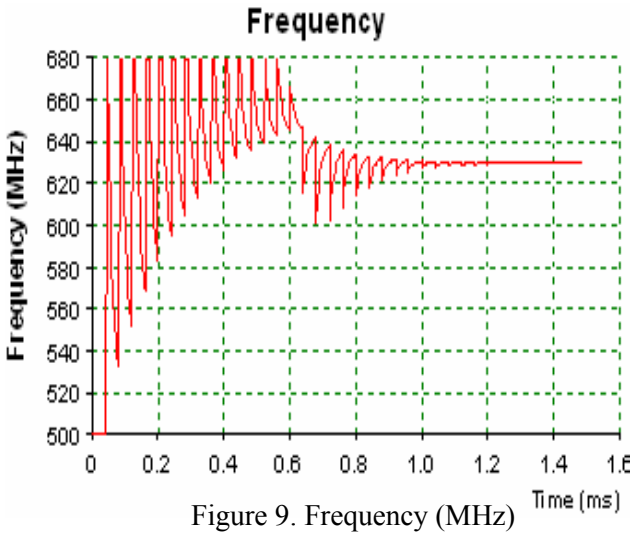


Figure 9. Frequency (MHz)

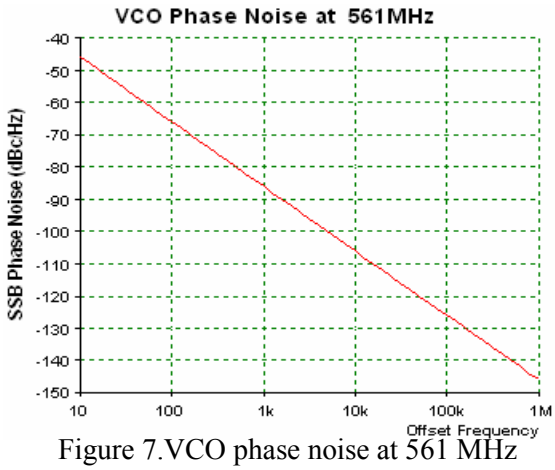


Figure 7.VCO phase noise at 561 MHz

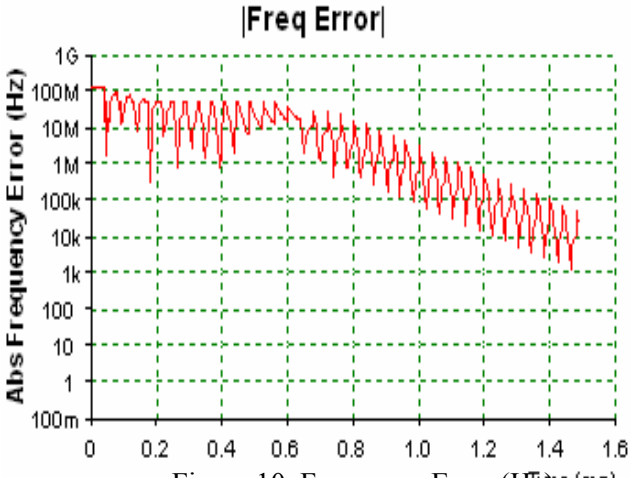


Figure 10. Frequency Error (Hz)

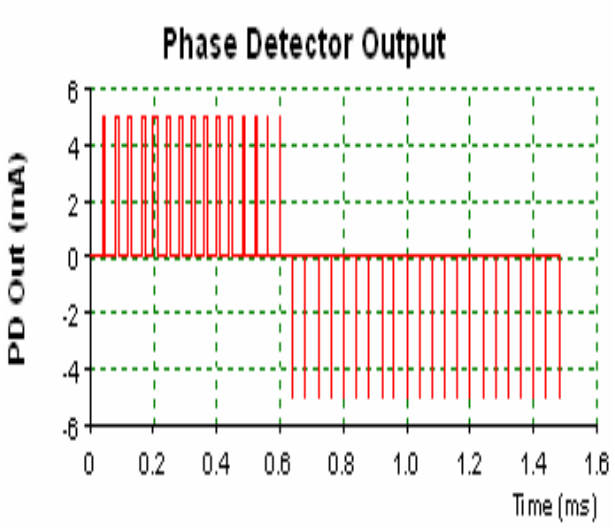


Figure 11. Phase detector output (mA)

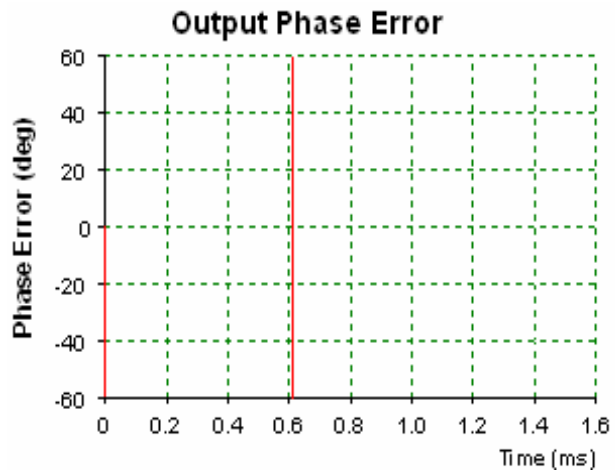


Figure 12. Output phase error (deg)

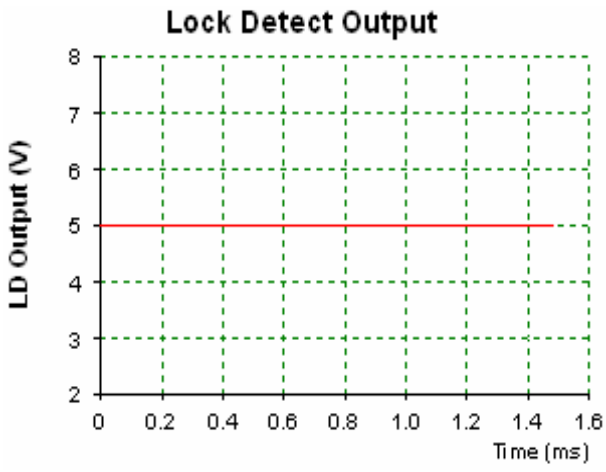


Figure 13. Lock detect output (V)

Frequency Domain simulation Results:

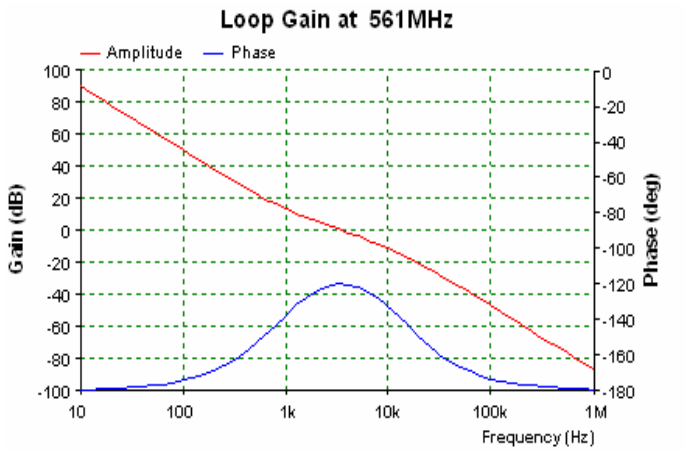


Figure 14. Loop gain at 561 MHz

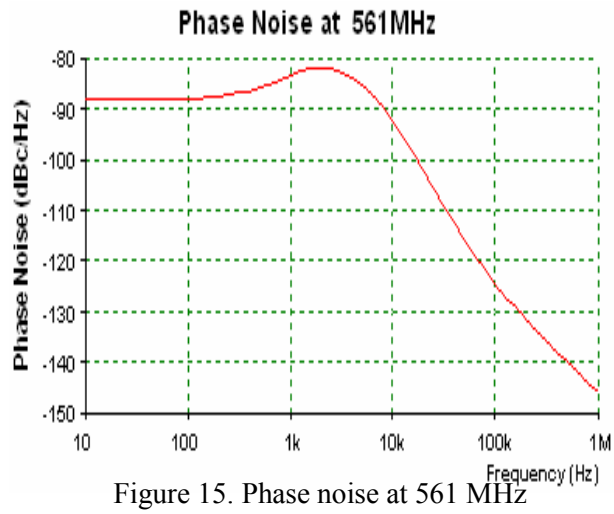


Figure 15. Phase noise at 561 MHz

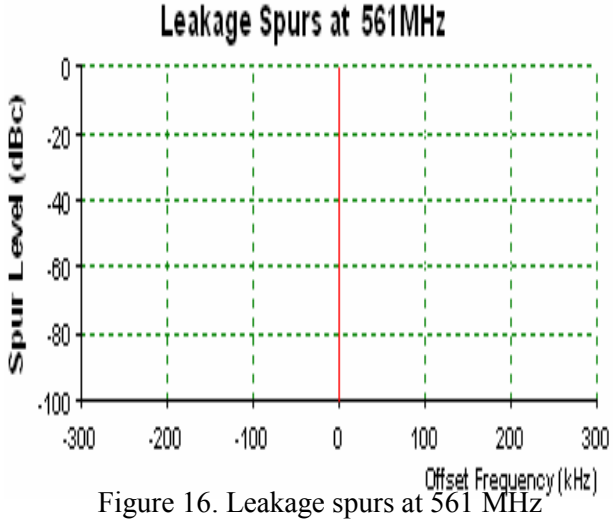


Figure 16. Leakage spurs at 561 MHz

4 Conclusion

Designing low noise PLLs as mentioned is very challenging since a number of performance metrics have to be taken into account simultaneously such as stability and reference spurs. The design is complicated because these metrics are not independent of each other; an improvement in one effect results in degradation in the other.

Noise analysis of PLLs in this paper brings out the trade-off between the suppression of noise at input and of VCO. A rough decision of the loop bandwidth might go as: If the VCO employed has bad noise performance, the loop bandwidth should be maximized; if the VCO provides a good intrinsic noise performance, the loop bandwidth should be minimized to suppress the noise at the reference oscillator.

From the simulation results it is clear that, increasing the charge pump gain promises low phase noise at low offset frequencies but has a detrimental effect on the reference spurs in the frequency spectrum. Reducing the resistance in the loop filter reduces the phase noise at high frequency offsets but affects the stability of the PLL.

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