A 10Gbps Analog Adaptive Equalizer and Pulse Shaping Circuit for Backplane Interface

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Abstract: - The speed of serial interface through a backplane channel suffers severe ISI (Inter Symbol Interference) caused by the limited bandwidth of the channel. In order to overcome the bandwidth limit, a pulse shaping circuit or an adaptive equalizer is used. This paper presents the comparison between two approaches. Prototype chip is designed for 10Gbps serial data communication through a 34-inch transmission line with a 0.18-μm CMOS process. The simulation and layout results show that the adaptive equalization has superior performance in power consumption, silicon area and the jitter performance.

Key-Words: - Adaptive equalizer, backplane, ISI, pulse shaping, serial interface

1 Introduction
By CMOS technology improvements, clock speed of primary circuits such as a CPU (Central Processing Unit), and a DSP (Digital Signal Processor) have continuously increased and attained several GHz operation. At this point, speed-up of a total system is bounded by the chip-to-chip or board-to-board communication speed. In case of several GHz data communications on a backplane channel, PCB lines have a number of imperfections such as flat loss, frequency dependent loss due to its limited bandwidth, and reflection due to the impedance mismatch.

These non-idealities degrade signal integrity considerably and hence pulse shaping or adaptive equalization techniques are frequently employed to compensate the bandwidth limit as depicted in Fig. 1. [1] Although digital implementation is preferred for relatively low speed communication, analog implementation is employed in several GHz data communication such as OIF CEI 6+, OIF CEI 11+, XAUI, and so on [2].

This paper presents an analog adaptive equalizer and a pulse shaping circuit in operating 10Gbps data on 34-inch backplane interface. Section II describes the channel model and section III describes the architecture of the pulse shaping filter and the adaptive equalizer. Section IV proposes the circuits and section V provides the simulation results. The conclusion is provided in section VI.
The channel has about 5dB attenuation at 1GHz and 40dB attenuation at 10GHz. This limited bandwidth causes long tail in impulse response as shown in Fig. 2(b). The ISI components for preceding symbol sequences are -11dB, -18dB, -23dB and so on.

This long tail of impulse response causes ISI and completely closes the eye opening in the received signal as shown in Fig. 2(d). The closed eye means that the received data cannot be recovered by a conventional clock data recovery circuits.

\[ X(n) = \sum_{k} h_k D_{n-k} = h_0 D_{n-1} + h_1 D_{n-2} + \cdots + h_{N-1} D_0. \]  

(1)

The multiplication is implemented by changing the polarity of the binary data. The optimal coefficients are obtained by the inverse of the channel model that is obtained from a system identification algorithm [9]. Since the characteristic of the channel can not be obtained in the transmitter side, the pulse shaping is applicable only for the known fixed channel. In this paper, a 3-tap FIR filter is chosen through the simulation using the channel model described in section II.

Fig. 3 shows the architecture of the FIR pulse shaping filter whose impulse response is described by,

\[ X(n) = \sum_{k} h_k D_{n-k} = h_0 D_{n-1} + h_1 D_{n-2} + \cdots + h_{N-1} D_0. \]  

(1)

Either a FIR (Finite Impulse Response) type filter or a IIR (Infinite Impulse Response) type filter can be employed for bandwidth compensation. The FIR type is preferred for the pulse-shaping due to the simplicity of implementation [3][4] while IIR type is commonly used for the adaptive equalizer due to simplicity of the adaptation circuitry [5]-[8].

Fig. 3 shows the architecture of the FIR pulse shaping filter whose impulse response is described by,
block is implemented with an array of differential pairs whose output currents are summed at the output node. The filter coefficients are realized by applying the bias current that corresponds to each coefficient.

The adaptive equalizer consists of a controllable HPF, a comparator and two square difference circuits. A novel controllable HPF is proposed in this work as shown in Fig. 6(a). A trans-conductance from the input to the output node is given as

\[ G_m = \frac{1}{R_1} + \frac{g_m (sR_2C_1 + 1)}{sR_2C_1 + 1 + g_m R_2/2}. \]  

(2)

Therefore, The DC gain is decided by the variable resistor \( R_1 \) and the zero of the filter is decided by the variable capacitance \( C_1 \). It is clear that the pole is located at higher frequency than the zero. The variable resistor is implemented with NMOS transistor operating in linear region. The variable capacitor is implemented with PMOS-type MOS capacitor whose source, drain, and bulk are tied together. In order to realize floating capacitor, two MOS capacitors are employed, whose gate is used as control node.

The square difference and integrator is implemented as shown in Fig. 6(b). The differential output current of the squarer is given by as [5]

\[ I_{d1} - I_{d2} = \frac{KW}{L} \left( v_{m,1}^2 - v_{m,2}^2 \right). \]  

(3)

The second part of the circuit transforms the voltage signal into a current signal, and then integrates that currents.

Fig. 6(c) shows comparator schematic which makes equalization output signal into digital signal.

As the output of the HPF is large enough, cascade of two differential amplifiers without inductive peaking technique is enough.
5 Simulation and layout results

The pulse shaping filter and the adaptive equalizer with the proposed controllable HPF are designed for 10-Gbps operation using 0.18um CMOS process.

Fig. 7 shows the SPICE simulation result of the designed controllable HPF. Fig. 7(a) shows the DC gain controllability without changing the zero frequency and the bandwidth. The control range of DC gain is 1~1.3. Fig. 7(b) shows zero controllability without changing the DC gain and the bandwidth. The control range of zero frequency is 500MHz ~ 1GHz.

![Image](a) Output waveform of the pulse shaping filter.

![Image](b) Received signal with the pulse shaping.

![Image](c) Received signal without pulse shaping.

![Image](d) Recovered signal with the equalizer.

Fig. 8. Transistor level simulation result of designed pulse shaping and equalizer circuits.

The designed pulse shaping circuit and the adaptive equalizer are simulated using 10Gbps pseudo random bit sequence data on the channel model that is described in section II.

Fig. 8(a) shows the output waveform of the pulse shaping filter. Although the high frequency component is significantly emphasized in the transmitter side, the received signal shows appropriate eye diagram as shown in Fig. 8(b). Note that the amplitude of the received signal is 1/5 of the transmitted signal. This means that an additional amplifier is required in the receiver side because the amplitude of the transmitter is limited by the current driving capability of the driver and the EMI radiation on the channel. Fig. 8(c) shows the received signal without pulse shaping. Despite the severe ISI in the received signal, the output of the equalizer’s HPF shows wide and clear eye opening with large signal amplitude.

Fig. 9 shows the layouts of the designed pulse shaping circuit and the adaptive equalizer. The area of the pulse shaping circuit and the adaptive equalizer are 1650×1450 and 1600×700, respectively.

![Image](a) Layout of the designed pulse shaping circuit.

![Image](b) Layout of the designed adaptive equalizer.

Fig. 9. The layouts of the designed circuits.
Table 1 summarizes the performance of the pulse shaping and the equalization. The equalizer output has 8-ps peak-to-peak jitter and 350-mV amplitude while the pulse shaping provides 10-ps peak-to-peak jitter and 30-mV amplitude. The equalizer is not only superior in the performance but the power consumption and the silicon area as well.

<table>
<thead>
<tr>
<th></th>
<th>Equalizer</th>
<th>Pre-emphasis</th>
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<tbody>
<tr>
<td>Process</td>
<td>0.18 □ CMOS</td>
<td>0.18 □ CMOS</td>
</tr>
<tr>
<td>Amplitude</td>
<td>350mV</td>
<td>30mV</td>
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<tr>
<td>Peak-to-peak jitter</td>
<td>8ps</td>
<td>10ps</td>
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<tr>
<td>Area</td>
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<td>2.24mm²</td>
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<tr>
<td>Power consumption</td>
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<td>60mW</td>
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</table>

6 Conclusion

This paper proposed a controllable HPF for 10 Gbps equalizer. The comparison of pulse shaping and the equalization is obtained from the designed circuits. The simulation results clearly showed that the equalization is a better choice than the pulse shaping for 10Gbps serial interface on a band limited channel.

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References: