High manufacturing-defect tolerance optically programmable architecture

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Abstract: Optically reconfigurable gate arrays, which consist simply of a holographic memory, a laser diode array, and a gate array VLSI, have a perfect parallel programmable capability. Even if a gate array VLSI includes defective areas, the perfect parallel programmable capability allows perfectly avoidance of those defective areas; instead, the remaining area on the gate array is used. Therefore, the architecture enables fabrication of large die VLSI chips and even wafer scale integrations using the latest processes with a high fraction of defects. Moreover, holographic memory is well-known to have high defect-tolerance because each bit of a reconfiguration context can be stored in the entire holographic memory and the damage of some component rarely affects its diffraction pattern or reconfiguration context. Therefore, the architecture has a high manufacturing-defect tolerance. In this paper, the high manufacturing-defect tolerance of optically programmable architectures is clarified using a single context prototype optically programmable architecture, which combines a liquid crystal spatial light modulator as a holographic memory, a He-Ne laser, and a perfectly parallel optically programmable gate-array VLSI.

Key–Words: High manufacturing-defect tolerance, Field programmable gate arrays, Optical reconfiguration, Holographic memory, Optically reconfigurable gate arrays

1 Introduction

Recently, as VLSI process technologies have progressed, the defective fractions of VLSIs have increased and die sizes have decreased to an increasing degree. However, to implement large systems onto VLSI, the demand for a non-defective large die VLSI chip is increasing day-by-day.

In the earliest use of field programmable gate arrays (FPGAs) [1, 2, 3], FPGAs were anticipated as defect-tolerant devices that allow inclusion of defective areas on the gate array because of their programmable capability. However, that hope was shattered because defects of a serial configuration line caused severe impairments that prevented programming of the entire gate array. To use a gate array perfectly, including its defective areas, a perfect parallel programmable capability is required that uses no serial transfer.

On the other hand, optically programmable gate arrays (OPGAs) [4, 5, 6] have been developed as faster context-switching devices than FPGAs. An OPGA comprises a holographic memory, a vertical cavity surface-emitting laser (VCSEL) array, and a gate-array VLSI. An 80-gate-count VLSI was implemented and 100-context-switching was attained. However, serial transfers between photodiode arrays and gate arrays are used in OPGA-VLSI. For that reason, a perfect parallel programmable capability was not realized. In addition, up to now, the manufacturing-defect tolerance of OPGAs has never been discussed.

Therefore, this paper proposes a high manufacturing-defect tolerant, perfectly parallel optically programmable architecture using a holographic memory, a laser source, and a bit-by-bit programmable gate array VLSI. It was fabricated to realize a perfect parallel programmable capability,
as shown in Fig. 1 [7, 8, 9]. The perfectly parallel programmable gate array VLSI allows perfect avoidance of its faulty areas; it instead uses the remaining area. Moreover, holographic memories are well known to have a high defect-tolerance. Therefore, the architecture enables the use of a large die VLSI chip and even entire wafers, including fault areas, realizing extremely high-gate-count VLSIs. This paper presents a high manufacturing-defect tolerant optically programmable architecture. The optically programmable architecture includes a liquid crystal spatial light modulator as a holographic memory, a He-Ne laser, and an optically programmable gate array VLSI. In addition, the manufacturing-defect tolerance and its effectiveness are discussed using experimental results.

2 Defects and failure of programmable gate arrays

As VLSI process technologies have progressed, the defective fraction of VLSIs has grown increasingly; moreover, the die size has also decreased to an ever greater degree. The number of non-defective chips in a wafer is estimated as

\[ N = \frac{A_{\text{wafer}}}{A_{\text{chip}}} (1 - DA_{\text{chip}}), \]

where \( A_{\text{chip}} \) and \( A_{\text{wafer}} \) respectively represent the chips’ die size and wafer size; \( D \) is the wafer’s defect density [10, 11]. Increasing the chip size increases the defective fraction. Therefore, to reduce the number of defective chips, the chip size \( A_{\text{chip}} \) is scaled down. However, the demand for large systems on a chip increases day-by-day.

The defects and failure of programmable devices can be classified mainly into three groups for study: manufacturing defects, run-time defects, and gradual failure. Among them, this study specifically examines the manufacturing-defect tolerance. In the case of manufacturing defects, a spare row method like that used for dynamic random access memories is a useful method for using defective chips [12, 13], in which the spare rows of a gate array are used instead of defective rows by swapping them with a laser beam machine. However, hardware redundancy entails hardware overhead. In addition, perfect avoidance of all defective areas on a chip can not be expected: inevitably, some chips must be discarded. In stark contrast, an optically programmable architecture never requires such hardware overhead, a process with a laser beam machine, or discarded chips.

3 ORGA architecture

3.1 VLSI part

The manufacturing-defect tolerances of previously proposed OPGAs [4, 5, 6] were not good because of serial transfers between photodiode arrays and programmable gate arrays, as with FPGAs. However, our newly developed ORGA-VLSIs with a perfectly parallel programming capability [7, 8, 9] have high manufacturing-defect tolerance. In the ORGA-VLSIs, serial transfers were perfectly removed and optical reconfiguration circuits including static memory functions and photodiodes were placed near and directly connected to programming elements of a programmable gate array VLSI. An array of optical reconfiguration circuits is shown in Fig. 2. In the reconfiguration procedure, a reconfiguration context is received by photodiodes and is stored instantaneously in toggle flip-flops when a configuration clock (CCLK) is raised. It is then supplied to a gate array of an ORGA-VLSI chip. The toggle flip-flops are used for temporarily storing one context and realizing a bit-by-bit configuration. Using this architecture, the optical configuration procedure for a gate array can be executed perfectly in parallel.

A block diagram of a gate array, a logic block, a switching matrix and an I/O block of a fabricated ORGA-VLSI chip are shown in Fig. 3. The ORGA-VLSI was fabricated using a 0.35 \( \mu \)m three-metal CMOS process [7, 8, 9]. In this fabrication, the photodiode size and the distance between the photodiodes were designed, respectively, as 25.5 \( \times \) 25.5 \( \mu \)m\(^2\) and 90 \( \mu \)m to ease optical alignment. The total number of photodiodes is 340. The gate count of the gate array is 68. The ORGA-VLSI chip consists of four logic
blocks, five switching matrices, and 12 I/O bits. Functionality of the VLSI chip is fundamentally identical to that of typical FPGAs. Nevertheless, each programming element of all blocks of the ORGA-VLSI is connected to an optical reconfiguration circuit to detect an optical configuration context. The logic block consists of a four-input-one-output look-up table (LUT) and a delay flip-flop with a reset function. These functions are optically reconfigurable using 40 optical reconfiguration circuits. Similarly, switching matrices can be reconfigured optically through 12–24 optical connections. Each I/O block is also controlled through nine optical connections. Thereby, the VLSI part can achieve a perfectly parallel configuration.

3.2 Optical part

Figure 1 depicts an overview of the optical component of ORGAs. The ORGA optical system comprises laser sources, an optical holographic memory, and a programmable gate-array VLSI. The holographic memory can store numerous reconfiguration contexts.

Figure 3: A photograph of an ORGA-VLSI board with a fabricated ORGA-VLSI chip and a CAD layout of the ORGA-VLSI. The ORGA-VLSI was fabricated using a 0.35 µm three-metal 4.9 × 4.9 mm² CMOS process chip. The gate count of a gate array on the chip is 68. In all, 340 photodiodes were used for optical configurations.

Figure 4: Gate-array structure of a fabricated ORGA. Panels (a), (b), (c), and (d) respectively depict block diagrams of a gate array, an optically reconfigurable logic block, an optically reconfigurable switching matrix, and an optically reconfigurable I/O bit.
Figure 5: System configuration for a holographic memory. The z axis is chosen as the optical axis of the ORGA system.

The reconfiguration contexts are addressed by a laser array that is mounted on the top of the holographic memory. The diffraction pattern from a holographic memory is receivable on a photodiode-array that is implemented in the programmable gate array of an ORGA-VLSI as a reconfiguration context. Therefore, this architecture enables perfectly parallel reconfiguration. Although an ORGA architecture has numerous reconfiguration contexts, in this paper, the defect tolerance is discussed under a single configuration condition: the number of contexts is limited to one.

3.3 Computer-generated hologram

Here, a hologram for ORGAs is calculated as a thin holographic medium with the setup shown in Fig. 5. A collimated plane reference wave propagates in the holographic plane. The size of the holographic medium is $H_x \times H_y$; the other area on the holographic plane is assumed as opaque, where $H_x$ and $H_y$ are the transverse dimensions and the thickness of the medium is neglected. The holographic medium is made up of rectangular pixels of size $\delta_x \times \delta_y$ on the $x_0 - y_0$ holographic plane. The pixels are assumed as analog values. In addition, the input object is made up of rectangular pixels of size $d_x \times d_y$ on the $x_1 - y_1$ object plane. The pixels can be modulated to be either on or off. The intensity distribution of a holographic medium is calculable as the following equation:

$$H(x_0, y_0) \propto \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} O(x_1, y_1) \sin(kr) dx_1 dy_1,$$

where $O(x_1, y_1)$ is a binary value of a reconfiguration context, $k$ is the wave number, and $L$ is a distance between the holographic plane and the object plane. The value $H(x_0, y_0)$ is normalized as 0–1 for the minimum and maximum intensities as

$$H'(x_0, y_0) = \frac{H(x_0, y_0) - H_{min}}{H_{max} - H_{min}}.$$

Finally, the normalized image $H'$ is used for implementing a holographic memory.

4 Manufacturing-defect tolerance of ORGAs

As explained previously, an ORGA consists of laser sources, an optical holographic memory, and a programmable gate-array VLSI. To estimate the manufacturing-defect tolerance of ORGAs, the manufacturing-defect tolerance for each component must be discussed. The following subsections include discussions of the manufacturing-defect tolerances of a laser component, an optical holographic memory, and a programmable gate-array VLSI.

4.1 Laser part

In an ORGA, several discrete semiconductor lasers or vertical cavity surface-emitting lasers (VCSELs) are used for switching configuration contexts. A few such laser sources might have manufacturing defects. However, the manufacturing defects of laser sources can be avoided easily by not using the contexts that correspond to the defective lasers. An ORGA has many reconfiguration contexts. Therefore, a few reductions of reconfiguration contexts are beyond consideration. Programmers need only to avoid the defective part when programming reconfiguration contexts for a holographic memory. Therefore, if ORGAs have absolutely correct programming capability for a holographic memory to avoid the defective part, the manufacturing-defect tolerance of laser sources can be neglected perfectly. In ORGAs, the manufacturing-defect tolerance of laser sources depends on the manufacturing-defect tolerance of a holographic memory.

4.2 ORGA-VLSI part

The avoidance method of a gate array’s defective areas is shown in Fig. 6. Here, it is assumed that a defective optically reconfigurable logic block (ORLB)
Figure 6: Defective area avoidance method on a gate array. Here, it is assumed that a defective optically reconfigurable logic block (ORLB) exists, as portrayed in the upper area of the figure. In this case, the defective area is avoided perfectly through the use of parallel programming by using the other components, as shown in the lower side of the figure.

exists in a gate array, as shown in the upper part of Fig. 6. In that case, another implementation is available, as shown in the lower side of Fig. 6. Using bit-by-bit reconfigurable optically reconfigurable gate array VLSIs, the defective area is perfectly avoided by using the other components. In this example, we assumed a defective area of only one optically reconfigurable logic block. Of course, for the other cells, optically reconfigurable switching matrices, and optically reconfigurable I/O blocks, a similar avoidance method can be adopted. For that reason, the architecture has a high manufacturing-defect tolerance.

Therefore, along with the laser part, if ORGAs have absolutely correct programming capability for a holographic memory, the manufacturing-defect tolerance of an ORGA-VLSI part can be neglected as well as programmable devices without defective areas. In ORGAs, the manufacturing-defect tolerance of an ORGA-VLSI also depends on the manufacturing-defect tolerance of a holographic memory.

4.3 Holographic memory

To program a large-die VLSI chip, high manufacturing-defect tolerance is necessary for a holographic memory to store several bits of a context. In addition, as described previously, the manufacturing-defect tolerances of the laser part and an ORGA-VLSI part depend on the manufacturing-defect tolerance of the holographic memory. Therefore, for ORGAs, the manufacturing-defect tolerance of the holographic memory is extremely important. In this section, the manufacturing-defect tolerance of a holographic memory is presented experimentally.

4.3.1 Simulation results

An impulse noise simulation was executed to confirm the manufacturing-defect tolerance of a holographic memory. The x-direction and y-direction calculation resolutions of an object or an ORGA-VLSI were defined respectively as 18 um and 18 um. Because the respective x-direction and y-direction distances between photodiodes of the target fabricated ORGA-VLSI are 90 um and 90 um, each pixel was defined as \(5 \times 5\) pixels, as shown in Fig. 8 (a). A context consists of \(20 \times 17\) bits for 340 programming elements of the target ORGA-VLSI. The resolution of a holographic memory was designed as 14 um \(\times 14\) um, which is equal to the resolution of a liquid-crystal spatial light modulator (LC-SLM). The pixels of the holographic memory were \(300 \times 300\). The target laser wavelength was 633 nm. The distance L between an object or an ORGA-VLSI and a holographic medium was designed as 10.0 cm. The intensity distribution of the holographic memory was normalized to 256 gradations, which is identical to that of an LC-SLM. The
Figure 8: Simulation and experimental results. Figure (a) shows a sample reconfiguration context. Figure (b) shows the normalized intensity distribution of a normally calculated holographic memory. Figures (c) and (d) respectively depict a simulation result and an experimental result of an image reconstructed from the holographic memories of Fig. (b).

The normalized intensity distribution of the holographic memory is shown in Fig. 8 (b), which was calculated from the context of Fig. 8 (a). The reconstructed context pattern is shown in Fig. 8 (c). Figure 9 (b) shows that to confirm tolerance for transmission defects or opaque defects of a holographic memory, 100 impulse noises are applied onto a normally calculated holographic memory of Fig. 8 (b). However, the reconstructed context pattern in Fig. 9 (c) has a very high contrast, which is equivalent to that of Fig. 8 (c). Therefore, we are able to present that a holographic memory has high manufacturing-defect tolerance.

4.3.2 Experimental Results

Figure 7 shows our constructed experimental system using a liquid crystal spatial light modulator (LC-SLM), a He-Ne-laser, and the fabricated ORGA-VLSI chip. Usually, a three-dimensional holographic memory is used as holographic material. However, LC-SLM was introduced here to implement a noise-applied holographic memory. A He-Ne laser is used as a light source: its wavelength is 633 nm and its power is 20 mW. The He-Ne laser light is made incident to a LC-SLM as collimated light using a collimator with two lenses and a pinhole. The LC-SLM panel is used as a holographic memory, as mentioned above. The LC-SLM is a projection TV panel (L3P07X-31G00; Seiko Epson) which is a 90° twisted nematic device with a thin-film transistor. The panel consists of 1024 × 768 pixels; each is 14 × 14 \( \mu m^2 \). The LC-SLM is connected to the evaluation board of L3B07X-E10A (Seiko Epson). The board input is connected to the external display terminal of a personal computer. Programming for the LC-SLM is executed with 256 gradation levels using a personal computer. The ORGA-VLSI was placed at a distance of 10.0 cm from the LC-SLM. Holographic patterns extracted by simulation results, as shown respectively in Figs. 8(b) and 9(b), were displayed on the LC-SLM. The diffraction patterns from the holographic memories are presented in Figs. 8(d) and 9(d), which were received on an ORGA-VLSI. Both reconstructions using a normal holographic memory and an impulse noise holographic memory were successful.

Figure 9: Impulse noises simulation and experimental results. Figure (a) shows the sample context similarly to Fig. 8. Figure (b) shows the normalized intensity distribution of a calculated holographic memory to which impulse noises are applied. Figures (c) and (d) respectively show a simulation result and an experimental result of an image reconstructed from the holographic memories of Fig. (b).
4.3.3 Discussion

A single bit of a semiconductor memory device is stored in a single-bit memory circuit. In contrast, in holographic memory, a single bit of a reconfiguration context is stored in the entire holographic memory. As presented above, the manufacturing-defect tolerance of ORGAs depends only on the holographic memory component. However, we have confirmed that 0.1% impulse noise never affects the configuration and the optical holographic memory has high defect-tolerance. Therefore, finally, we could conclude that ORGAs have high defect-tolerance.

5 Conclusion

Optically reconfigurable gate arrays have perfect parallel programmable capability. This paper described that, even if a gate array VLSI includes defective areas, the perfect parallel programmable capability allows perfect avoidance of defective areas and uses the remaining area of a gate array VLSI. Therefore, the architecture enables fabrication of large-die VLSI chips and wafer-scale integrations using the latest processes with a high defective fraction. We have demonstrated that a holographic memory has high defect-tolerance because each bit of a configuration context can be stored in the entire holographic memory and damage to a part of it rarely affects its diffraction pattern or reconfiguration context. Finally, we conclude that the architecture has a high manufacturing-defect tolerance.

In the future, optically reconfigurable gate arrays will be a type of next-generation three-dimensional (3D) VLSI chip with extremely high gate count and a high manufacturing-defect tolerance.

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