A 5 GHz CMOS Low Power Down-conversion Mixer for Wireless LAN Applications

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Abstract: - This paper describes a 1.5-V 5 GHz I/Q down conversion mixer in a 0.18-µm CMOS process. The mixer achieves a conversion gain of 12.7 dB within 1-dB compression point ($iC_{1dB}$) of -15.83 dBm. It also achieves a double side band (DSB) NF of 13.5 dB. The mixer's IIP3 is -5.94 dBm. The mixer consumes only 5.72 mA of current from a 1.5-V power supply.

Key-Words: - Analog RF-CMOS, IEEE 802.11a, IEEE 802.11b, front-end, receiver, wireless LAN

1 Introduction

CMOS RF integrated circuits (RFICs) for wireless communication have gained much interest due to their potential low cost and the prospect of system level integration. In the 5 GHz frequency range, the IEEE 802.11a wireless LAN (WLAN) standard which is based on an orthogonal frequency division multiplexing (OFDM) modulation technology is compatible with data rates up to 54 Mbps [1]. The IEEE 802.11a WLAN standard provides nearly five times the data rate and has ten times the overall system capacity as currently available IEEE 802.11b WLAN systems [2]. With these upgrading features, IEEE 802.11a WLAN became a promising standard in the personal communication market. The needs for low voltage operating RF chips with lesser power consumption and higher performance/price ratio have led to increased interest and research of the front-end receiver. The mixer is one of the most challenging building blocks in the front-end receiver. It provides frequency translation from RF to the intermediate frequency (IF) called “down-converter”, or from IF to RF called “up-converter”.

Fine line CMOS mixers with gate length of 0.18-µm or below open up the possibility of low power consumption compared to the bipolar and BiCMOS technologies. They must also equal and surpass the low noise figure of these technologies. Among the various CMOS mixer research, a passive linear mixer [3] can have very high IIP3 with the sacrifice of high NF. Such a high NF will limit the signal to noise ratio of a front-end. Using the current mode multiplication technique [4], a CMOS active mixer may be designed for low NF but its conversion gain will be very low. To overcome this low conversion gain, a very high gain LNA is required to minimize the effect of noise degradation in the overall receiver design. This work is for the design and implementation of an active double-balanced I/Q mixer which overcomes the limitations as stated before as well as achieves equal or better performances than the existing bipolar and BiCMOS technologies [5, 6].

This work

![Fig. 1. Front-end block of an IEEE 802.11a WLAN receiver](image)

A simplified block diagram of the front-end of an IEEE 802.11a WLAN receiver is shown in Fig. 1. In this architecture, the RF amplification and
downconversion are the most critical to implement in CMOS. This paper describes the design and implementation of a mixer in a 0.18-µm CMOS process which is quite competitive with today's bipolar implementation. The prototype design represents a first step toward a fully integrated monolithic WCDMA/UMTS. The rest of the paper is organized as follows. Design details is described in section 2. Section 3 presents simulations of samples. Finally, section 4 derives the conclusion.

2. Circuit Implementation

Fig. 2 shows the proposed double balance active down-conversion mixer. The design is based on a complex version of the ubiquitous current-steering CMOS form. The mixer structure is chosen to be a differential double balanced mixer for its inherited insensitivity to LO-IF isolation. It also suppresses common-mode substrate noise and interference. The mixer comprises differential pairs driver stages (Q1-Q6) and four differential switching quad (Q7-Q14).

Fig. 2. The proposed double balanced down-conversion mixer

Each four mixer FETs of the switching quad are attached to the drain of each driver stage. For large signals, the voltage at the common source follows the highest of the four instantaneous gate voltages. The LO waveforms of the gates consists of four sine waves spaced apart in phase by 90°. The driver stage amplifies the RF signals to compensate for the attenuation due to switching process, and to reduce the noise contribution from the switching quad. The two I and Q mixers are resistively loaded because of reducing flicker noise at outputs. In order to improve both the gain and the linearity of the mixer, we consider a CMOS $g_m$ cell technique which is a counter part of the bipolar multi-tanh principle [7], is shown in the Fig. 2. The matching devices Q1-Q2 and Q5-Q6 (32-µm /0.18-µm) form the CMOS $g_m$ cell with input transconductors Q3-Q4 (50-µm /0.18-µm). In this configuration, each input differential pair behaves a reasonably linear transconductance over a small specified input voltage range. The overall transconductance is the sum of the individual offset transconductance and can be made roughly constant over an almost arbitrary large range of input voltage. We also used a constant CMOS $g_m$ bias circuit which is shown in Fig. 8 for making the circuit independent of temperature and voltage variations. At the transconductor output, the signal is split into I and Q paths inside the mixer. Independent I and Q LO signals (off-chip) are applied to create quadrature baseband paths. The transconductor output current splits between I and Q paths such that all of the transconductor current goes to the I branch at the instance that the Q branch core is in its transitional state, and vice versa. Hence, each switching pair which does not have any current at the balanced point periodically lowers the noise figure to ensure low noise figure and the improvement in the conversion gain. At the output, the load capacitors are chosen such that it works as low pass filter with cut-off frequency at 35 MHz to remove the strong out-of-band signals from the input to the baseband filters.

3. Simulation Result

The mixer was simulated with the cadence spectreRF simulator. Figures 3 to 6 show simulation results of the mixer. The mixer achieves a conversion gain of 12.7 dB with an RF input and an LO input return losses of -29.97 dB and -12.54 dB, respectively. It can be seen from Fig. 4 that I/Q gain mismatch is almost negligible. The mixer also achieves an NF of 13.5 dB at 1 MHz output frequency. As two-tone testing, two tones are located at 5.77 GHz and 5.76 GHz, respectively. Fig. 6 illustrates IIP3 measured to be -5.94 dBm. Table I summarizes the performance of the mixer and compares it with ones in [5, 6, 8].
Fig. 3. $S_{11}$ at the RF input and LO input of the proposed mixer

Fig. 4. Conversion gain of the proposed mixer

Fig. 5. NF of the proposed mixer

Fig. 6. IIP3 of the proposed mixer

Fig. 7. Layout of the proposed mixer

Fig. 7 shows the layout of the mixer. The layout including the RF pads uses a compact area of $1.3 \times 1.6 \text{ mm}^2$. For the purpose of improving isolation of the mixer, the strategy is to make the layout...
symmetrical as much as possible. The mixer core devices are laid out with common centroid symmetry. To reduce the gate and substrate resistance of the mixer input transistor, multiple fingers (2.5-µm width each) with gate contacts at both sides have been used. All the RF inputs and outputs use ground-signal-ground configuration with shielded pads. The mixer including the bias circuit is biased in its nominal 8.58 mW regime i.e., drawing a nominal bias current of 5.72 mA from a 1.5-V power supply.

4 CONSTANT g_m BIASING

The robustness in the performance of the mixer depends primarily on the transconductance of the transistors Q_1- Q_6 in Fig. 2. Taking into account global process spread, supply voltage variations 10% and temperature variation (-45°C to 85°C), the worst case performance are: gain = 10 dB NF = 20 dB, and IIP3 = -5 dBm at a supply voltage of 1.5-V and with a current consumption of 7.5 mA.

Better circuit performance can be obtained using a constant g_m bias circuit. Fig. 8 illustrated the constant g_m biasing circuit for the mixer. In this circuit, a bias current that makes the transconductance, g_5, proportional to a reference conductance, \(I/R\). The transistor M_5 is much wider than M_6 so that it operates on a very small over-drive voltage. The positive feedback loop implemented by the current mirror formed by M_1,M_3 ensures that M_5 conducts the stable bias current. The driver of the mixer intercepts this bias current via a V_{th} current reference formed by M_10,M_11. To make the current through M_11 proportional to V_{th}, we choose M_11 wider than M_10. To make the current through M_11 proportional to V_{th}, we choose M_11 wider than M_10. This current provides the bias current for mixer input devices through M_14, so that all bias voltages track V_{th}, thus providing a measure of stability.

The biasing circuit stabilizes the mixer amplification. Taking into account global process spread, supply voltage variations 10% and temperature variation (-45°C to 85°C), the worst case performance are: gain = 12 dB NF = 17 dB and IIP3 = -5.6 dBm at a supply voltage of 1.5-V and with a current consumption of 6.5 mA.

5. Conclusion

This paper presents an I/Q mixer for wireless LAN applications in a TSMC 0.18-µm CMOS process. The mixer achieves an IIP3 of -5.94 dBm. Operating at 1.5-V supply voltage, the mixer provides a conversion gain of 12.7 dB within 1-dB compression point of -15.83 dBm. The I/Q mixer including bias circuit consumes only 8.58 mW of power which makes it the lowest power consumption of the I/Q mixers. In the noise response, the mixer acquires of 13.5 dB noise figure. Hence, in the 5 GHz band, the 1.5-V mixer provides high gain with low power consumption, low noise figure and moderate linearity. Thus this mixer can be used to achieve amplification as well as frequency translation in IEEE 802.11a WLAN front-end which requires RF designers to design fully integrated, low noise and low power consumption architectures for SoC applications. In the future work, this mixer with high IIP2 will be integrated with an LNA to build a direct conversion IEEE 802.11a WLAN front-end receiver.

References:


