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Investigation of Single Cell Delay and Delay Mismatch in Ring Oscillator Based Test Structure

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Abstract: - In previous work, we presented a test structure based on ring oscillator (RO) to measure single cell delay and delay mismatch, which can provide reliable information on intra-die and inter-die parameter variations. A delay cell of the configurable RO in the test structure considered for the computation technique consists of an inverter and a conducting transmission gate between adjacent cells. This paper will analyze the effects on delay cells of the transmission gates connecting to the output of inverters included in the active RO and investigate in depth delay mismatch in this RO based test structure. Monte Carlo simulation results reveal that the computation technique is applicable to derive delay mismatch between delay cells. A large number of post-layout simulations for different layout structures with different number of cells and different transistor sizes have been performed to analyze delay mismatch related to interconnect and device parameter variations.

Key-Words: - Delay Measurement, Delay Mismatch, Ring Oscillator, Process Variations, Intra-Die Fluctuations, Inter-Die Fluctuations.

1 Introduction

The consideration of device fluctuation is an important theme in designing high performance CMOS integrated circuits, particularly on the deep submicron technology. As polysilicon gate lengths have decreased below the wavelength of light used in the optical lithography process, the importance of intra-die fluctuations of channel length have become more than that of inter-die fluctuations. Especially in high speed digital circuits, delay mismatch due to intra-die variation cannot be neglected.

In many digital circuits such as Delayed Locked Loop (DLL) and Time-to-Digital Converter (TDC) involving delay chains composed of identical delay elements, the mismatches in the propagation delay of individual delay elements cause timing uncertainty. In DLL circuits, a Voltage Control Delay Line (VCDL) that consists of several tuneable delay cells is used to generate multiple phases of the low frequency clock, which are combined into one high frequency clock. The stochastic mismatch between the cell delays causes clock skew of the intermediate clock phases, leading to spurious peaks in the output frequency spectrum of the output signals. Similarly, the delay-chain-based TDC circuits such as the Vernier Delay Line (VDL) [1][2] time measurements are achieved with a timing resolution that depends on the propagation delays of the delay cells in the chain. Any delay mismatch between delay cells affects the circuit resolution, degrading the accuracy of the measurement. On the same token, in frequency synthesis circuits, like Fraction-N Synthesis circuits [3][4], a ring oscillator (RO) is usually used to generate desired clock signal. However, delay cell mismatch due to interconnect and process variations causes timing uncertainty to the synthesized signal, leading to jitter. All these detrimental factors are due to delay mismatch between identical delay cells in the same delay chain or RO. Hence measuring single cell delay and delay mismatch are very important to intra-die variation characterization.

Earlier attempts for characterizing delay mismatch due to process variations use statistical analysis based on averaging [5][6] instead of single cell delay values. These solutions use a large number of RO on the test chip, and characterize performance variations by measuring frequencies of ROs. Such methods may be very efficient to characterize variability through a wafer (die-to-die fluctuations), but is not suitable to characterize intra-die delay mismatch caused by interconnect and random device parameter variations. Hence the thorough estimation and characterization of the intra-die process variations and mismatch may not be obtained. Another approach to measure cell delay based on random sampling is reported in [7][8]. The values of input and output voltages are sampled at a random time instant and two boolean random variables S_{in} and

S_{out} respectively are obtained. It is demonstrated that the probability Pr (S_{in} =1, S_{out} =0) is proportional to the delay of the rising edge through the cell. Similarly, the probability Pr (S_{in}=0, S_{out} =1) is proportional to the delay of the falling edge. With this method, a large number of events have to be generated to achieve high measuring precision. The generation of such large number of events in turn would require large number of counters for each cell. With 0.18um CMOS technology, delay mismatch between 2-transistors inverters can reach as low as a few picoseconds requiring sub-picoseconds measurement resolution. Using code density test to characterize the delay mismatch would need quite considerable number of counters, making the technique area consuming. In our previous work [9], we presented a test structure based on modified RO. Single cell delay and delay mismatch can be derived only by measuring RO periods with high resolution oscilloscope. This paper will give further investigation of delay mismatch in this structure.

The organization of the paper is as following: Section 2 gives a brief introduction of the proposed test structure and design considerations about the effects of "off" transmission gates are investigated. Section 3 describes the effect of the layout on the delay mismatch using three different layout structures. Section 4 analyzes delay mismatch related to layout structures, transistor sizes, and number of cells with further details. Section 5 will summarize and conclude the overall achievement.

2 Proposed test structure

2.1 Introduction of test structure

We have proposed a configurable RO circuit by means of modified ROs [9], which aims to characterize the delay mismatch due to process variations in identical buffer elements. The test structure is shown in Fig. 1.

For a given single RO with N delay elements, the overall structure is composed of 2N+1 delay elements, providing 2N+1 individual ROs that are selected in circular manner controlled by two groups of transmission gates, SW and S transmission gates, acting as switches, as shown in the Fig. 1. The S switches, which connect between two neighbour inverters, are used to select the inverters that form the current RO. The SW switches are used to select the current RO by connecting the output of the last inverter to the input of the first one. For instance, the first RO is composed of first N delay cells, N being an odd positive integer value. When the first RO is activated, S1 to S(N-1) and SW1 are on, while other switches are off. The second RO is obtained by disconnecting the 1st delay cell from the current RO and appending the N+1th delay cell at the end of the RO. Therefore, when the second RO is selected, the switches S2 to SN and SW2 are on, while other switches are off. Similarly, the third RO is obtained by removing the 2nd delay cell from the current RO and appending the N+2th delay cell at the end and so on. The last RO has cell 2N+1 as the first delay cell and cell N-1 as the last cell. The configuration of a particular RO is controlled by the corresponding switches. Thus a total number of 2N+1 ROs are obtained by reconfiguring the modified RO architecture.

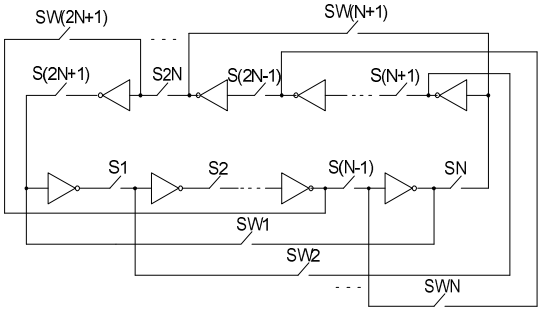


Fig.1 Proposed delay mismatch measurement architecture [9]

The modified RO architecture allows characterizing the mismatch in the constituent delay cells simply by measuring the corresponding periods of the 2N+1 ROs, and then single cell delays are derived. In fact, by performing some mathematical manipulations, the propagation delay of each delay cell is computed from the measured periods.

2.2 Design consideration

The computation method to derive single cell delays presented in [9] is based on the common formula for RO period estimation. That is, for an N-element RO, the period (P) can be expressed as:

$$P = 2\sum_{i=1}^{N} D_i \qquad (1)$$

with D_i is the i^{th} cell delay. According to the 2N+1-cell test structure, for each RO, only the first cell is different from its next RO, and only the last cell (N^{th} cell) is different from its previous RO. Hence, by calculating the different periods between adjacent ROs, we can get different delays between any delay cell and its next N+1 cell. Then by arranging all these different delays, single cell delays and delay mismatch can be derived. Note that these different delays are obtained based on the assumption

that only an inverter and the transmission gate connecting this inverter to its next inverter are considered as a delay cell, and delays of only selected inverters and conducting transmission gates are taken into account in the formula. In fact all the "off" transmission gates (OTG) connected to the selected inverters also influence the actual period of the RO. For OTG, the equivalent resistances are considered as infinite, while diffusion capacitance (junction capacitance) still exist and act as load capacitance at the delay cell output. If the effect of OTG is considered, the relation between two RO periods become more complicated

Fig. 2 shows all of the components influencing the period of the 1st RO in an 11-cell structure. Among them, all OTG locating outside RO will affect delay cells but is not considered in the computation method.

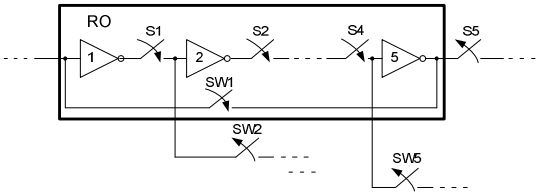
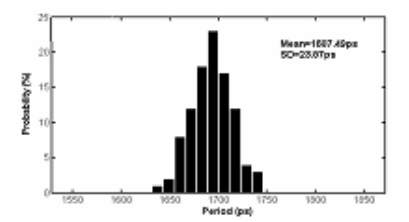
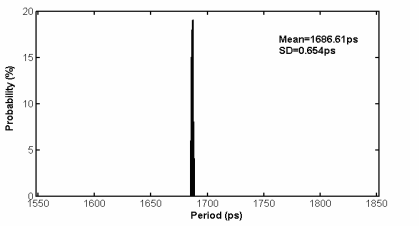


Fig.2 Components influencing the 1st RO period in 11-cells structure

In the ideal situation, the effect of OTG should be equal for each RO, therefore its effect would be cancelled when calculating different RO periods. However due to process variations, the effect of OTG may be different from one RO to the other. In order to analyze the effects of OTG, Monte Carlo simulations have been carried out with an 11-cell structure using minimum transistor sizes for both inverters and switches. For statistical simulations, we only setup variations in transistor length, since it is the main source of delay mismatch. Moreover, because it is a common practice to treat the parameter variability inside die as a normal distribution [10], these length variations are assumed to follow a normal (Gaussian) distribution and the same standard deviation (1.8 nm) of the transistor lengths is used for both delay cells and OTG. The distribution of delay mismatch caused by fluctuations in transistor length in the delay cells and OTG are depicted in Fig.3 (a) and Fig.3 (b), respectively. The results show that the maximum delay deviation for transistor length variation in delay cells is as large as 23.87ps, whereas it is only 0.65ps for transistor length variations in OTG. That means that under certain process variation, device parameter variation in delay cells is the dominant factor that cause delay mismatch in the circuit. Although OTG connecting to selected inverters may influence RO period, they cause little delay mismatch due to process variations. Hence the effect of OTG could be cancelled when calculating different periods in the computation procedure. Thus the computation method presented in section [9] is well applicable for single cell delay measurement. Therefore, the delay mismatch obtained using this test structure represents mainly delay variability caused by delay cells, which in fact what we are interested in.



(a)



(b)

Fig.3 Delay mismatch due to transistor length fluctuation (a) in delay cells and (b) in OTG

3 Layout structures

In [9], we reported that the test structure is completely symmetrical. However, after layout, the unbalanced interconnect wires may induce inevitable delay mismatch between delay cells. In this section, three layout structures will be presented. In application circuit, it is always expected that the structure have the smallest delay mismatch due to layout. Moreover, the parasitic capacitance of interconnect in the structure should be small, because this smaller capacitance will in turn cause less delay mismatch due to interconnects. All of the following layouts are designed for the 15-cell architecture with minimum transistor sizes.

3.1 Type-I layout structure

Considering effects of spatial variation in intra-die process variations, the cell-to-cell delay mismatch should be able to represent this spatial variation, so that all 15 inverters and 30 transmission gates are put

in the same line in type-I layout structure (see Fig. 4).

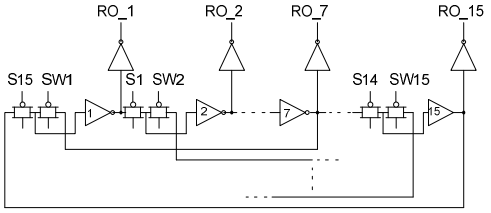


Fig.4 Components placement in Type-I layout structure

This layout structure forms a dense interconnect area in the bottom of device, which may produce large parasitic capacitance influencing cell delays. Moreover, the horizontal interconnect wires are very long in this structure because all the devices stay in one line, however the vertical wires can be made short.

3.2 Type-II layout structure

In order to shorten the long interconnect wires; type-II structure is designed. In this structure, inverters and transmission gates are placed in different two lines as shown in Fig 5.

Comparing to type-I structure, the horizontal interconnect wires may be shorter, but the number of the vertical wires increases much more, because metal wires between two lines include not only interconnects between inverters and SW switches, but also interconnects between inverters and S switches. The more crossing wires make parasitic capacitance more complicated.

3.3 Type-III layout structure

Considering common layout structure of the ROs in many applications, a different layout topology is shown in Fig.6. In this structure, inverters are placed in two different lines surrounded by transmission gates that are located inside the ring. Hence this structure would form two dense interconnect areas.

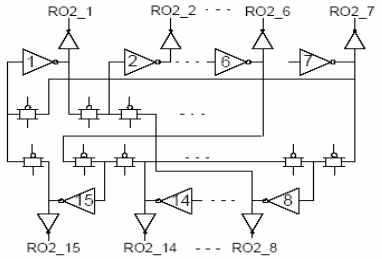


Fig. 6 Components placement in Type-III layout structure

4 Delay mismatch analysis

This subsection analyzes the delay mismatch in the three layout structures presented earlier using the results obtained from Monte Carlo simulations. Subsequently, the structure with the best delay mismatch will be selected for analyzing delay mismatch related to transistor sizes and number of cells in the ring. The goal of the analysis is to provide valuable consideration to reduce the effect of delay mismatch in application circuit design.

All simulations were performed for post-layout under TSMC 0.18um CMOS Technology and the same simulation procedure has been followed for each structure. Layout was extracted with parasitic capacitances in Virtuoso of CADENCE. In Monte Carlo process file, length deviation (standard deviation) is set up to 0, 1.8, and 3.6 nanometers, respectively. The nominal length values used for each test case are described in the corresponding sub-sections. Each simulation was carried out for 100 runs, and for each run, random length values were assigned to transistors by the simulator based on the Gaussian distribution defined by the chosen deviation and nominal length values. From the simulation results, all RO periods were obtained and then our computation method is used to obtain single cell delay and delay mismatch. With length deviation set to 0 nm, the delay mismatch observed is only due to unbalanced interconnect wires in the layout. For the other two cases, the delay mismatch is caused by both the layout and the process variations. The delay

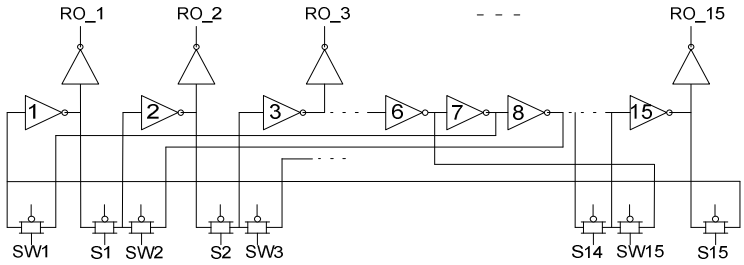


Fig.5. Components placement in Type-II layout structure

mismatch is characterized by using the standard deviation of cell delay (σ) and the relative deviation, also called coefficient variation (CV), which is defined as the ratio of standard deviation to the mean value (μ).

4.1 Delay mismatch due to the layout

For the three layout structures described in section 3, unbalanced interconnect wires leading to delay mismatch concentrates on dense interconnect areas, where parasitic capacitances are very complicated. Simulations were performed to compare delay mismatch in different layout structures. The nominal transistor length values used for the three layout structures are 0.18um.

Table 1 presents delay mismatch in detail for the three structures. We notice that delay mismatch in type-I structure is larger than that in the two others, although average cell delay in type-1 is very small. Comparing type-II to type-III structures, delay deviations are much close. However, from parasitic capacitance point of view, interconnects in type-II induce smaller capacitance which result in smaller average cell delay. Therefore, type-II is the optimum structure with the smallest delay mismatch and the lowest cell delay.

Table 1 Delay mismatch in different layout structures

Length Deviation	*Type-I structure*		
	μ (ps)	σ (ps)	CV (%)
0nm	117.11	2.33	1.99
1.8nm	116.98	2.35	2.00
3.6nm	116.67	3.22	2.76
	Type-II structure		
0nm	124.74	1.19	0.95
1.8nm	124.82	1.79	1.43
3.6nm	124.56	2.00	1.60
	Type-III structure		
0nm	133.18	1.49	1.12
1.8nm	133.19	1.88	1.40
3.6nm	133.32	2.57	1.93

4.2 Delay mismatch related to transistor size

This section analyzes the effects of delay mismatch for different transistor sizes. Since type-II is the structure with the smallest delay mismatch as described in the previous subsection, it was chosen to carry out Monte Carlo simulations for three 15-cell architecture with transistor lengths as 0.18um, 0.36um and 0.72um respectively. The obtained single cell delays and delay mismatches are tabulated in Table 2.

From Table 2 we see that enlarging the transistor length increases the single cell delay. Furthermore, larger circuit area may increase unbalanced interconnect which will lead to more delay mismatch, and even so at the presence of no process variations. However, the relative deviation decreases. That is, the increase in mismatch is less than the increase in cell delays. Therefore, the effects of delay mismatch would decrease with the transistor size increasing.

Table 2 Delay mismatch for different transistor sizes

Length Deviation	L=0.18um		
	μ (ps)	σ (ps)	CV (%)
0nm	115.71	1.83	1.58
1.8nm	115.66	2.44	2.11
3.6nm	115.25	1.53	1.32
	L=0.36um		
0nm	281.34	3.43	1.22
1.8nm	281.62	3.45	1.22
3.6nm	280.67	4.23	1.51
	L=0.72um		
0nm	766.7	6.59	0.86
1.8nm	767.1	6.4	0.83
3.6nm	765.7	7.38	0.96

4.3 Delay mismatch related to the number of cells

In order to investigate the dependence of delay mismatch on the number of cells in the RO, Monte Carlo simulations were also conducted on ring oscillators with different number of cells with a single transistor length of 0.36um. The numbers of cells were chosen to be 11, 15 and 31. The results obtained are illustrated in Table 3.

Table 3 Delay mismatch for different number of cells

Length Deviation	11-cells RO		
	μ (ps)	σ (ps)	CV (%)
0nm	281,34	3,43	1,22
1.8nm	281,62	3,45	1,22
3.6nm	280,67	4,23	1,51
	15-cells RO		
0nm	280,28	4,3	1,5
1.8nm	283,77	5	1,76
3.6nm	283,01	4,94	1,75
	31-cells RO		
0nm	305,84	3,98	1,3
1.8nm	305,98	4,06	1,33
3.6nm	304,86	6,8	2,23

Basically, with the increasing number of cells, the

delay would increase because of an increase in interconnects. However, delay mismatch does not increase, especially in the case of smaller process variation, as the effect of layout on latter is dominant when process variation is minor. Moreover, with increasing the number of cells, the length of wire increases at the same time, therefore cell delay increases. Since the unbalance in interconnects and the delay deviation (standard deviation) are both proportional to the wire length, there will be no change in the relative deviation of cell delay.

In summary, delay mismatch in RO highly relies on layout and process variations. When designing application RO circuit, there is a direct trade-off between circuit area and delay mismatch. Larger transistor sizes imply larger circuit area, but lead to small relative deviation of delay which may decrease the effect of delay mismatch on the circuit.

5 Conclusion

Statistic analysis reveals that our proposed test structure and computation method presented in [9] is feasible and enough accurate to measure single cell delay and delay mismatch. In this architecture, although OTG may influence the period of ROs, they induce little delay mismatch due to process variations. Hence in terms of parameter fluctuations, only the fluctuation in inverters and conducting transmission gates affect delay mismatch in this test structure. Delay mismatch in RO is quite dependent on layout structure, transistor sizes and the number of cells. A good layout structure relies on strict balance of interconnect between cells. With increasing transistor sizes, delay mismatch may also increase, but the relative deviation of delay will decrease, which means that the effect of process variation on delay mismatch will decrease. This gives a trade-off between circuit area and delay mismatch when designing application circuits. When jitter due to single cell delay mismatch is the main concern in the circuit, it is necessary to increase transistor sizes to decrease the effect on the delay mismatch. Changing cell number may be considered to get desired cell delays, especially when the process variation is small. Implementing large number of the same test structures on a test chip may be considered to investigate delay mismatch due to intra-die variations. Measuring large quantities of such test chips can reveal the effects of inter-die variations. Furthermore, the test structure can be imported into new and emerging semiconductor technologies.

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