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A Low Voltage Low Power 5.7 GHz Variable Gain LNA in 0.18 um CMOS Technology

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Abstract: This paper presents a 2.4 GHz 0.18 µm CMOS single-ended Variable Gain Low noise Amplifier (VGLNA). The circuit is suitable for low voltage, low power operation, uses a current-reuse topology to increase linear gain and save power consumption. The common-source gain stages are stacked for minimum power dissipation while maintaining high gain. The VGLNA exhibits noise figure less than 3 dB and gain of 12 dB and 8 dB gain tuning range , P_{1dB} of -2.8dBm. The VGLNA circuit dissipates 2.3 mW DC power from a supply voltage of 1.2 V. A gain/power figure of 5.2 dB/mW is achieved. Simulation results are presented

1 Introduction

The rapidly growing demand for broad band wireless communications, and the convenience introduced by portable wireless devices have drastically influenced the way people communicate. Due to the increasing demands on the wireless services, the operating frequency is moving toward the 5 GHz (U-NII) band. According to this it is desirable to implement RF front ends in a high level of integration with low fabrication cost.

Recently CMOS technology has attracted great attention in the implementation of RF circuits due to the advances in its high frequency characteristics of both active and passive devices. The unity gain frequency f_T of CMOS devices becomes comparable to that of the GaAs process . Thus the CMOS process with 0.18 um feature size is a good candidate for highly integrated system on chip (SOC) applications. Despite the technology's potential for application in multi gigahertz range, it typically involves higher power dissipation due to the inherently low transconductance of the MOSFET devices , in addition to the limitations imposed by the technology on the supply voltage. Thus a special attention has to be paid to develop low-power and low-voltage techniques for CMOS RF circuits.[1-4]

In almost all wireless receivers, the receiver is supposed to process the weakest and strongest input signals specified by the sensitivity and dynamic range specifications. This variable gain LNA eases the job of the receiver by meeting the sensitivity specification in the High gain mode and dynamic range specification in the Low gain mode. Since the gain is controlled in the first block, the remaining blocks are now required to meet a more relaxed specification and hence will be power efficient (consuming less dc power). The controllable gain can prevent the saturation of the receiver when the input signal is relatively large.

In Typical wireless receiver systems, LNA plays a crucial role and is one of the key components, it tends to dominate the the sensitivity of the whole receiver systems, thus it should be designed with a special care to the noise factor and gain.

2 Circuit Topology and Desgin

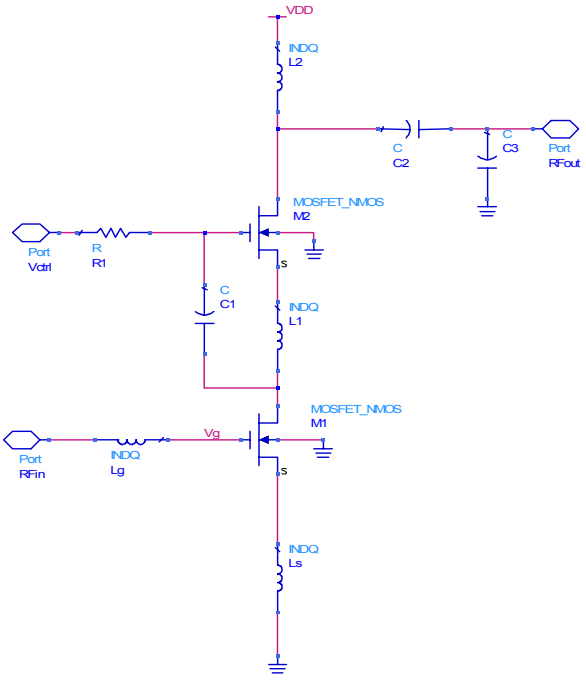

Fig. 1. Schematic of the VGLNA

The topology of the proposed VGLNA circuit is single ended current reused cascade stage. Transistor M1, and M2 are both in common source configuration, since the sources of M1 and M2 are connected to signal ground separately, they are both share the same DC current to reduce the consumption. The overall circuit diagram is shown in Fig. 1, the equivalent circuit of the input stage is shown in Fig. 2.

The gate width of the transistor of the input stage is determined in a way to reduce noise [2], the width of transistor M1 is found to be 150 um, multi finger transistor structure should be used in the layout design of the transistor, to minimize the noise source of the gate resistance.

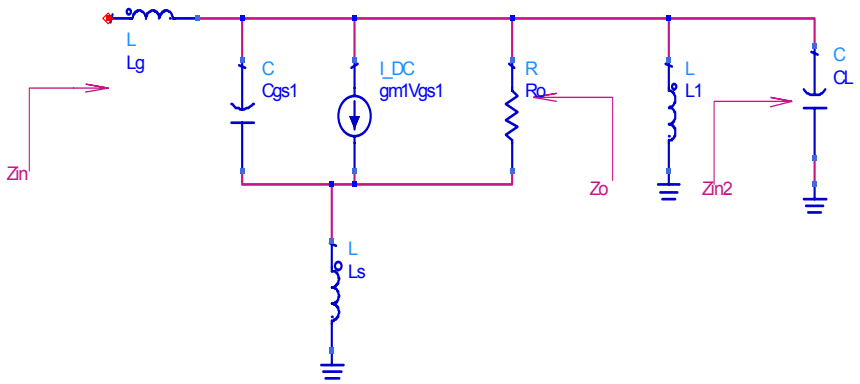

Fig. 2. Schematic of the equivalent circuit of the input stage

To achieve input matching to 50 Ω characteristic impedance, and inductance at the source of M1, L_s source degeneration, and an inductance L_g at the gate. The combination of the gate and source equivalent inductance cancels the reactance of the parasitic capacitance at the gate at the resonance frequency ω_o . The input impedance is calculated from:

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_{m1}}{C_{gs}} L_s \quad (1)$$

at resonance frequency $\omega_o = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}}$,

the imaginary part is canceled leading to :

$$Z_{in} = \frac{g_{m1}}{C_{gs}} L_s = 50\Omega \quad (2)$$

L_1 is used for the first stage inductive load , with no extra dc voltage drop, is chosen to resonate with the parallel equivalent capacitance at the frequency of interest. In addition L_1 and C_1 provides matching between the first and second stage (M1, M2)[5]. The output matching network is composed of L_2, C_3.

3. Gain Control

The gain is controlled through the voltage Vctrl applied to the gate of the second stage transistor,M2. As the gate voltage of M2 changes the drain voltage of transistor M1 changes moving the transistor's bias point between the high gain region and low gain region without significant degradation in the input and output return loss, and without significant degradation in the noise figure.

4. Simulation Results

The VGLNA is simulated using 0.18 μm TSMC CMOS device parameters from MOSIS. Results are performed at source and load impedance of 50 Ω. Fig. 3, and 4 shows the simulated gain and noise figure at different control voltages with frequency., a gain of 11.85 dB and noise figure of 1.98. dB are obtained from simulation Fig. 5, shown the gain variation with control voltage.

Fig 6, and 7 shows the simulated input and output return loss S_{11} and S_{22} at different frequencies, S_{11} of -20 dB and S_{22} of -30.1 is achieved.

Fig. 6, shows the simulated gain compression, P_{1dB} of -2.8 dBm is achieved. Table I summarizes the performance of the proposed VGLNA circuit.

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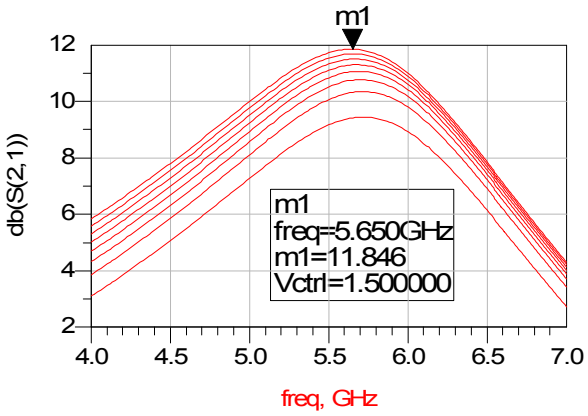


Fig. 3 Gain at different control voltages

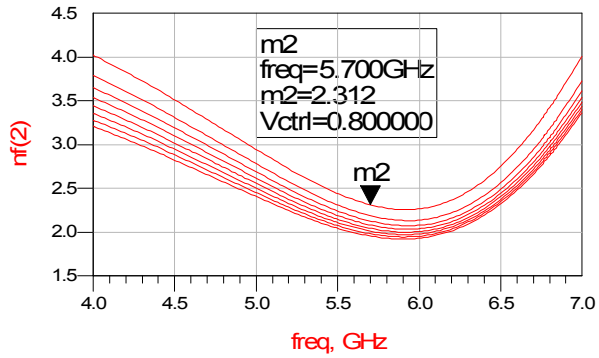


Fig. 4 Noise figure at different control voltages

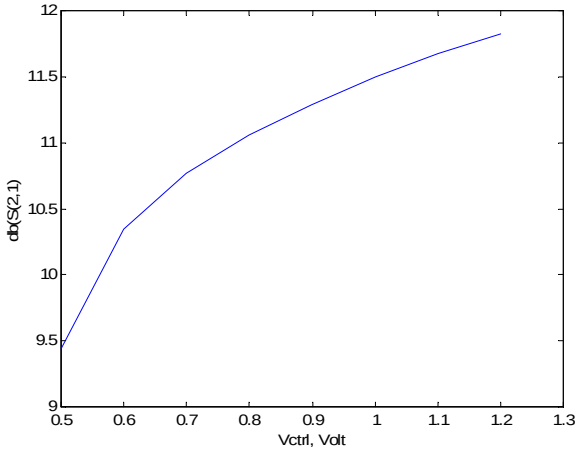


Fig. 5 Simulated gain at the frequency of interest with V_{ctrl}

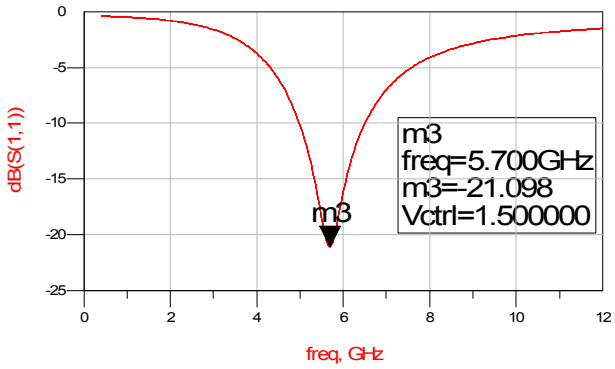
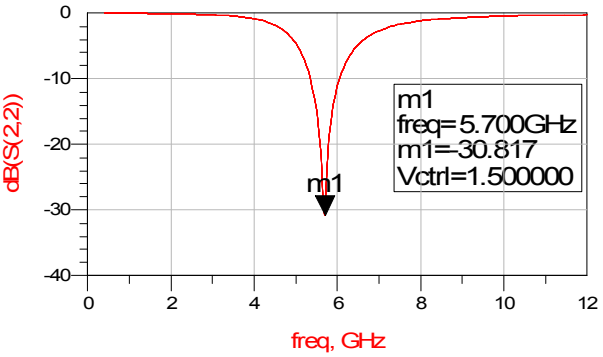


Fig. 6 Simulated Input return loss



F9g. 7, Simulated Output return loss

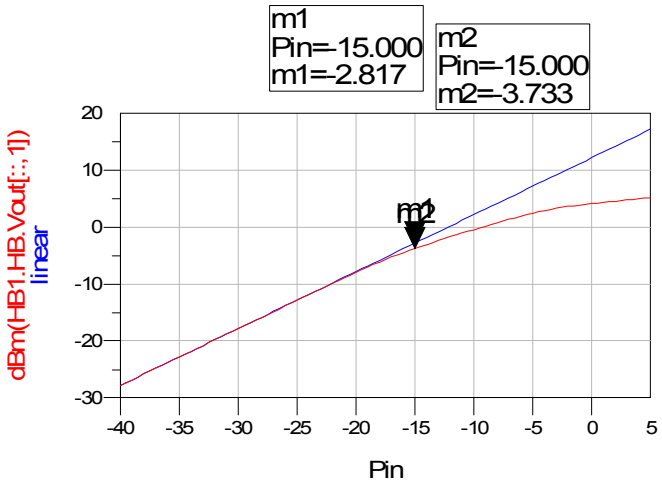


Fig. 8, Simulated 1dB gain compression point

Table 1. Performance of the proposed circuit

Paramater	Value
f_o	5.7 GHZ
V_{DD}	1.2 V
S_{21}	11.8 dB
S_{11}	-20.1dB
S_{22}	-30 dB
Power Dissipation	2.3 mW
P_{1dB}	-2.8 dBm
Noise Figure	1.89 dB

5 Conclusion

A 5.7 GHZ variable gain LNA s has been designed using 0.18um CMOS parameters, the LNA achieved an input return loss S11=-20.1dB. With a supply voltage of Vdd=1.2 V producing a gain of 11.8 dB, output return loss of S22=-30dB. The circuit consumes 2.3mW, and it is suitable for low voltage low power applications. Layout is sent for fabrication, measurement results will be performed.

References:

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