Chip Level Charge Recovery

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Abstract: - Charge recovery uses charge from falling datalines to charge the rising datalines. Previous works addresses to this phenomena using statistical switching models where the amount of energy savings depends on the number of lines shorted, the control circuitry, data length & pattern [1]. We are extending the concept to creation of an intermediate level virtual source/sink, which acts as a charge reservoir & facilitates for charge recovery. Implementation of the concept provides feasibility for chip level charge recovery, even suitable for a single switching line. We could observe up to 35% reduction in switching power.

Key Words: - low power, databus design, energy recovery, charge recycling, charge recovery.

1 Introduction

Charge recovery databus is used for low power applications. Concept utilizes the fact that the charge given away by the high-to-low transitioning net can be utilized to some extent by the low-to-high transitioning net [1], [5]. Wide and long databuses consume significant amount of energy. Introduction of such technique reduces the overall current demand resulting in significant reduction in I^2R component[2]. This in turn reduces chip heating. Any change in state of databus shorts all the transitioning lines and provides a path for charge flow from high-to-low going nets to low-to-high going nets. This phenomenon certainly requires some extra time for charge transfer mechanism and hence puts performance penalty.

We have extended the charge recovery concept to a broader perspective. There are many cases where statistical switching nature of databus may not be helpful for charge recovery. Extreme case is of an isolated net where we cannot go for charge recovery. Introduction of an intermediate level virtual source/sink facilitates such recovery. What we intend to do is the creation of an intermediate level charge reservoir which exchanges energy from all those switching nets for which we wish to introduce charge recovery. We have introduced a floating capacitor realized with floating metal mesh. This mesh takes charge from all high-to-low going nets and gives charge to low-to-high going nets. Initially the floating mesh is at zero potential. After several cycles of operation, the mesh gets charged to a stable intermediate potential. Subsequent cycles of operation enjoy constant charge recovery irrespective of data pattern.

2 Problem Statement

Active power dissipation is a major point of concern in deep submicron silicon. Density of design is increasing continuously. Integration of billions of transistors on a single chip has been made feasible. Such a large system consumes a lot of power, which causes heating of the system. People have been trying various methodologies in technology as well as in design to reduce this power consumption while maintaining the speed and functionality [3], [4]. Lowering of supply voltage, bus encoding for low active power, low-k dielectrics, and high mobility devices with strained silicon lattice all addresses to the issue. This high current demand in turn creates several problems such as creation of local voltage islands due to IR drop. Such situations make system difficult to be designed. Charge recovery is a method by which we reuse the energy carried by charge for successive transitions.

3 Charge Recovery

Implementation of a charge recovery databus requires transition detection pulse generation circuit, tristate driver and a connecting switch. Also a chip/block level capacitive mesh is formed. As the transition is detected; transitioning line is shorted to the capacitive mesh for a fixed duration. This duration is realized by the pulse generation circuitry. During the charge transfer phase tristate drivers are disabled so as to allow the transfer of charge before the data lines are driven to their respective states. During charge transfer phase datalines achieve intermediate potential without any driving effort by

tristate drivers. High-to-Low going net discharges till intermediate level of floating mesh. Similarly Low-to-high going net is charged till intermediate level by the floating mesh. Fig.1 represents the basic concept of described charge recovery system. Datalines exchange energy with virtual source/sink through charge recovery circuit.

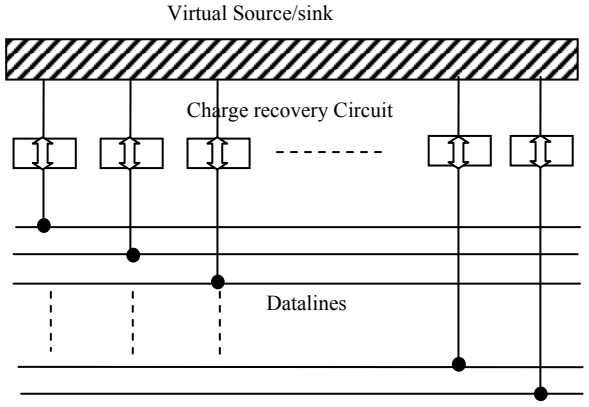

Fig1. Basic concept

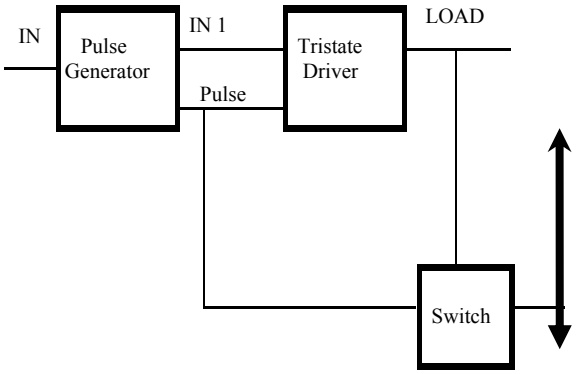

Fig2. Charge Recovery Circuit

Charge recovery circuit is shown in Fig.2, which consists of transition detection pulse generator, tristate driver and a connecting switch. This switch can be realized with a pmos or a passgate. This switch is connected to the floating mesh/shorting line whose capacitance is quite large in comparison to the total capacitance of transitioning datalines.

4 Model & Simulation

Let the intermediate equilibrium voltage of floating mesh capacitor be V′ .If the supply voltage is V, number of rising lines R and number of falling lines F, then we can write:

$$RCV' = FC\,(V-V') \qquad (1)$$

Hence, the intermediate voltage is given by:

$$V' = \frac{F}{R+F}V \qquad (2)$$

Since we are using large capacitive mesh as a reservoir, number of rising transitions equals' number of falling transitions over time. Therefore the equilibrium voltage becomes:

$$V' = V/2 \qquad (3)$$

Thus all the transitioning nets are charged or discharged till this intermediate value by the charged mesh. Here we are assuming that the rate of charge transfer offered to rising and falling nets are same. This depends on the nature of the switch used to short these transitioning lines to the floating mesh. We are also assuming that the pulse duration of charge recovery phase is sufficient enough to provide these nets equilibrium with the charged mesh of intermediate potential. In practical this is not feasible. If we are using a PMOS switch then it provides higher charge transfer rate from falling net and lower charge transfer to the rising net, hence equilibrium potential shifts to the higher side. In this case we observe:

$$V' > V/2 \qquad (4)$$

If we are using a pass gate then we can see V/2 intermediate equilibrium voltage provided the pulse duration for charge transfer is exactly equal for rising as well as falling nets or sufficient enough in both cases to achieve equilibrium.

Charging of floating capacitor/mesh is achieved through many cycles. Transitioning nets exchange charge from floating net and floating net starts charging (Fig-4). After several cycles of operation the rate of transfer of charge from rising & falling net becomes equal. At this point the floating capacitor achieves steady state voltage (Fig-5). Now the benefit of charge recovery is maximum and steady. It's independent of data pattern & bus width. During steady state when a stable virtual intermediate level source/sink is created all

transitioning nets change their state as shown in Fig. of the cases, free routing area can be utilized to

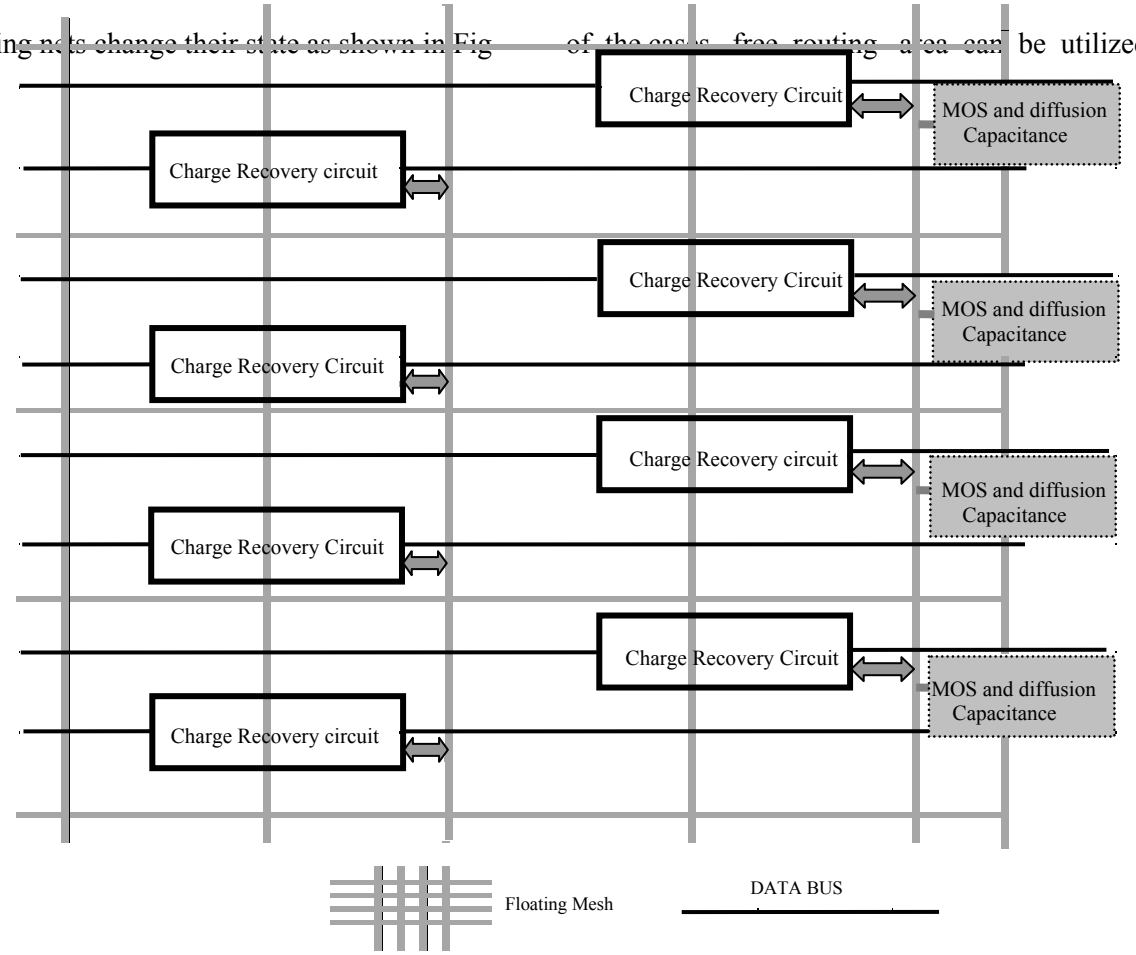

Fig3. Chip/Block level charge recovery scheme using capacitive mesh

6. All rising transitions are charged till intermediate level by the floating mesh during pulse as the drivers are disabled and they are charged by the charge transfer from floating mesh/capacitor. After the completion of this charge transfer phase, these nets are driven to supply voltage by the tristate driver. Similarly falling net discharges to floating mesh till intermediate equilibrium voltage. This is the charge which is being trapped or recovered. Further these nets are discharged completely by the tristate driver once the pulse period is over.

5 Performance & Penalty

Implementation of a charge recovery databus using floating mesh requires a dedicated floating metal network for creation of large capacitive seat which connects multiple blocks where we wish to use the concept. Along with metal capacitance we also use MOS and diffusion capacitances. Introduction of these capacitances add area to our system. In most increase the capacitance of connecting network. Charge redistribution phase is a timing penalty for the system. This should be noted that we are targeting only low power applications where we intend to operate at low frequencies. Hence we have sufficient timing budget for the introduction of the scheme. Charge recovery databus is supposed to be used when we are operating at low frequencies and the transition time of the nets is quite large so as to minimize the power with quasi static operation. Charge recovery adds another power saving over and above quasi-static driving. Chip/block level implementation using large floating mesh is shown in Fig-3. Databus or any isolated single dataline is connected to floating capacitive mesh through charge recovery circuit. So the scheme is useful for frequently used control signals also. Charging time of floating mesh is in the order of microseconds. Also it's going to depend on the number of transitioning nets & capacitance of floating capacitor realized. So its going to take some time before the advantage is realized. In comparison to real time of

operation it's quite negligible.

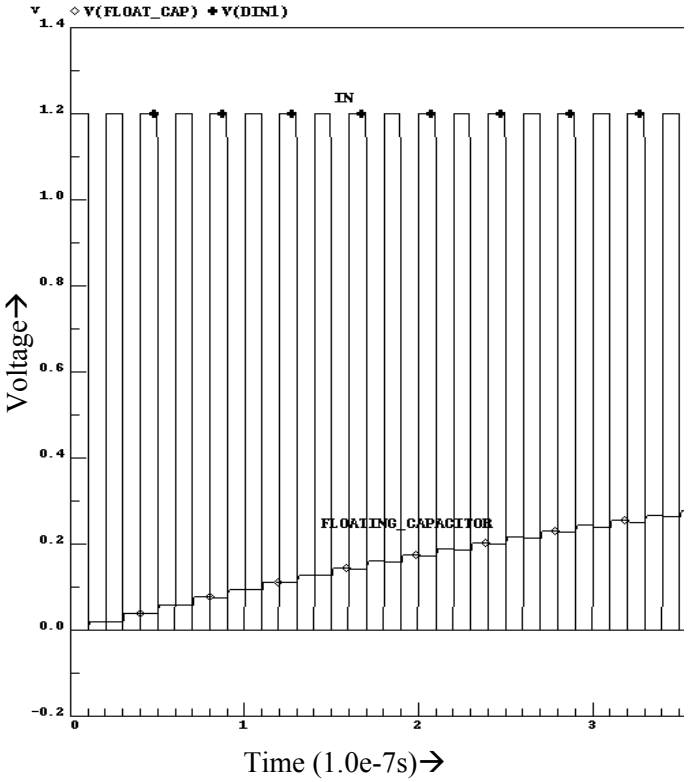

Fig.4 Initial Charging of floating cap

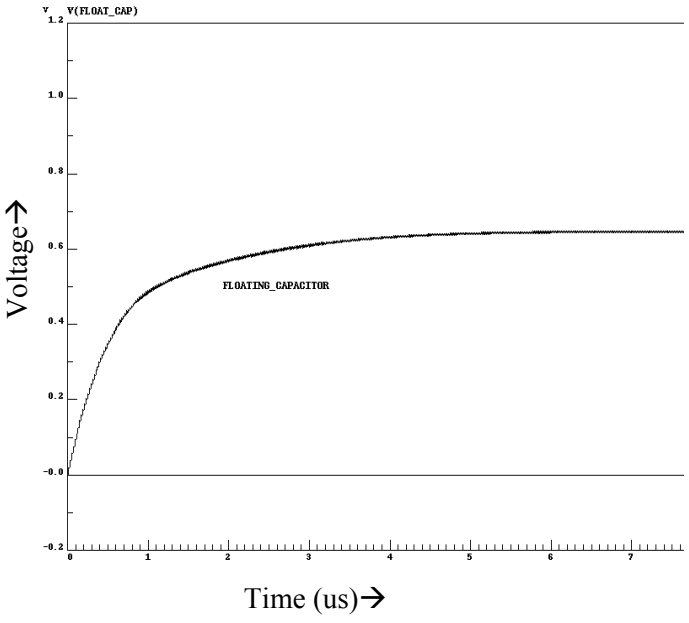

Fig.5 Floating mesh achieves steady Intermediate voltage

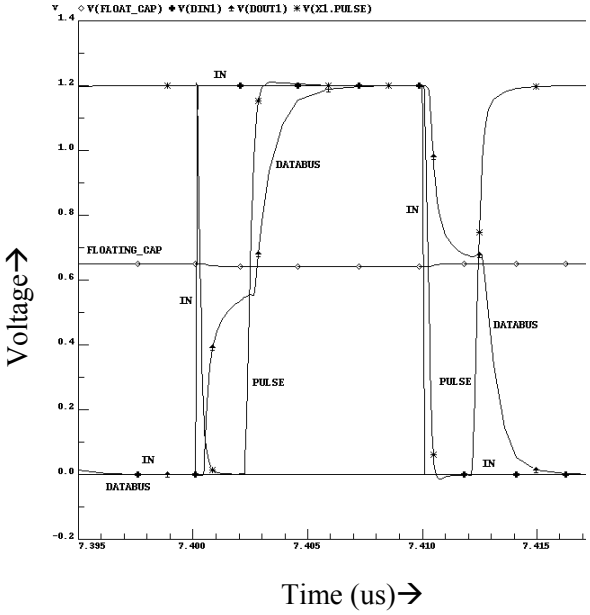

Fig.6 Charging and discharging of dataline using charge recovery

6 Results & Conclusion

We have done simulations taking four random switching datalines which are connected to a large capacitor using charge recovery circuit. Fig. 4,5 and 6 are taken from those simulations, which explains the operation of the charge recovery databus. We are working with 90nm CMOS technology with a supply voltage of 1.2 volts. Experiments were performed by varying the size of load lines as well as the pulse width which is used for charge transfer. We could observe that with an increase in load, our advantage also increases if the rest of circuitry remains same. This is obvious from the fact that the power consumed by the control/charge recovery circuit becomes prominent if we are dealing with smaller loads. With an increase in pulse duration, gain is observed if the initial duration is insufficient to provide maximum charging/discharging up to intermediate voltage. Otherwise pulse duration need not be increased. Pulse width also depends on system's demand for performance. If the timing budget doesn't allow pulse width for a complete charge transfer then we have to compromise with the advantage. Scheme is suitable for long, heavily loaded datalines. We could observe a reduction in

current consumption up to 35%. This reduction is possible for all data patterns. Datalines need not be nearby to facilitate charge recovery. Any isolated dataline can take part in charge recovery & hence lesser power consumption irrespective of data length & pattern.

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