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Noise Characterization of CMOS Image Sensors

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Abstract: - This paper presents noise characterization of a CMOS 0.6-µm image sensors system. The integrated readout circuit adaptability allows measuring the photocurrent magnitude of each pixel in charge integration mode or in transimpedance mode. In order to find the minimum detectable signal of this system and to identify the main dominant noise sources, an accurate noise analysis is performed under dark and illumination conditions. Noise measurement and simulation with Spectre present a good agreement with the values predicted by the proposed analytical equations.

Key-Words: - CMOS, integrated amplifier, measurement, noise, PPS, simulation.

1 Introduction

For low power and low cost applications, random addressing, etc, CMOS image sensors are widely used. However, despite several benefits, CMOS Passive Pixel Sensors (PPS) and Active Pixel Sensor (APS) have not yet reached the Charge Coupled Device (CCD) noise performance. Because of their high dark current value and a significant noise, CMOS devices are prone to strong disparities, which severely limit the performance [1-4].

After introducing the system under investigation in section 2, in section 3 we present the three operating modes, which are the reset, the charge integration and the transimpedance mode. Then, in section 4, a noise analysis is proposed during the entire operation cycle. Finally, theory is compared with measurement and simulation results in section 5.

2 On-Chip Image Sensor System

The investigated sensor contains a 4x4 matrix of PPS together with an integrated operational amplifier added on the serial output of the matrix [1, 2]. This on-chip image sensor system has been fabricated in CMOS AMS 0.6-µm technology. Concerning the pixel itself, there are two possible configurations. Fig. 1 presents only two PPS of the matrix associated to the amplifier. Pixel 2, at the bottom, is in normal configuration (one of the most popular architecture) and pixel 1, at the top left, has what is called a reverse configuration [2]. The photodiodes J1 are made up by using a P^+ diffusion layer on N well and the photodetectors J2 are realised with a N^+ diffusion or N well on a P substrate. Each photodiode has a reset transistor $M_{rst\theta}$ and a selection transistor $M_{sel\theta}$, with θ = 1, 2, …, 16. $M_{rst\theta}$ and $M_{sel\theta}$ are NMOS transistors, which act as switches. The M_{rst}' switch is a PMOS. The feedback capacitance C_{int}, connected between the input V- and the output V_{out}, is of type inter-poly capacitance.

Concerning the integrated amplifier, the main model parameters are the following:

- ✓ Gain bandwidth product GBW = $A_0 f_{cOA}$ close to 7.9 MHz, with A_0 = 87.7 dB;
- ✓ Offset voltage V_{off} of about 10 mV;
- ✓ Common Mode Input Range : [0.4 V ; 3.8 V];
- ✓ Equivalent input noise voltage e_n of 0.5 µV/Hz$^{1/2}$ at 10 Hz and 15 nV/Hz$^{1/2}$ at 100 kHz.

Note that these values are obtained from Spectre simulations.

At the output, the signal flows through an analogical I/O pin to allow monitoring with an oscilloscope and measurement with a spectrum analyzer.

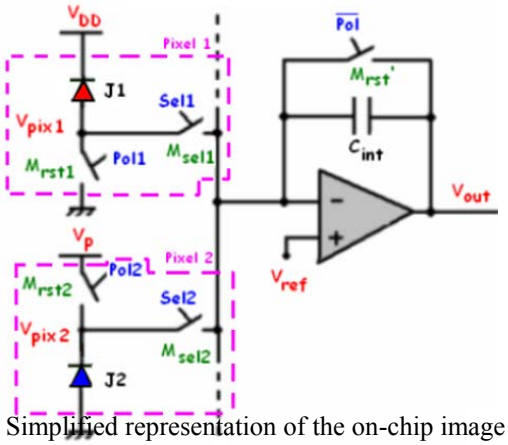

Fig. 1: Simplified representation of the on-chip image sensor.

Both Polθ (with θ = 1 to 16) and $\overline{Pol}$, are numerical signals resulting from the Keil MCB167 V2.0 evaluation board, associated to the Infineon C167CR microcontroller [5]. The numerical signals Selθ are delivered by an integrated multiplexer, associated to the same microcontroller, while V_p and V_{ref} are voltage biases generated by an external circuit. Consequently, all requested DC values are available, in order to provide reverse bias to all photodetectors.

3 Sensor System Operation

To provide an improved adaptability with respect to the operating conditions, the PPS matrix can operate in two modes (transimpedance or integration), with a reset phase after the readout of each pixel, just before the next pixel readout.

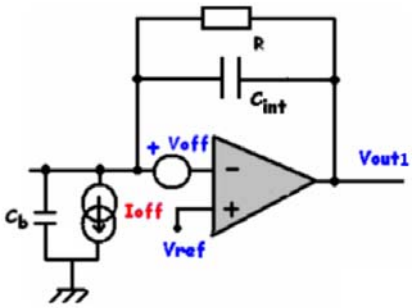

Fig. 2: On-chip amplifier during reset.

3.1 Reset Phase

During this phase, the photodetectors are biased with an appropriate reverse voltage in order to evacuate the charge on the capacitance C_{int}. All switches $M_{rst\theta}$ (θ = 1 to 16) as well as M_{rst}' are closed by Polθ and $\overline{Pol}$, respectively, whereas the selection transistors $M_{sel\theta}$ act as open switches. Hence, the amplifier is in the follower mode. This configuration is represented in Fig. 2, where R is the equivalent channel resistance of M_{rst}'; V_{off} is the offset voltage source of the integrated amplifier; I_{off} represents the offset current due to various leakage mechanisms (the amplifier itself, the bitline, the switch-off transistors); C_b denotes the parasitic bitline capacitance, that is evaluated as $C_b = NC_b' + C_{OA}$, with N being the number of rows times the number of columns; C_{OA} denotes the equivalent capacitance seen at the amplifier input V_-; C_b' corresponds to the pixel capacity on V_-, as well as the stray capacity of the connecting line.

In the steady-state, the output voltage V_{out1} is close to V_{ref}.

3.2 Transimpedance Mode

The transimpedance mode is currently employed for a fast detection with a direct current-to-voltage conversion and a high dynamic range [6-13]. However, a tradeoff must be made between sensitivity and bandwidth.

In this mode, the reset transistor M_{rstX} (belonging to the photodetector X) is open, while all other reset transistors M_{rst}' and M_{rstY} (with Y = 1 to 16 and Y ≠ X) remain closed. M_{selX} is also turned-on, whereas the other selection transistors M_{selY} are turned-off. Consequently, in the steady-state, the output voltage is proportional to $R(I_{ph}+I_{dc})$, where I_{ph} and I_{dc} are the photo- and dark currents, respectively.

3.3 Integration Mode

The charge integration mode is especially employed at low-illumination levels [9, 13-18]. However, it cannot allow a fast or a continuous data conversion. Here, the conversion time depends on the integration time t_{int}, which, at its turn, depends on the junction current.

In this mode, M_{rstX}, as well as M_{rst}' and M_{selY} are turned-off, whereas M_{rstY} and M_{selX} are in conduction. Then, the total junction current is integrated on the capacitance C_{int}. Hence, the temporal voltage evolution at the output is linear in $(I_{ph}+I_{dc})t_{int}/C_{int}$.

4 Noise Analysis

In order to evaluate the minimum detectable signal, it's necessary to find the output noise RMS value at the end of the readout phase. To do this, assuming that all noise sources are independent, a noise analysis is carried out during various operation modes separately.

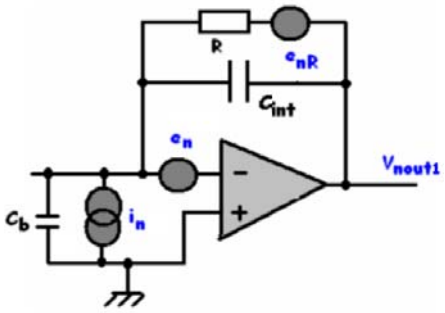

Fig. 3: Noise equivalent circuit during reset.

4.1 Noise During Reset

At the output, only the noise due to the readout circuit (amplifier and the feedback elements) is sensed. However, at each detection node of the matrix, a αkT/C noise is also present (α being 1 for a complete reset and 1/2 for an incomplete reset), where T is the absolute temperature and k denotes the Boltzmann constant [19, 20].

The noise equivalent circuit of the follower, in its steady-state, is proposed in Fig. 3. It contains three main noise sources [21]:

- ✓ e_{nR}, the channel noise of the feedback transistor M_{rst}'. As this device operates as a switch, in the ohmic region, the thermal noise is dominant. Its Power Spectral Density (PSD) is described by the following equation:

$$S_{e_{nR}}(f)=R^2 S_{i_{nR}}(f)=4kTR \quad (1)$$

- ✓ e_n, the equivalent input noise voltage of the amplifier. It is viewed as a superposition of thermal noise and 1/f noise, such as:

$$S_{e_n}(f)=a_{OA}+\frac{a_{fOA}}{f} \quad (2)$$

where a_{OA} and a_{fOA} are positive real coefficients deduced from experimental data (expressed in $V^2.Hz^{-1}$ and V^2, respectively).

- ✓ i_n, the equivalent input noise current, mainly arising from the contribution of the amplifier and the substrate. Its PSD is given by:

$$S_{i_n}(f)=a'_{OA}+\frac{a'_{fOA}}{f} \quad (3)$$

where a'_{OA} and a'_{fOA} are expressed in $A^2.Hz^{-1}$ and A^2.

Since the circuit of Fig. 3 is time-invariant, the equation of the output noise voltage v_{nout1} is deduced from a nodal analysis. Thus, as $A_0 >> 1$, its PSD is given by [2]:

$$S_{v_{nout1}} \approx \frac{R^2\left(S_{i_{nR}}+S_{i_n}\right)+S_{e_n}\left(1+\left(\frac{f}{f_{c1}}\right)^2\right)}{1+\left(\frac{f}{f_{c2}}\right)^2} \quad (4)$$

with $f_{c1}=\frac{1}{2\pi R\left(C_b+C_{int}\right)}$ and $f_{c2}=\frac{1}{2\pi RC_{int}}$.

4.2 Noise in Transimpedance Mode

At low frequency, the noise equivalent circuit of the acquisition chain is presented in Fig. 4. The newly introduced elements are:

- ✓ i_{nD}, the noise equivalent current source of the photodetector. As it is generally admitted [19, 22, 23], only the shot noise is dominant. Its PSD is:

$$S_{inD}(f)=2q(I_{ph}+I_{dc})=2q(s_\lambda P_{opt}+I_{dc}) \quad (5)$$

with q, the elementary charge ; s_λ, the quantum efficiency and P_{opt}, the optical power.

- ✓ e_{nRs}, the thermal noise voltage of the particular selection transistor, R_s being its equivalent channel resistance.

The total output noise voltage PSD under steady-state condition has been computed. We find [2]:

$$S_{v_{nout2}} \approx \frac{R^2\left(S_{i_{nD}}+\left(\frac{C_j}{C_b}\right)^2 S_{i_n}\right)+\left(\frac{f}{f_{c3}}\right)^2 S_{e_{nRs}}+\left(1+\left(\frac{f}{f_{c4}}\right)^2\right)S_{e_n}}{1+\left(\frac{f}{f_{c5}}\right)^2}+\frac{S_{e_{nR}}}{1+\left(\frac{f}{f_{c6}}\right)^2} \quad (6)$$

where C_j is the photodetector capacitance, $f_{c3}=\frac{1}{2\pi RC_j}$, $f_{c4}=\frac{1}{2\pi\left(R_sC_j+R\left(C_b+C_j+C_{int}\right)\right)}$, $f_{c5}=\frac{1}{2\pi\left(RC_{int}+R_sC_j\right)}$ and $f_{c6}=\frac{1}{2\pi RC_{int}}$.

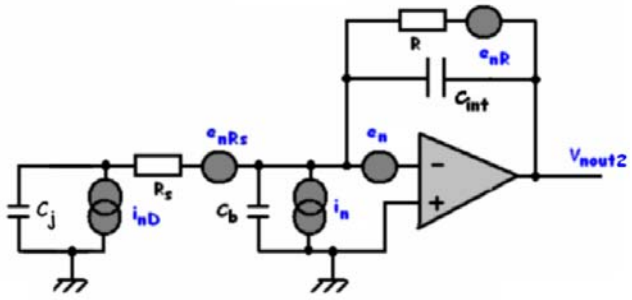

Fig. 4: Noise equivalent circuit in transimpedance mode.

4.3 Noise During Integration Phase

When operating in integration mode, the equivalent circuit of Fig. 4 remains still valid, provided that R and e_{nR} are both suppressed. Note that during this phase, the steady-state is never reached. However, as all components are supposed linear, a frequency-domain analysis can still be performed. S_{vnout3} is then found to be [2]:

$$S_{v_{nout3}}(f) \approx \frac{S_{i_{nD}}}{\left(2\pi C_{int}f\right)^2}+\left(\frac{C_j}{C_{int}}\right)^2 S_{e_{nRs}} + \left(\frac{C_b+C_j+C_{int}}{C_{int}}\right)^2 S_{e_n}+\left(\frac{C_j}{C_b}\right)^2\frac{S_{i_n}}{\left(2\pi C_{int}f\right)^2} \quad (7)$$

All these noise equations have been implemented in a MATLAB program in order to check the predicted numerical values against measurement and simulation.

5 Experimental Results

Table 1 presents the main parameters of the photodetector under investigation. Starting from the foundry datasheet, the junction capacitance parameters have been computed. As it was previously proved [23, 24], the junction capacitance value, deduced from the

Table 1: Various photodetectors data, at 300 K.

Type	Dimensions (µm²)	C_j simulated (fF)		I_{dc} (fA) at 2.5 V		$I_{dc} + I_{ph}$ measured* (fA) at 2.5 V
		at 0 V	at 5 V	Measured	Simulated	
Ndiff-Psub (J1)	*5.80 x 5.80*	*22.76*	*11.59*	*6.64*	*3.69*	*81,76*
Nwell-Psub (J1)	*6.55 x 6.60*	*17.04*	*7.87*	*13.45*	*5.69*	*22,04*
Pdiff-Nwell (J2)	*11.75 x 11.75*	*98.35*	*45.03*	*6.52*	*7.46*	*22,69*

* exposed to sunlight (unknown light intensity).

foundry datasheet, compares well with experimental data.

Concerning the dark current estimation, the adopted technique consists to average 100 successive measurement points, which yields the measured values of I_{dc} and $I_{dc} + I_{ph}$ presented in Table 1. A significant discrepancy appears between the measured and computed values (with MATLAB). A possible explaination must take into account to the following point:

- ✓ I_{off} has been neglected;
- ✓ The foundry maybe underestimated the junction leakage current parameters [24, 25].

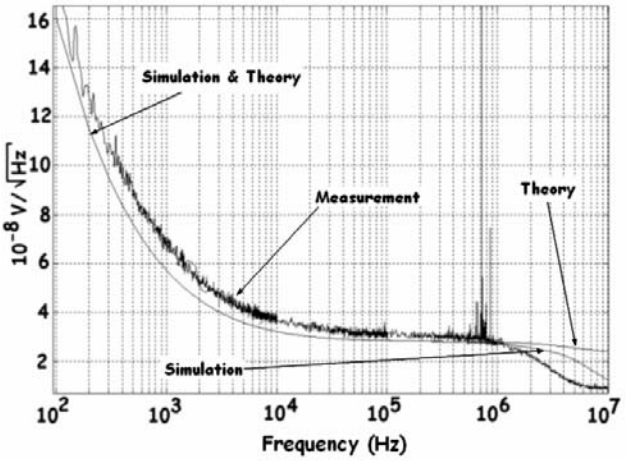

Fig. 5: RMS output noise voltage versus frequency, during reset.

A noise analysis in frequency-domain of any of the sixteen pixels has been carried out, by assuming that the readout circuit operates in the follower/transimpedance mode. During the first phase (follower mode), it is possible to determine the noise contribution of the integrated readout circuit alone (amplifier and its associated feedback elements). Analysis during transimpedance phase yields the noise of the global acquisition chain.

Simulations have been also performed under Cadence design tools together with the AMS CMOS 0.6-µm design kit and Spectre [26]. For CMOS transistors used as switches or inside the operational amplifier, the BSIM 3v3 model has been employed. Photodetectors have been modelled by paralleling a diode with a DC current generator to account for the carriers generated by light. As the steady-state is admitted, the small-signal parameters can be deduced from DC simulation. Thus, the following parameters have been added to the numerical model : V_{ref} = 2.5 V; R = 35.11 kΩ; C_{int} = 1 pF; C_b' = 2 fF; C_{OA} = 587.3 fF; a_{fOA} = 2.5 10^{12} V²; a_{OA} = 205.02 10^{-18} V².Hz^{-1}; $a'_{OA} = a'_{fOA} = 0$.

Fig 5 presents the output noise plots, obtained during reset. Experimental data are collected by sweeping the Vector Signal Analyser HP 89410 between 0.1 Hz and 10 MHz, with an integration window of 3 Hz. Each data point on Fig. 5 is an ensemble mean value of 256 samples. The previously developed model (eq.(4)) shows a good agreement with both simulation and measurement Nevertheless, the level of measured noise is slightly higher than the predicted value with a relative error less than 9 % at 100 Hz and less than 14 % at 100 kHz. This difference can be due to the noise source i_n which has been neglected in our calculation. Thus, for f_{min} = 2.5 Hz and f_{max} = 100 kHz, we have found $\overline{v_{nout1}^2}$ = 7.87 10^{-11} V². Finally, Fig. 5 proves that the 1/f noise of the amplifier is dominant at low frequency but at frequencies higher than 10 kHz, the thermal noise of M_{rst}' becomes dominant and it imposes a noise floor of about 30 nV/$\sqrt{Hz}$. Moreover, it has been noted that if measurement is made without shielding, interfering signals of strong amplitude appear close to 1 MHz.

A second measurement campaign has been carried out at the LAAS/CNRS laboratory in Toulouse. Fig. 6 illustrates the employed setup. Here, the output of the integrated amplifier goes on a Low Noise Amplifier (LNA), which is connected to the spectrum analyzer Avantest R9211B (controlled by a computer). The whole equipment is enclosed in a Faraday box. Except the spectrum analyzer and the computer, which are supplied by 220 V / 50 Hz, the remaining circuits are biased by internal batteries. Measurements have been performed between 2.5 Hz and 100 kHz, at an ambient temperature of 25.5°C. In order to estimate the noise contribution of the photodetectors, a laser with an optical fiber illuminates the active surface. The laser is temperature-controlled to deliver a wavelength of 830 nm. The

optical power is adjusted according to the current through the laser device.

Fig. 7 shows the output noise of the LNA with both inputs shorted-circuited. At low frequency, we note a noise in $f^{-1.5}$ and, at higher frequency, a noise floor appears close to 0.95 nV/$\sqrt{Hz}$, with a corner frequency around 200 Hz. Consequently, the noise level of the LNA is well below the noise level of the investigated system on-chip.

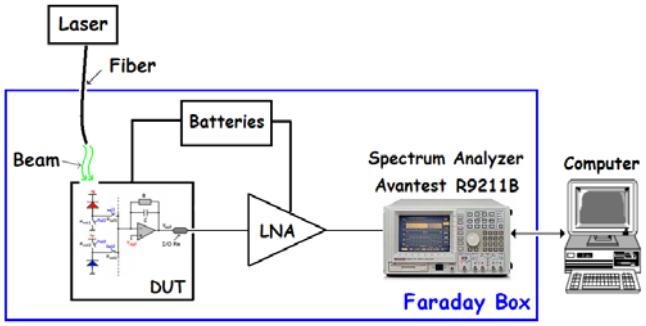

Fig. 6: Setup for noise measurement.

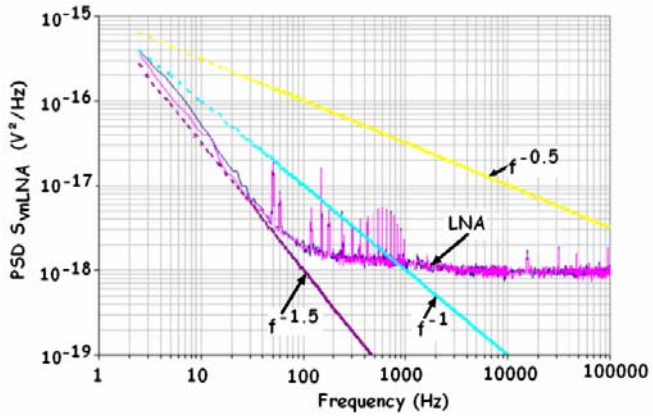

Fig. 7: Noise voltage PSD of the LNA versus frequency.

The plot of Fig. 8 refers to the photodiode J2 (Ndiff-Psub) and the amplifier in transimpedance mode, when applying various optical powers. In addition, a plot of the noise power obtained by simulation under Cadence and MATLAB has been added. Under dark condition, the shapes of the theoretical and experimental curves are quite identical with a relative error less than 2.5 % at 100 Hz and at 100 kHz. Besides, if the optical power of the laser is increased, the shape of the noise PSD remains the same, the plot being shifted upward. Consequently, as it is assumed through equations (5) and (6), the total output noise can be rewritten as: $S_{vnout2}=S_{vnout2}\big|_{dark}+|H|^2 s_\lambda P_{opt}$, where H is the transfer function between the optical input and the voltage output.

Fig. 9 presents the noise contribution of the photodetector J1 (Pdiff-Nwell) associated to the integrated amplifier. The aspect of the plot remains the same as previously, but, as this photodetector is less sensitive to the incident 830 nm light, the noise level variation with the optical power is less significant than in the case of Fig. 8.

Finally, with C_j = 32 fF and the previously defined parameters under dark condition, the computed mean square value of the noise voltage at the output $\overline{v_{nout3}^2}$ is 1.04 10^{-10} V² and the same result is obtained by simulation.

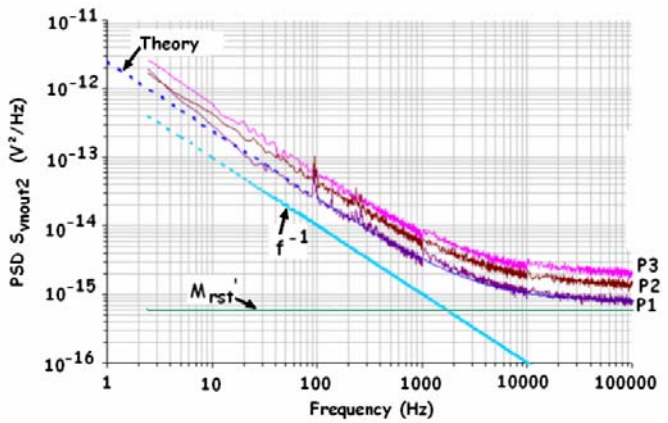

Fig. 8: Output noise of the photodetector J2 associated to the on-chip transimpedance amplifier, at three different illumination powers P1, P2 and P3.

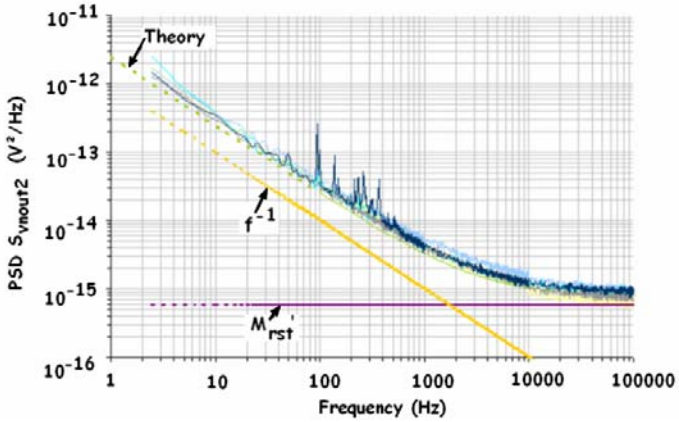

Fig. 9: Output noise of the photodiode J1 associated to the transimpedance amplifier.

6 Conclusion

A noise characterization of a CMOS PPS fabricated in CMOS AMS 0.6-µm technology has been presented. In order to find the minimum detectable signal of this system in dark and under illumination, an accurate noise analysis is performed, pertinent to all configurations. Noise measurement and simulation with Spectre compare well with the proposed analytical model. At low frequency, the 1/f noise of the integrated amplifier is dominant and, at higher frequency, the thermal noise of the transistor M_{rst}' imposes the noise floor.

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