Simulation of a Novel Bipolar-FET Negative Differential Resistance Circuits

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Abstract: In this paper, a new circuit that consist of n-channel FET and n-p-n transistor that act as a negative differential resistance circuits is presented. This circuit exhibit Type-S differential negative resistances. The circuit explanation and simulation is presented.

Keywords: Simulation of circuit, differential Negative resistance, Bipolar-FET circuits.

1 Introduction

Negative resistance devices are useful in that they can reduse cust and increase speed in a number of circuit applications.Solid State devices possessing differential negative resistance are very useful for a wide range of applications involving oscillation, amplification and logic operations.In recent year, the negative differential resistance devices have been widely used in various applications such as multistate memory [1], A/D converters [2], multivalued logic circuits [3], current and voltage references [4]. The negative differential resistance characteristics of devices make them operate at very high frequency [5], and the multipeak current-voltage characteristics of the integrated negative differential resistance circuits can greatly reduce circuit complexity in digital circuit applications [6].Tunnel diodes can be used as microwave oscillator, tuned amplifier, mixer, logic gates, flip flops, counters, multivibrator etc. Similarly, UJT can also be used as relaxation oscillator. Wide applications of SCR in control systems is well known. However, the value of their negative resistance can be adjusted only slightly. Moreover, since they are not made of standard FET or Bipolar transistors or both, their fabrication and mass production as integrated circuits is not feasible. Another approach for inventing new solid state negative resistance devices is to combine FET and Bipolar transistor with resistors.

The first circuit which exhibited negative resistance characteristics
and did not use internal bias was found in 1965 by Nagata [7].
After that few more circuits were added. Basic procedure to generate these circuits was try and hit. No systematic method exists even today.

2 Algorithms for generating such devices

In 1983, Chua. Yu and Yu [8] gave a somewhat reliable procedure to generate Type-N devices. Many circuits using this procedure are generated.
This procedure only helps in discriminating possible candidates which may exhibit negative resistance characteristics. This also can not tell absolutely whether the circuit will exhibit the negative resistance or not. The procedure is based on observations. Final 'yes' can be said only after simulation using SPICE or fabricating and checking the circuit.
Kumar and Nayak [10] proposed the algorithm in 1984 for generating type-S devices. However, this algorithm is also not ultimate and one can not be hundred percent sure whether the circuit is desirable or not. But this method is very efficient and gives quick estimate about resistance values. Also it is not time consuming and tells us whether the circuit will exhibit negative resistance or not.

3 Novel Type-S circuit

Nagata [7] has given a differential negative resistance circuit consists of two transistors with out internal bias. It has typical S-type current-voltage characteristic. The configuration of the circuit is shown in Fig.1.
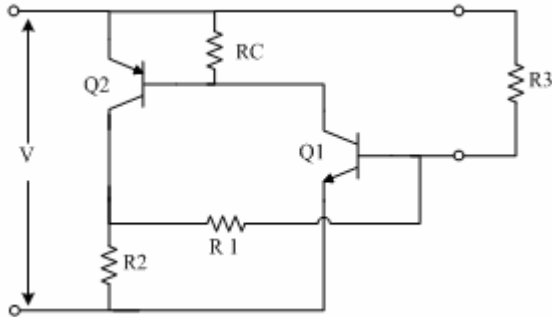

Fig.1 Negative differential resistance circuit consist of two BJT

The circuit is simple and the characteristics of the circuit are independent of transistor parameters if the transistors have typically large betas.

A new circuit (Fig.2) which uses two resistors, one n-channel FET and one n-p-n Bipolar transistor is presented. This circuit gives wide flexibility in curves and the design is simple since calculations involved are not much complex.

The operation of the circuit is like this. The circuit has $V_{GS}=0$, so the current will pass through R_1, FET and R_2 initially. I_B flowing is very small so voltage V_{BE} will be developed at Q2. When this voltage is equal to cut in voltage of base emitter junction 0.6 Volts, Q2 goes in saturation and V drops giving very high I.
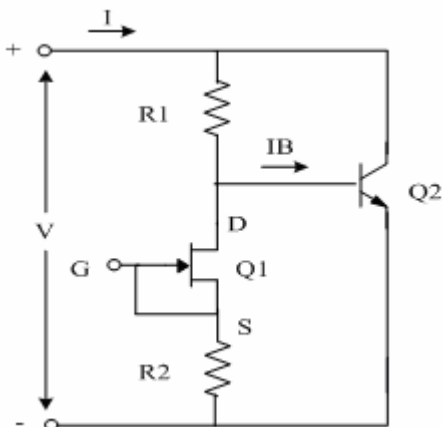

Fig. 2 The proposed new circuit

Theoretical explanation of the new circuit as shown in Fig.2 is as follows, the current and voltage in the new circuit are,

$$V_{BE} = \frac{R_2 \times V}{R_1 + R_2} \tag{1}$$

And

$$\frac{V - V_{BE}}{R_1} = I \tag{2}$$

$$KV = I$$

Where

$$K = \frac{1}{R_1 + R_2}$$

It is the slope of curve in region-1. When $V_{BE} = 0.6$, transition occurs from Region-1 to Region-3.

The voltage at which this takes place is from equation (1).

$$V = \frac{R1 + R_2}{R_2} \times 0.6 \tag{3}$$

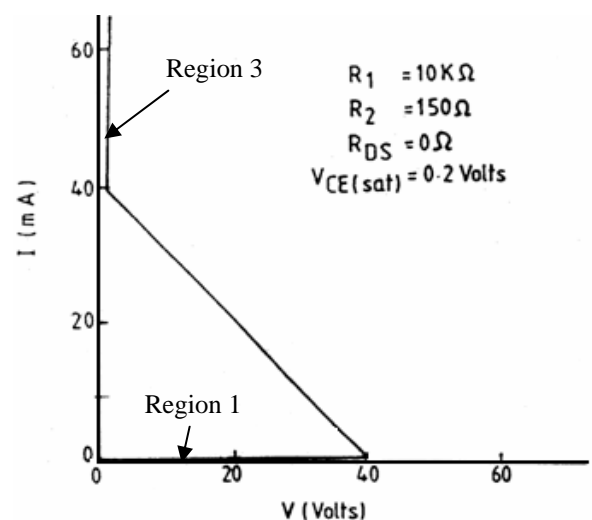Up to when the transition took place I_B was very small not enough to put Q2 in saturation.

Fig. 3 Circuit response (PSPICE Simulation)

The value of I is near to zero in region-1. When transition takes place in Region-3 of Type-S curve, current of the order of 40 mA flows in the circuit with $V=V_{CE} = 0.2$ Volts which is saturation collector emitter voltage. The PSPICE simulation results are shown in Fig.3.

I flowing at this time depend on r_{GS} which is only several ohms (typically 5 ohms). The resistance between D and S is several hundred kilo/ohms to several kilo/ohms. Hence, while finding V_{BE}, R2 should be replaced by

$$R = R_2 + r_{DS}$$

We can design considering FET only without R_2 and necessary r_{DS} as shown in Fig.4.

While fabrication this is useful. R_2 gives flexibility to locate transition points e.g. peak and valley points. Other FET bipolar circuits with more than two active devices are given in [11].
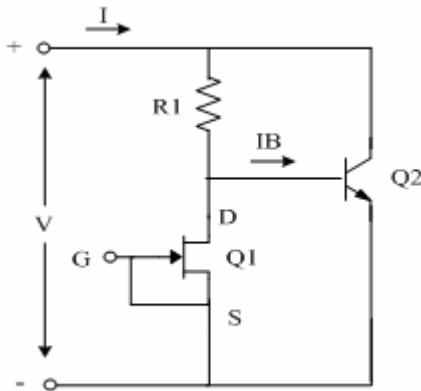

Fig. 4 The proposed new circuit

4 Conclusion

A new circuit consisting of one n-channel FET and one n-p-n transistor with two resistor that act as a negative differential resistance circuits is presented, explained and simulated. This circuit exhibit Type-S differential negative resistances.

In the Bipolar-FET negative resistance Type-S circuit the source resistance (i.e., R_2) gives flexibility to locate transition points e.g. peak and valley points.

Design are simple in these cases. The field is new and not much work has been done especially in FET circuits. The scope for future research is very wide.

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