4th WSEAS International Conference on ELECTRONICS, CONTROL and SIGNAL PROCESSING, Miami, Florida, USA, 17-19 November, 2005 (pp.12-17)

CMOS LNA and Mixer Components for 2GHz applications in 0.18-µm CMOS

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Abstract: - This paper describes a low noise variable gain amplifier (LNA) and a mixer for a WCDMA front-end receiver based on a direct architecture in 0.18-µm CMOS. The LNA provides a 50Ω input impedance and utilizes a tuned load to provide high selectivity. The LNA achieves a maximum small signal gain of 16.8 dB and a minimum gain of 4.6 dB with good input return loss. In the high gain and the low gain modes, the NFs are 0.83 dB and 2.8 dB, respectively. The LNA's IIP3 in the high gain mode is 2.1 dBm. The mixer achieves a conversion gain of 16 dB and a double side band (DSB) NF of 13.8 dB. The mixer's IIP3 is 12.12 dBm. The achieved low noise figure, gain and overall IIP3 fulfill the specifications for a UMTS LNA and mixer design. The LNA and the mixer, respectively, consume 4 mA and 5 mA of current from a 1.8-V power supply.

Key-Words: - CMOS analog integrated circuits, direct conversion, WCDMA, Receiver, Front-End, UMTS

1 Introduction

CMOS RF integrated circuits (RFIC) for wireless communication in the 2 GHz frequency range have gained much interest owing to their potential low cost and the prospect of system level integration. The most challenging building blocks in the front-end receiver are the low noise amplifier (LNA) and the mixer. The basic function of the LNA is to provide signal amplification while adding as little noise and distortion as possible to improve the overall noise figure and linearity of the front-end. In addition, the variable gain LNA (VGLNA) maximizes the overall dynamic range requirements for the receiver [1]. One the other hand, the mixer provides frequency translation from RF to the intermediate frequency (IF) called "down-converter", or from IF to RF called "up-converter".

Fine line CMOS VGLNAs and mixers with gate length of 0.18-µm or below open up the possibility of low power consumption compared to the bipolar and BiCMOS technologies. They must also equal and surpass the low noise figure of these technologies. This work is for design and implementation of an active CMOS two mode VGLNA and an active double-balanced mixer which achieves equal or better performance than the existing bipolar and BiCMOS technologies [2]-[3]. A simplified block diagram of the front-end of a WCDMA receiver is shown in Fig.1. In this architecture, the RF amplification and down-conversion stages are most and critical to reduce the system noise and most challenging to implement in CMOS.

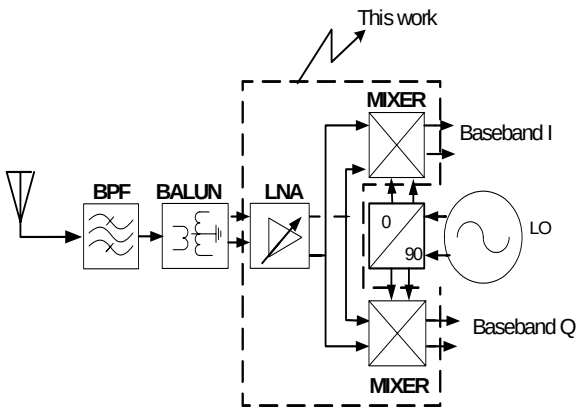

Fig.1 WCDMA receiver front-end application of LNA and mixer

This paper describes design and implementation of a CMOS variable gain low noise amplifier (LNA) and a mixer in a 0.18-µm CMOS process which is quite competitive with today's bipolar implementation.

The prototype design represents a first step toward a fully integrated monolithic WCDMA/UMTS. The rest of the paper is organized as follows. Design details is described in section 2. section 3 presents simulations of samples. Finally, section 4 derives the conclusion.

2 Circuit Implementation

2.1 LNA

The proposed variable gain feature of a cascode LNA is shown in Fig. 2. The variable gain LNA reduces the dynamic range requirement for the succeeding stages and also reduces the required gain of the base band filter (BBF). Two gain settings, such as maximum gain of 18 dB and minimum gain

$$F_{\min} \approx 1 + \sqrt{\frac{4}{5}} \frac{w}{w_T} \sqrt{\gamma\delta(1-|c|^2)} \qquad (1)$$

where $\omega_T = g_m/C_{gs}$ the unity gain frequency with g_m is the transistor transconductance and C_{gs} is the gate source capacitor. $\gamma = 3/2$ is the channel thermal noise, c is the complex correlation term equals to j0.395, $\delta = 4/3$ is the co-efficient of gate noise. It can be observed from (1) that F_{min} is effective for $\omega < \omega_T$ and the NF increases with increasing the frequency. Fortunately, thanks to the down scale rule of CMOS, the ω_T raises up and allow us to operate at higher frequency while maintaining minimum noise figure. Finally, having the F_{min} at the frequency of interest, the optimal transistor size can be calculated in the following:

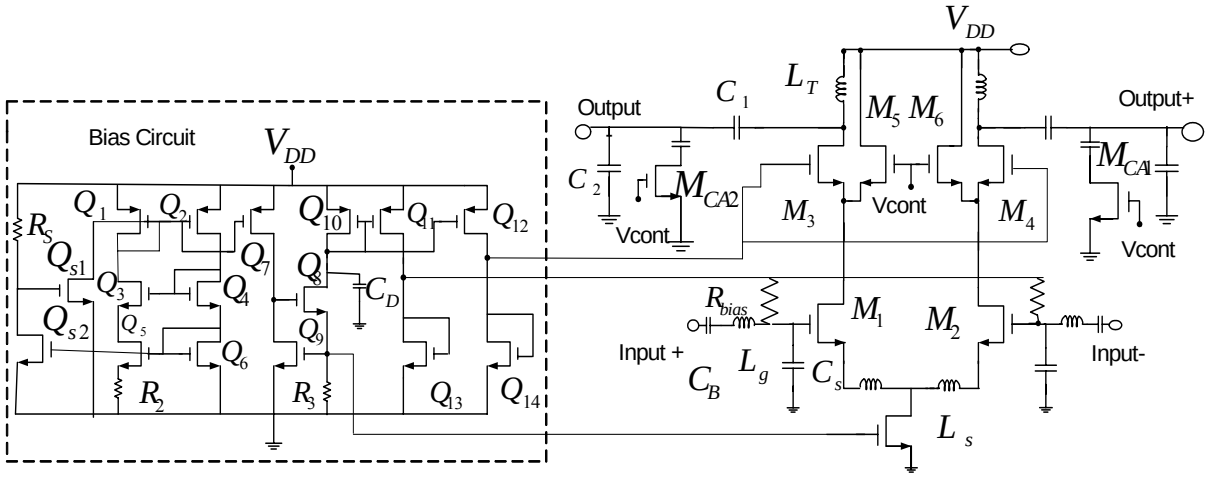

Fig. 2 . Schematic of the LNA

of 6 dB, are used to achieve the best overall NF and linearity. As shown in Fig. 2, the inductively degenerated CS input consists of transconductors M_1-M_2, and gate and source inductors, L_s and L_g, respectively. By employing this inductive source degeneration, a controllable real term in the input impedance can be generated which is equal to $L_s.g_m/C_{gs}$. At the operating frequency of interest, by choosing L_s properly, this real term can be made equal to 50Ω. L_g is added in series to provide resonance at the center frequency. Thus, the maximum signal is collected and gain could be optimized. To obtain the power match at resonance the real part of the input impedance also must be equal to source resistance. For the noise figure calculation, the size of the input transistor is chosen such that it minimizes the noise as shown in the following expressions [4]:

$$W_{opt} \approx \frac{1}{3.w.L.C_{ox}.R_s} \qquad (2)$$

with R_s = 50Ω and L is the gate length. It must be noted here that in the above calculation the noise parameters γ, δ and c are considered as independent of the bias voltage and hence, the W_{opt} value is not exactly one that width optimization requires. All the inductors used in this design are the integrated spiral types except L_g, used for tuning purpose. The target NF is 1.8 dB. Since the NF requirements depends on the input configuration as well as bias current, we use optimum bias current as 4.2 mA and devices width 120-μm for M_1-M_2.

At the input, the off-chip capacitor C_B is a DC blocking capacitor. A small value of shunt capacitance C_s (~ 110 fF) at the input optimizes the gain and noise of the LNA. This shunt capacitor C_s

corresponds to pin and pad capacitance of the package. Transistors M_3 and M_4, known as cascode devices, form a common gate stage, cascode the input stage. The advantage of using the cascode device is that, it basically shields the output from the input stage. It highly increases the reverse isolation S_{11}. A higher reverse isolation lowers LO leakage and increases stability. The common gate stage presents low input impedance leading to a low voltage gain in the input stage.

In addition to the cascode devices, we implement a differential pair betweentrans conductors and load which has variable gain feature. These transistors are controlled by a control voltage (Vcont) for steering the signal current between LC load and voltage supply resulting in 9 dB gain reduction. Moreover, two capacitor arrays and which are regulated by the Vcont, reduces the gain by an additional 3 dB. The advantage of realizing all the gain reduction at the LNA outputs is that the LNA will have minimum noise figure in both low and high gain modes.

At the output, the inductor L_T, the metal-insulator-metal capacitors C_1, C_2 and the total drain-node capacitance of M_3 and M_4 compose an output LC resonance tank circuit. Capacitors C_1, C_2 perform capacitive transformation of the impedance level at the drain node to a desired lower output impedance level which is suited for reducing signal amplification. The DC current through the cascode stage is determined by the gate voltage of M_1 and M_2. This is generated by a CMOS g_m bias circuit which is shown in Fig. 2 and injected by a high value register to the gate terminal. The CMOS g_m bias circuit which consumes only 2 mA of current makes the LNA independent of temperature and voltage variations [5].

2.2 Mixer

Fig. 3 shows the double balance active mixer The design is based on a complex version of the ubiquitous current-steering CMOS form. The mixer structure is chosen to be a differential double balanced mixer for it's inherited insensitivity to LO-IF isolation. It also suppresses common-mode substrate noise and interference. The mixer comprises differential pairs driver stages (Q_1-Q_4) and four differential switching quad (Q_5-Q_{12}). The transconductors are inductively degenerated to achieve higher linearity. The driver stage amplifies the RF signals to compensate for the attenuation due to switching process, and to reduce the noise contribution from the switching quad. The two I and Q mixers are resistively loaded because of reducing flicker noise at outputs. Four mixers FETs are attached each driver stage. In order to improve linearity of the mixer, we consider a constant g_m CMOS cell technique as shown in the Fig. 3. The devices Q_3 and Q_4 form constant g_m cell [6] with input transconductors for enhancing linearity of the

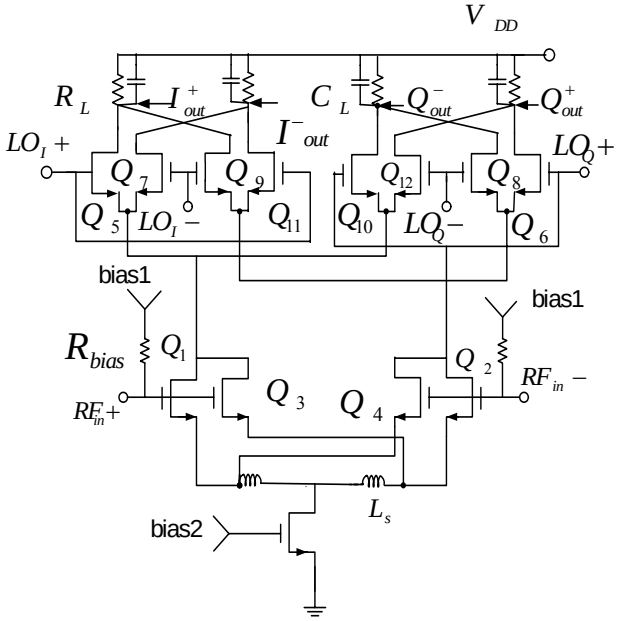

Fig. 3. Schematic of the mixer

LNA. In this configuration, each input differential pair behaves a reasonably linear transconductance over a small specified input voltage range. The overall transconductance is the sum of the individual offset transconductance and can be made roughly constant over an almost arbitrary large range of input voltage. We also used a CMOS g_m bias circuit as same as in Fig. 2 which is not shown in Fig. 3.

At the transconductor output, the signal is splited into I and Q paths inside the mixer. Independent I and Q LO signals (off-chip) are applied to create quadrature baseband paths. The transconductor output current splits between I and Q paths such that all of the transconductor current goes to the I branch at the the instance that the Q branch core is in its transitional state, and vice versa. Hence, each switching pair will not have any current at the balanced point which periodically lowers the noise figure to ensure low noise figure and the improvement in the conversion gain. At the output, the load capacitors are chosen such that it works as low pass filters with cutoff frequency at 45 MHz to

remove the strong out-of-band signals from the input to the baseband filters.

3 Simulation Results

The LNA and mixer were simulated independently with the cadence SpectreRF simulator. Figures 4 to 8 show simulation results of the VGLNA. We find that in the HGM and the LGM, the VGLNA achieves noise figure of 0.83 dB and 2.8 dB, with input return loss of -17 dB and -11 dB, respectively. As we see in the Fig. 5 that the reverse isolation at the LGM is slightly better than the HGM but the overall reverse isolation is less than -33 dB. We also find that LNA performs gains of 16.8 dB and 4.6 dB in the HGM and the LGM, respectively. As two-tone testing, two tones are located at 2.09 GHz and 2.08 GHz, respectively. Fig. 7 and 8 illustrate IIP3 in the HGM and LGM measured to be 2.13 dBm and 4.3 dBm, respectively.

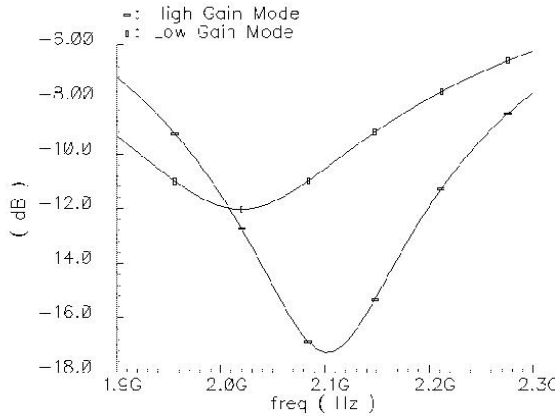

Fig. 4. S_{11} in the high gain mode and low gain mode of the LNA

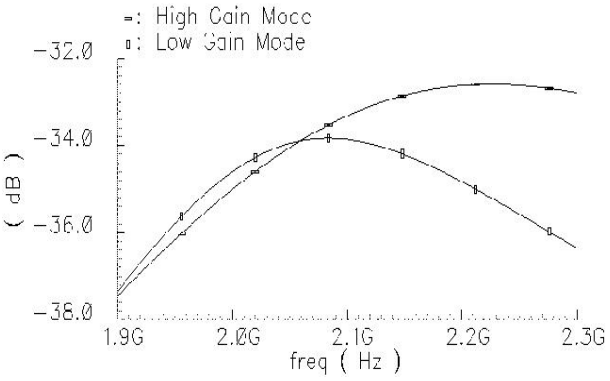

Fig. 5. S_{12} in the high gain mode and low gain mode of the LNA

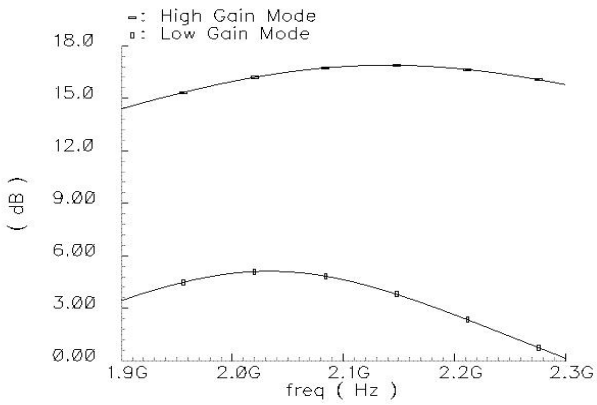

Fig. 6. Voltage gain in the high gain mode and low gain mode of the LNA

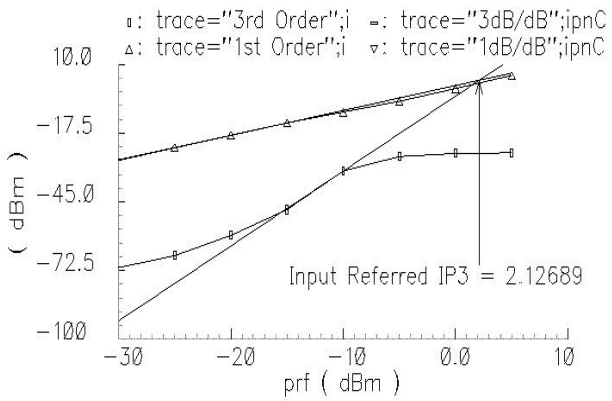

Fig. 7. IIP3 in the high gain mode of the LNA

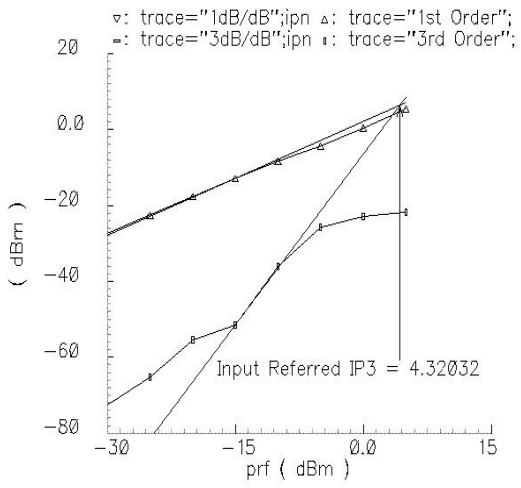

Fig. 8. IIP3 in the low gain mode of the LNA

On the other hand, figures 9 to 11 show simulation results of the mixer. The mixer achieves a conversion gain of 16 dB and an NF of 13.8 dB at 12 MHz output frequency. As two-tone testing, two tones are located at 2.09 GHz and 2.08 GHz, respectively. Fig. 11 illustrates IIP3 measured to be 12.12 dBm. Table 1 and 2 summarize the performances of the LNA and mixer, respectively. Table 2 also compares the performace of this mixer with the one in [7].

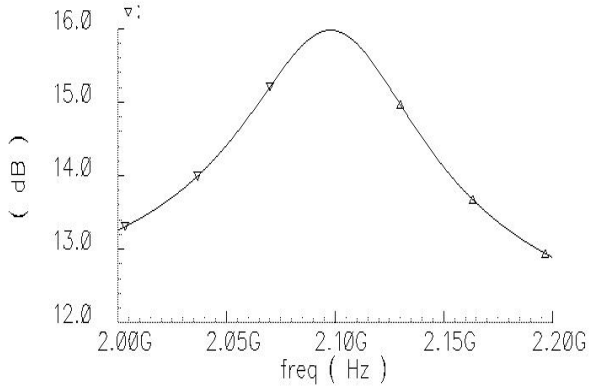

Fig. 9. Conversion gain of the mixer

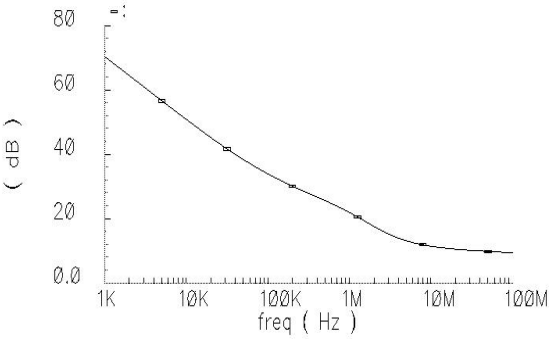

Fig. 10. NF of the mixer

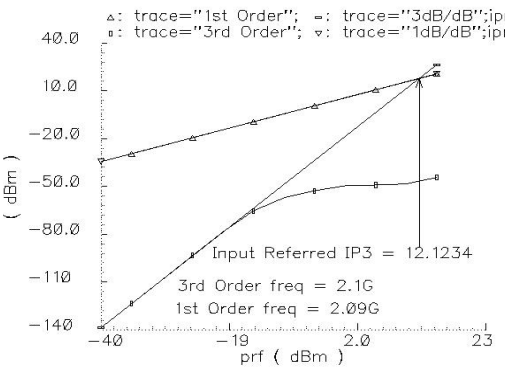

Fig. 11. NF of the mixer

TABLE 1
SIMULATION SUMMARY OF THE LNA

Parameter	LNA(HGM)	LNA(LGM)
Center frequency (GHz)	2.1	2.1
Current (core LNA) (mA)	4	4
$-\lvert S_{11} \rvert$ (dB)	-17	-11
$-\lvert S_{12} \rvert$ (dB)	-33	-34
$-\lvert S_{22} \rvert$ (dB)	-5.5	-12
Gain (dB)	16.8	4.6
NF (dB)	0.83	2.8
IIP3/iCP (dBm)	2.1/-9.5	4.3/-7.8
Supply Voltage (V)	1.8	1.8
Power Consumption (mW)	2.33	0.64
Technology	TSMC 0.18 µm	

TABLE 2
SIMULATION SUMMARY OF THE MIXER

Parameters	This work	[7]
Center frequency (GHz)	2.1	2.1
Current (core mixer) (mA)	5	2 × 6
Conversion Gain (dB)	16	12
NF (dB)	13.8	20.5
IIP3 (dBm)	12.12	13
LO Power (dBm)	-2	N.A
LO to RF feedthrough (dB)	-132	N.A.
Supply Voltage (V)	1.8	1.5
Power Consumption (mW)	9	2 × 9
Technology	0.18-µm CMOS	0.13-µm CMOS

4. Conclusion

This paper presents a variable gain LNA and I/Q mixer for a W-CDMA receiver in a TSMC 0.18-µm CMOS process. In the HGM and the LGM, the LNA achieves NF of 0.83 dB and 2.8 dB, with input return loss of -17 dB and -11 dB, respectively. These noise figures are the lowest reported noise figures for an active VGLNA. Operating at 1.8-V supply voltage, the circuit provides a maximum gain of 16.8 dB within -9.5 dBm 1dB compression and a minimum gain of 4.6 dB. In the linearity response, the LNA acquires IIP3 of 2.13 dBm in the HGM. One the other hand the mixer achieves an IIP3 of 12.12 dBm. Also, operating at 1.8-V supply voltage, the mixer provides a conversion gain of 16 dB. In the noise response, the mixer acquires of 13.8 dB noise figure. Using current steering technique, the power consumption of the proposed mixer mixer is 9.0 mW which is almost half of the traditional mixer design [7]. The achieved low noise figure, gain, low power dissipation and overall IIP3 fulfill the specifications for a UMTS LNA and mixer design [8]. In the future work, the LNA and mixer can be integrated together on the same chip to achieve amplification in a WCDMA receiver which requires RF designers to design fully integrated, low noise and low power consumption architectures for SoC applications.

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