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High-Speed Hardware Efficient FIR Compensation Filter for Delta-Sigma Modulator Analog-to-Digital Converter in 0.13 μm CMOS Technology

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Abstract: - A high-speed hardware efficient 41-tap, 15-bit word length Finite Impulse Response (FIR) Compensation Filter has been designed as a component in a Delta-Sigma Modulator (DSM) Analog-to-Digital Converter (ADC). The filter is targeted for high-throughput by pipelining its adders and multipliers. Efficient circuit-level techniques, namely customized adders, multipliers and D-flip-flop (DFF) are used to further improve performance. The FIR filter is implemented in CMOS 0.13 μm technology which contains approximately 180K transistors and occupies 2.69 mm^2 area. The filter is capable of operating at a maximum clock rate of 1.25 GHz.

Key-Words: - High-Speed, Delta-Sigma, ADC, FIR Filter, Compensation

1 Introduction

CMOS digital circuits have evolve into a prevalent choice for hardware implementation in the ever advancing integrated circuit (IC) industry. Digital signal processing (DSP) has become a mature and prominent technology in cellular phones, personal digital assistants, still-image cameras, video cameras, and video recorders, where they provide superior performance, at lower cost, lower power, and compact designs as compared with analog circuits. DSP has been used to transform or manipulate analog or digital signals for a long time. One of the most frequent applications is the filtering of a signal. Digital filters are implemented using electronic digital circuits that perform the operations of delay, multiplication, and addition [1]. Analog filters are implemented using resistors, inductors, capacitors, and, possibly, amplifiers [2]. The values of these analog components can drift over time and their precision is limited. In addition, especially when filtering takes place at low frequencies, inductors are often large and heavy. The multiplier coefficients of digital filters are established by the circuitry and do not drift. Digital filters can be implemented using low power digital integrated circuits so that per unit cost of digital filter construction is less than a comparable analog filter [2].

This paper presents the design and implementation of a high-speed and hardware efficient pipelined FIR Compensation Filter for a DSM ADC. With the pipelining of the adders and multipliers of the filter, very high throughput can be achieved. To further increase the performance of the compensation filter for achieving high-speed, full customized square-root select adders, carry-save multipliers and low-power DFF are used. The filter is custom designed and implemented in IBM 0.13 μm CMOS 8SF process.

2 Background

This section first provides the application of FIR Compensation Filter as a component in a DSM ADC, and then reviews the background of FIR digital filters architecture and design.

2.1 FIR Compensation Filter in DSM ADC

DSM ADC shapes the magnitude of the quantization noise so that the noise is reduced at lower frequencies and increased at higher frequencies. If the input signal is confined to a relatively small band compared to the ADC sampling frequency, then the resolution is increased by passing the digital output of the DSM through a low pass filter. It is well documented that an effective low pass filter for a DSM ADC of order L is a cascade of L+1 SINC low pass filters. For example, a first order DSM would incorporate a cascade of two digital SINC low pass filters to reject the high frequency quantization noise [3, 4]. The transfer function for a cascade of two SINC filters is

$$[HSINC(f)]^2=[\sin(M*\pi*F)/M*\sin(\pi*F)]^2 \quad (1)$$

where $F=f/f_s$ and M=number of bits low pass filter output. The frequency response for the $[HSINC(f)]^2$ filter is shown in Fig. 1.

Ideally the low pass filter should have a magnitude of one in the frequency range of 0 to fb; however the SINC filter has a substantial droop in magnitude at the upper region of baseband that must be precisely compensated by a second digital compensation filter. Thus in the pass band, the compensation filter must have a transfer function HFIR (f) so that HFIR (f) * $[HSINC (f)]^2$ has a value of one with an error that is less

than the resolution of the ADC. If the resolution of the ADC is 12 bits, then the error must be less than 2^{-12}. At the same time, the gain of the compensation filter in the stop band must be such that HCOMP (f) * $[HSINC (f)]^2$ is small enough so that the noise is sufficiently rejected outside the pass band to support the 12 bit resolution. A block diagram of the DSM ADC with the low pass cascaded SINC filters and FIR compensation filter is shown in Fig. 2.

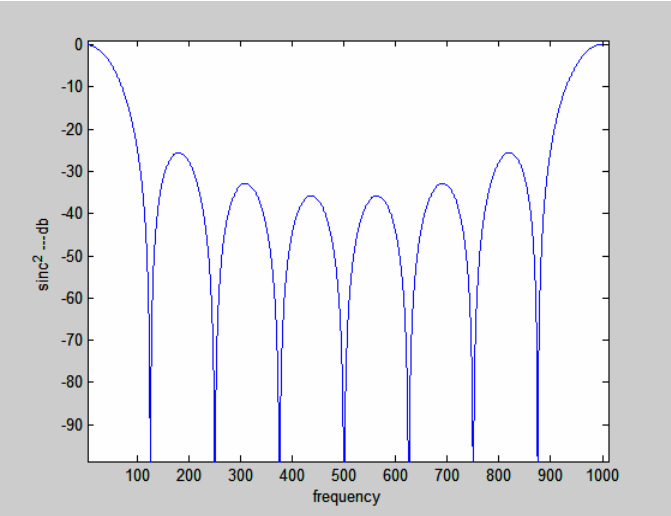

Fig. 1 $[HSINC(f)]^2$ Frequency Response, M=8, f_s=1GHz

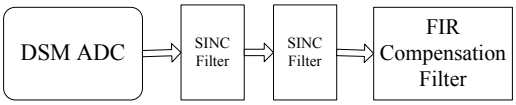

Fig. 2 DSM ADC with Filters

A 41-tap with 15-bit data and 15-bit coefficient linear phase FIR filter has been designed to give the desired frequency response for the compensation filter as shown in Fig. 3. As seen in Fig. 3, the frequency response of the 41 taps FIR Compensation filter is equal to $1/[HSINC (f1)]^2$ in the pass band of 0 to 50 MHz.

The product of the frequency response for the cascaded SINC filters and the FIR Compensation filter must be precisely equal to 1 in the pass band (error < 2^{-12}). The combined frequency response for the cascaded SINC low pass filter and the FIR Compensation filter is of the form shown in Fig. 4.

The filter coefficients for the 41-tap linear phase FIR Compensation filter is shown in Table 1. The floating point representation of the coefficients was produced using a custom MATLAB algorithm that insures the required accuracy for compensation in the pass band, while maintaining sufficient rejection in the stop band [5]. A Java code was written to convert the coefficient to Q*n.m* format.

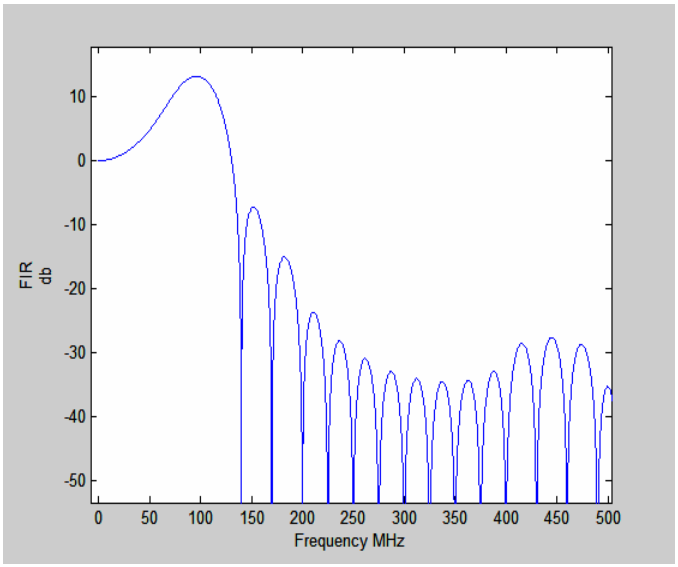

Fig. 3 Frequency Response for 41 Taps FIR Compensation Filter

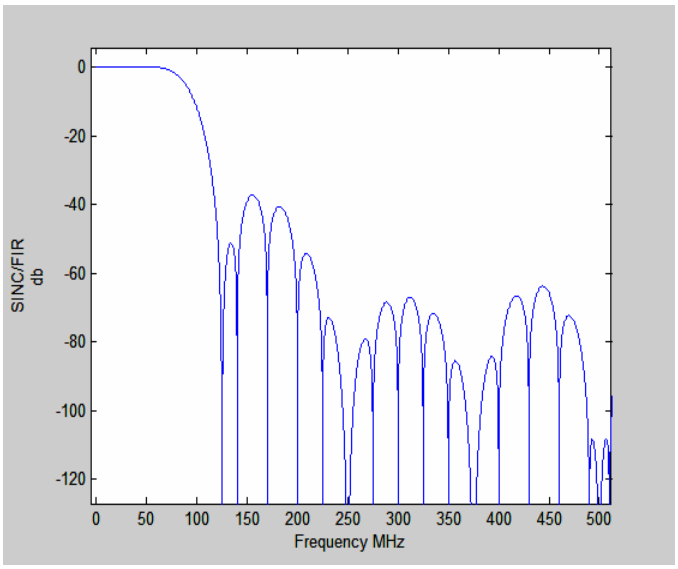

Fig. 4 Combined Frequency Responses of Cascaded Sinc Filters and 41 taps FIR Compensation Filter

2.2 FIR Digital Filters

Finite Impulse Response (FIR) filters are digital filters that have a unit impulse response that is finite duration. Fig. 5 illustrates the direct form FIR filter. The implementation of the filter requires *N* multiplications and *N* additions for each output sample. The transfer function for the FIR filter can be expressed as:

$$H(z) = \sum_{k=0}^{L-1} h(k) z^{-k} \qquad (2)$$

where L is the number of taps.

Linear phase FIR filters are preferable because the phase shift of the output is a linear function of the frequency and it has a symmetrical property. The symmetrical property of linear phase FIR filter allows us to design a hardware reducing configuration filter where the delayed signal is fed back to halve the number of multipliers required [1] as shown in Fig. 6. Although extra summing adders are required, it has only half the number of inputs and thus is simpler to implement [1]. Therefore, the linear phase FIR filter reduces the number of multiplications required from N to $(N/2) + 1$. The transfer function for the linear phase FIR filter can be expressed as:

$$H(z) = z^{-L}[h(0) + \sum_{k=1}^{L} h(k)(z^{k} + z^{-k})] \qquad (3)$$

where L is the number of taps.

Table 1 Filter Coefficients for 41-Tap Linear Phase FIR Filter

Taps	Coeff.	Coeff. in Q*n.m*
20	0.933	00000.1110111011
19, 21	-0.866	10000.1101110110
18, 22	1.319	00001.0101000110
17, 23	0.168	00000.0010101100
16, 24	1.027	00001.0000011011
15, 25	-0.211	10000.0011011000
14, 26	0.385	00000.0110001010
13, 27	-1.542	10001.1000101011
12, 28	0.548	00000.1000110001
11, 29	-3.260	10011.0100001010
10, 30	1.366	00001.0101110110
9, 31	-2.555	10010.1000111000
8, 32	3.420	00011.0110101110
7, 33	1.006	00001.0000000110
6, 34	1.424	00001.0110110010
5, 35	1.876	00001.1110000001
4, 36	-6.002	10110.0000000010
3, 37	3.710	00011.1011010111
2, 38	-8.431	11000.0110111001
1, 39	10.047	01010.0000110000
0, 40	-3.397	10011.0110010110

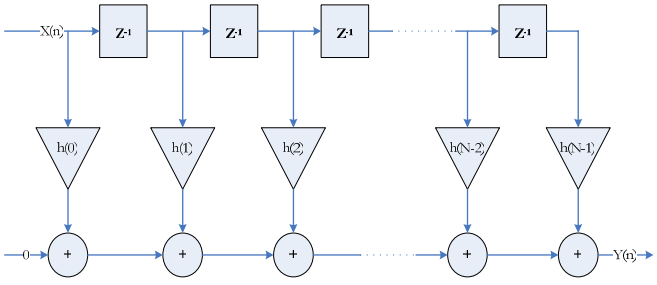

Fig. 5 Direct Form FIR Filter Design

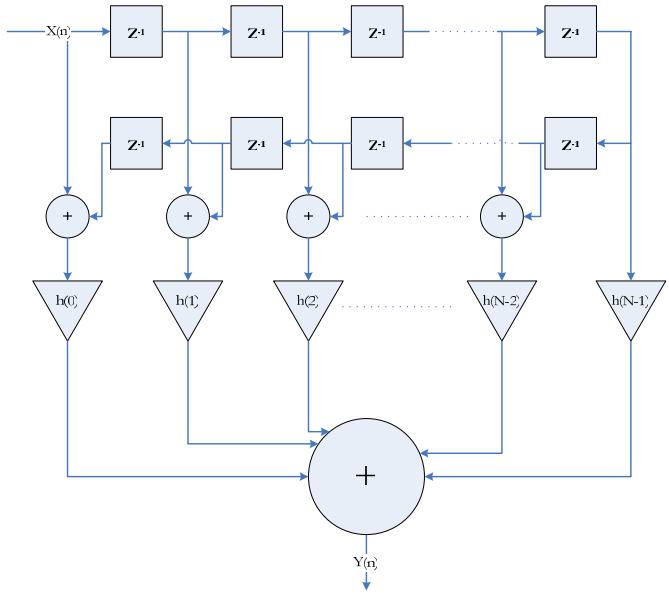

Fig. 6 Linear Phase FIR Filter Design

3 Filter Implementation

The FIR Compensation Filter implementation is now considered in more detail. The components of the FIR filter are discussed, followed by the discussion of the filter taps and final adder tree.

3.1 Delay Element

The delay element used in the implementation of the FIR Compensation Filter is the CMOS master-slave DFF. The delay element used for pipelining takes up about 15% area of the entire filter. Therefore, an excellent DFF design which has a delay of 70.49 ps and area of 132.66 μm^2 is chosen.

3.2 Adder

The adders used in the FIR compensation filter are in the range between 12 to 24 bits. In order to meet the high speed requirement of the compensation filter, a very fast adder is required. Square-root Carry Select Adder (CSA) was chosen because it is considered as a compromise solution between Ripple Carry Adder (RCA) and Carry Look-Ahead Adder (CLA) [$O(\sqrt{n})$ time and $O(2n)$ area], hence it is a good tradeoff between the compact area of RCA and the short delay of CLA [6].

3.3 Multiplier

The multiplier is the heart of the FIR compensation filter. It takes up about half of the size of the compensation filter. Careful optimizations have been taken into account to reduce the complexity and area of the multipliers. As discussed above, the FIR coefficients are fixed. Thus, the FIR compensation filter design can

exploit this fixed coefficient aspect to build a high speed, hardware efficient multiplier. The challenge remains to map the filter design into a suitable architecture. Note that the coefficients in Table 1 are truncated to three decimal fractional digits. This coefficient accuracy is consistent with the required 12 bit ADC resolution. The coefficients can be represented in binary form to the same accuracy using equation 4.

$$h(i) = \sum_{k=-10}^{k=3} C_k 2^k \qquad (4)$$

where $C_k = 0$ or 1

The compensation filter then can be designed according to the linear phase FIR filter design as shown in Fig. 6. A generic *nxn* array multiplier was considered for building the multipliers but it was deemed impractical because of the wide word length. It required a large area.

Out of the 21 coefficients in Table 1, only 6 coefficients have 50% and above number of 1s. Therefore, an easy solution to reduce hardware is to exploit the large number of 0s in the filter coefficients. To avoid wasting area and power for fixed filter coefficients, multiplication can be realized more efficiently with shift-and-add, by executing only the operations corresponding to the bits set to 1 in the coefficients. This idea is presented in Fig. 7 using a 4x4 array multiplier for simplicity with a coefficient of 0101.

The multipliers stages were reduced tremendously with the area optimized shift-and-add multiplier but it still cannot reach the desired clock speed. In order to work with high speed and high throughput, the multipliers had to be pipelined. As the multipliers are in canonical form, it was easy to pipeline them at the bit level to achieve high throughput.

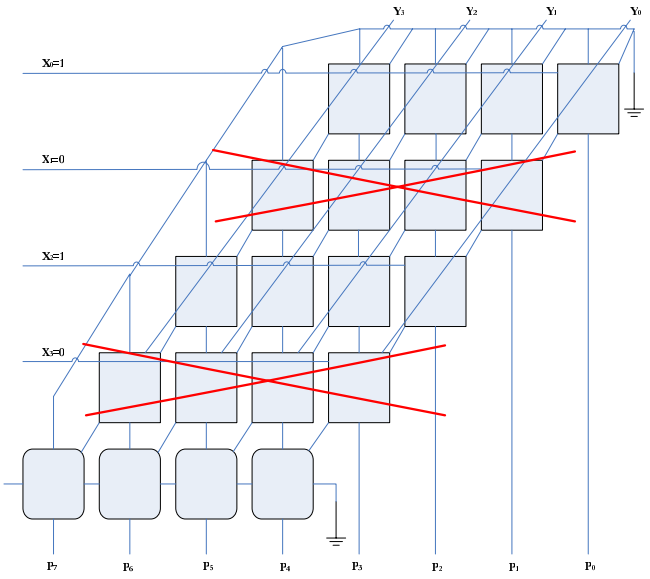

Fig. 7 Area Optimized Shift and Add Multiplier

3.4 Filter Taps

The pipeline FIR Compensation Filter taps are built with the adder and multiplier discussed above. The taps are built according to Fig. 6 with the tap structure of Fig. 8. The first tap had to be constructed slightly different, it is without the 13 bits input adder.

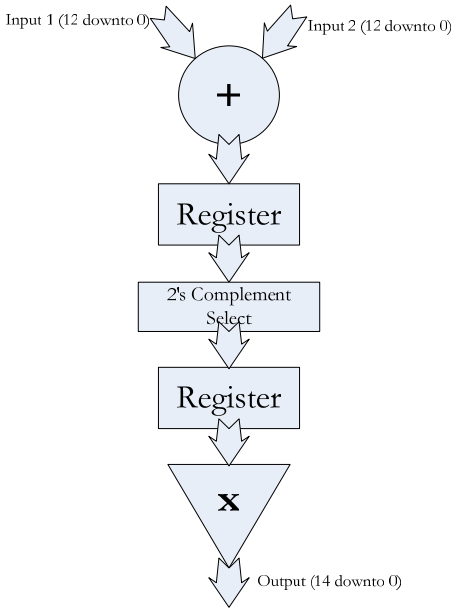

Fig. 8 Tap Structure of Compensation Filter

3.5 Adder Tree

The final block of the compensation filter is the adder tree. The output from the taps must be summed up to form the filter output. A straight forward approach would be to cascade 20 adders. This however would deem an unfeasible solution as it would introduce long propagation delays. Furthermore, the timing and throughput requirement for the FIR Compensation Filter could not be fulfilled.

Pipelining the multipliers would not be enough to ensure the required speed and throughput because the output of the multiplier is 15 bits. With the wide output from the multipliers, addition also takes significant time. Also, to further improve throughput of the compensation filter, the critical path in the adders needed to be shortened. Thus, adders as well as multipliers needed to be pipelined. Due to the pipelined multipliers, the outputs from the multipliers have different clock arrival time. This would change the timing difference of the two inputs of the next adder from one clock cycle to more than one clock cycle, which would cause incorrect addition output. In order to solve this problem, an adder tree had to be used to balance the timing difference between the two inputs of the adder by one clock cycle. With the use of an adder tree the number of adders, switching capacitance and propagation delay was reduced. The balance adder tree is shown in Fig. 9.

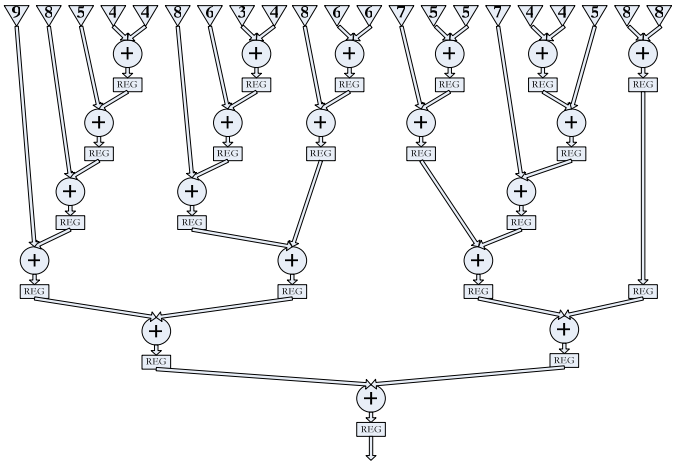

Fig. 9 Balance Adder Tree for FIR Compensation Filter

4 Results and Analysis

The FIR Compensation Filter was simulated with Cadence Analog Simulator. In addition, the top-level filter design was also simulated in Cadence Analog-Mixed-Signal (AMS) environment. A 13 bit ideal ADC was written in Verilog-AMS to generate digital outputs for the FIR compensation filter.

The layout of the filter was designed and placed using Virtuoso XL Layout Editor (VXL). Then, it was routed with Cadence Chip Assembly Router (CCAR).

Table 2 compares the characteristics and performance of the 41-tap FIR Compensation Filter with some previously published designs.

Table 2 Comparisons of Current FIR Filter Characteristics and Performance with Various Previously Published Designs

	[7]	[8]	[9]	[10]	This Work
Taps	10	16	24	10	41
Word Length	17	7	23	6	15
Operating Frequency	175.44 MHz	225 MHz	55 MHz	1.30 GHz	1.25 GHz
Throughput	N/A	N/A	287.5 Msam/s	1.32 Gsam/s	1.28 Gsam/s
Voltage	2.5V	3.3V	2.0V	2.1V	1.2V
Area	5 mm^2	0.13 mm^2	4.01 mm^2	0.46 mm^2	2.69 mm^2
Process	0.25 μm	0.35 μm	0.35 μm	0.18 μm	0.13 μm
Implement Methods	ASIC	Full Cust.	FPGA	Mixed Cust. & ASIC	Full Cust.

5 Conclusions

A 41-tap Linear Phase FIR Compensation filter for Delta-Sigma Modulator Analog-to-Digital Converter has been presented. It is area optimized while maintaining high throughput. The filter operates up to 1.25 GHz without distortion. Its adders and multipliers are pipelined to obtain high throughput. The compensation filter is area efficient because it adopts the linear phase methodology. The custom designed multipliers further reduce the hardware cost of the filter, which yielded a relatively small area of 2.69 mm^2.

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