Architecture Design for an Adaptive Equalizer

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Abstract : - In this paper, an adaptive equalizer using LMS algorithm has been simulated using MATLAB software. Also the variants of LMS algorithm sign- sign, sign-data and sign-error are simulated for low complexity adaptive equalizer. Analysis of mean squared errors for LMS and its variants have been done. From the results of matlab , input data is taken for VHDL simulation of LMS adaptive equalizer. The output from VHDL simulation is plotted using matlab. Architecture for LMS adaptive equalizer is discussed here and simulation results have been obtained.

Keywords **: -** Adaptive, LMS, MMA, MSE,RLS, VHDL

1 Introduction

To circumvent the channel impairment caused by multipath fading, more and more receivers resort to adaptive equalizers. An adaptive equalizer is essentially a linear adaptive filter used to model the inverse transfer function of the channel. The Adaptive algorithms are classified as Stochastic gradient algorithms and Exact least Square algorithms. Stochastic gradient algorithms include self orthogonalizing algorithms as a subclass. In each case, there are two basic ways (sample by sample basis and block by block basis) in which the free parameters of the algorithm are updated [6].

The conventional least mean square (LMS) algorithm (with sample update), normalized LMS algorithm and block LMS algorithm (with block update) are all stochastic gradient algorithms. Recursive Least Squares (RLS) algorithm is least squares algorithm. Out of these algorithms, LMS and RLS algorithms are popularly used. RLS algorithm has better convergence speed than LMS. But the complexity for hardware implementation is very high. LMS algorithm is widely adopted in hardware implementation because of its simplicity and robustness.

The paper is organized as follows. In section 2, structure of adaptive filter during training mode and the variants of LMS algorithm are discussed. The matlab simulation results have given in section 3. The floating point representation used in VHDL (Modelsim) simulation of LMS equalizer is presented in section 4 along with the multiplexed multiplier architecture design for adaptive equalizer.

2 LMS and its variants

The Least mean square algorithm that is based on an approximated stochastic gradient computes an estimate of the LMS solution at every time step. The computation can be divided into three steps: Computing the filter output: $Y(n) = W^T(n). X(n)$, computing the error $e(n)=d(n) - y(n)$and adapting filter weight $w(n+1)=w(n)+\mu.X(n)e(n)$. The step size parameter is denoted by μ W(n), e(n) and X(n) represent the coefficient of the feed forward filter ,the error signal and the input signal respectively. The optimization criterion is the LMS error. Hence the mean square is minimized at every time instant. While implementing a low complexity adaptive equalizer , the LMS algorithm is usually simplified to the sign-error(sign-data)LMS algorithm by replacing e(n) [X(n)] with simply the sign of e(n) [X(n)] .The sign-sign LMS algorithm can be used to further reduce the implementation complexity by employing only the signs of e(n) and X(n) for updating.

The basic configuration of the system simulated for adaptive equalizer consists of the following modules as shown in the figure 1 [8].

Transmitter : Data generator can be used to generate the input signal data. The delay must be introduced to the output of data generator to compensate the delay the signal encountered in the channel filter and equalizer. The delay may be set to the largest integer closest to{ (K+N)/2}.

Channel filter : It is an Finite impulse response (FIR) filter module with the coefficients c(n), { $0 \le n \le K-1$} that simulate channel distortion. The channel can also be modeled by the impulse response of raised cosine function.

Noise generator : It is used to generate the additive noise generally present in the digital communication system.

Adaptive Equalizer: It is an FIR filter with tap coefficients {h(k),0<=k<=N-1}, which are adjusted by adaptive filtering algorithm like LMS, sign-data LMS, sign-error LMS and sign-sign LMS .

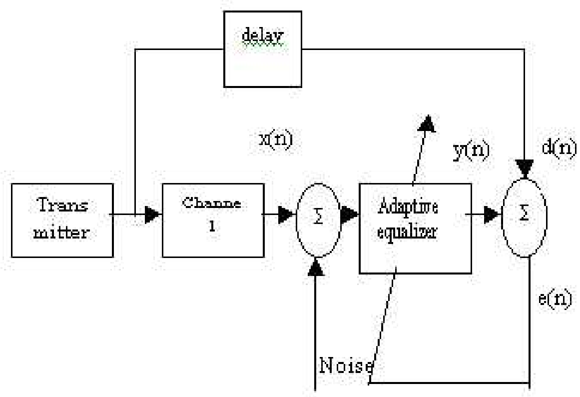

Fig .1:Structure of adaptive equalizer

3 Matlab simulation results

3.1 FIR filter as a channel

Simulation of two tap LMS adaptive equalizer is shown in figure 2 for 500 samples. The channel is considered as FIR filter with two taps with coefficient values [1,0.6] .

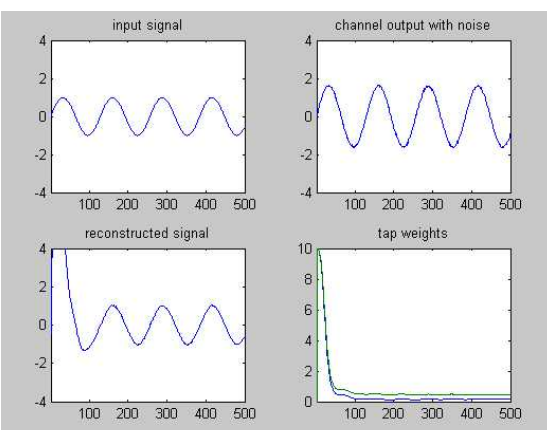

Fig . 2 : LMS two tap equalizer

3.2 Raised cosine channel

Simulation of eleven tap adaptive filter (Equalizer) using MATLAB software has been done and the input signal, channel output with added noisy signal, reconstructed signal and filter taps are plotted. The impulse response of the channel is described by the raised cosine

$$h_n = \begin{cases} 0.5 * [\, 1+ \cos\,((2\Pi / W)^* (n-2))\,], & n = 1, 2, 3 \\ 0, \text{ otherwise} \end{cases}$$

where the parameter W controls the amount of amplitude distortion produced by the channel, with the distortion increasing with W. The noise generator is gaussian noise with zero mean and a variance 0.001 [6].The simulation results for LMS adaptive equalizer for μ =0.075 with W = 2.9 are shown in Figure 3.

The results of sign-data LMS adaptive equalizer are shown in Figure 4 with μ =0.075 and W = 2.9.With the less computation involved, the results of sign-data LMS are comparable with LMS algorithm. The simulation results of sign-error LMS are shown in Figure 5 with the same μ and W. The transmitted signal can be reconstructed with low convergence speed. The simulation results of sign-sign LMS are shown in Figure 6 with the same μ and W. The transmitted signal can be reconstructed with some distortion. This distortion can be eliminated by adjusting the value of step size μ.

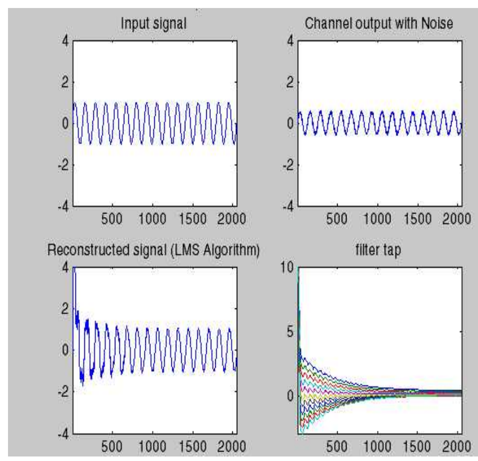

Fig .3:LMS algorithm (11 tap)

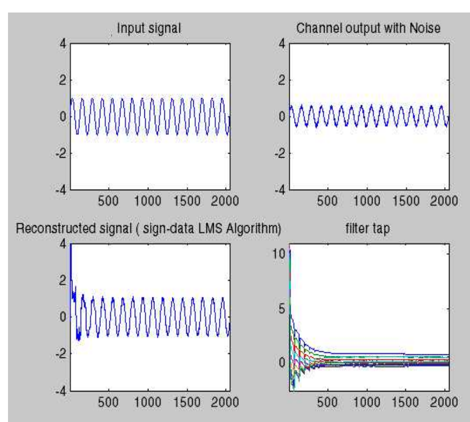

Fig. 4: sign-data LMS algorithm(11 tap)

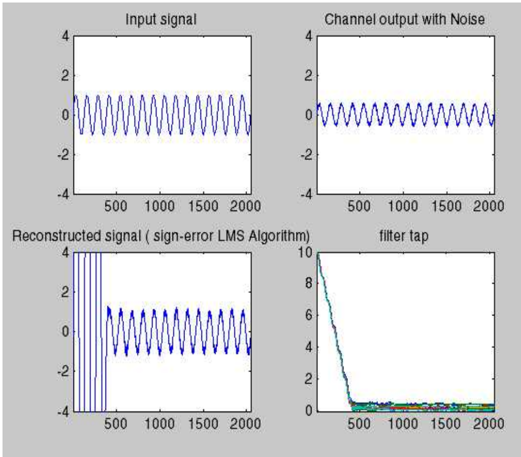

Fig. 5: sign - error LMS algorithm(11 tap)

Plot of mean squared error (MSE) “e^2 (n) versus n” for LMS algorithm is shown in the figure 7. Error decreases at each time step and the weights converge with error reduces to zero. Similarly plots have been obtained for sign-data LMS,sign-error LMS and sign-sign LMS algorithms as shown in the figures 8,9 and 10 respectively. Mean squared error of sign-data LMS is comparable to LMS algorithm with less computation involved. By Comparing mean squared errors, the MSE of sign-sign is high for the same μ..By choosing the proper value of μ. as 0.001415 the MSE is reduced with the low convergence speed as compared to conventional LMS as shown in the figure 11. By choosing the proper value of step size, the converging speed of sign-sign LMS can be improved [7].

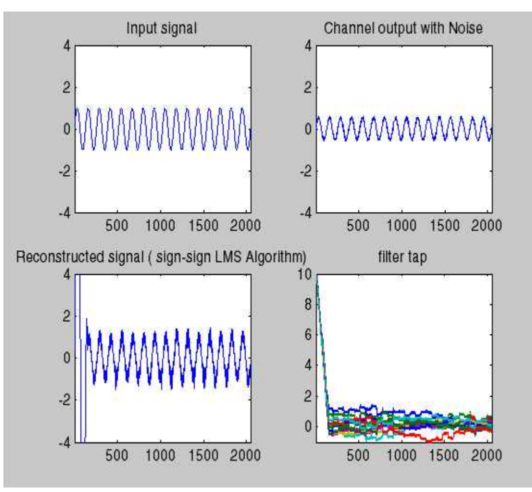

Fig. 6:sign-sign LMS algorithm (11 tap)

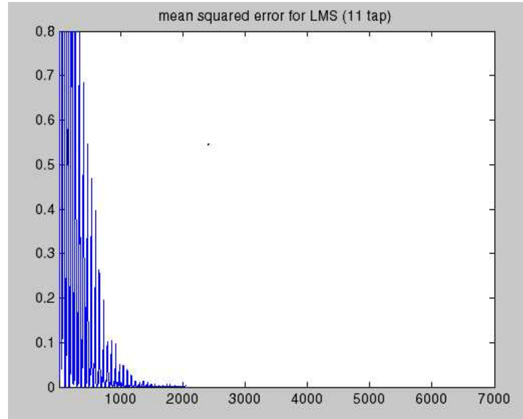

Fig. 7 : Mean squared error for LMS with μ =0.075 .

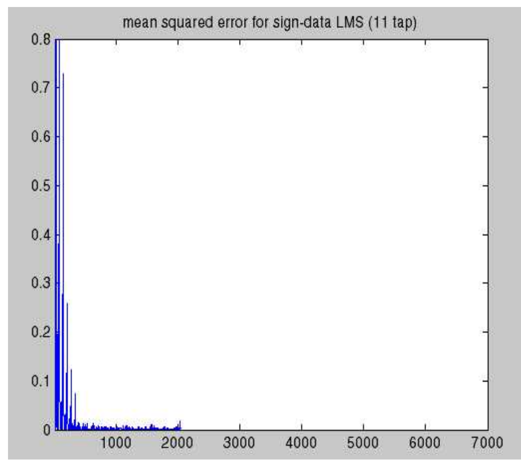

Fig. 8: Mean squared error for sign-data LMS with μ =0.075

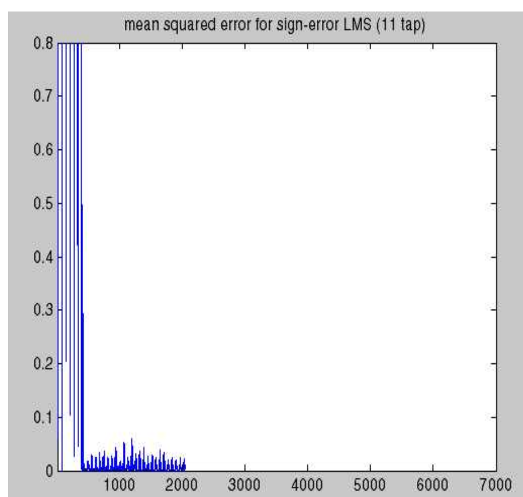

Fig. 9 :Mean squared error for sign-error LMS with μ =0.075

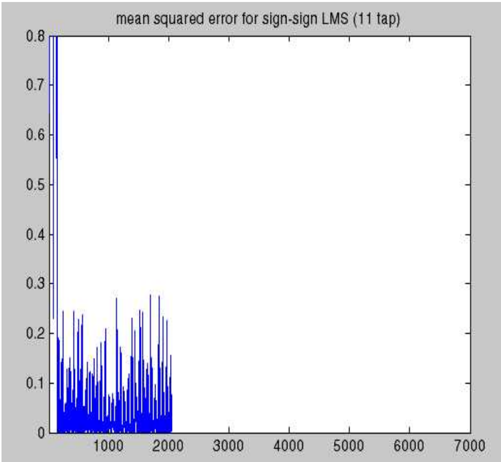

Fig. 10 :Mean squared error for sign-sign LMS with μ =0.075

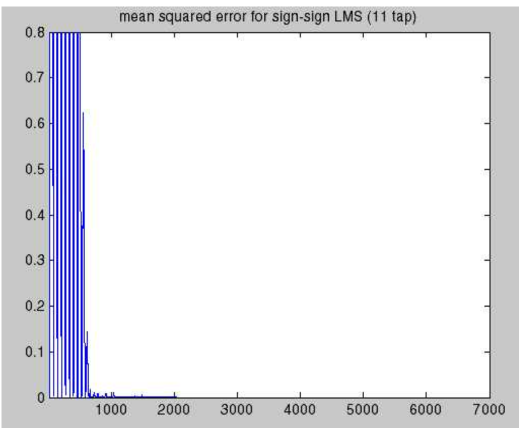

Fig. 11 :Mean squared error for sign-sign LMS with μ =0.001415

4 VHDL Simulation

From the results of matlab , five hundred samples of input signal x(n) and desired signal d(n) have taken and two tap LMS adaptive equalizer is simulated using VHDL. The three parts of LMS algorithm is designed with the architecture shown in the Figure 12. The following equations are designed with this architecture.

Y(n) = W0(n-1)X(n)+W1(n-1)X(n-1). (1)
e(n)=d(n)-Y(n). (2)
W0(n)=W0(n-1)+ μe(n).X(n). (3)
W1(n)=W1(n-1)+ μe(n).X(n-1) (4)

In the above architecture ,each tap requires two multipliers for computing filter output and updating the filter weight. And one more common multiplier for μ multiplication. To reduce the number of multipliers the following architecture called multiplexed multiplier architecture is discussed in this section .

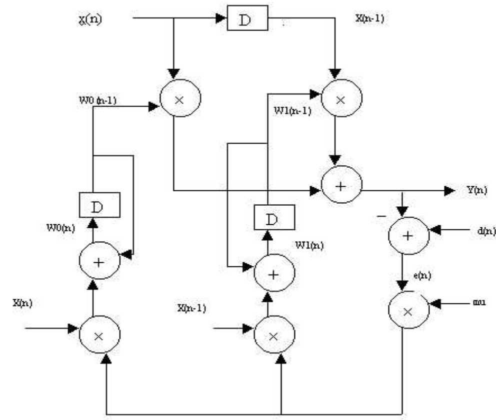

Fig. 12: Architecture of two tap LMS equalizer

4.1 Multiplexed multiplier architecture

The figure 13 describes a fully parallel MMA architecture that dedicates each hardware multiplier to each corresponding filter tap. The multiplexer multiplexes between the filter tap weights and the error values. In other words ,when the multiplexer control bit is set to '1' ,the filtering operation is performed and when the control bit set to '0' , the weight update operation is performed .In this architecture ,multipliers are reused ,i.e.. multiplexed in time,for both filtering and adaptation. This design employs 'M' number of multipliers, where 'M' denotes the number of taps [2].

4.2 Low Complexity Architecture

To have low complexity architecture ,variants of LMS algorithm sign-data LMS,sign-error LMS and sign-sign LMS are considered [7]. In sign-data LMS and sign-error LMS number of multiplications are reduced in updating operation. In sign-sign LMS no multiplications are required in updating operation.The updating equation is reduced to
W(n+1)=W(n) + μsign(X(n)).sign(e(n)). (5)
This requires only exclusive OR gate and adder and hence leads to low complexity architecture .

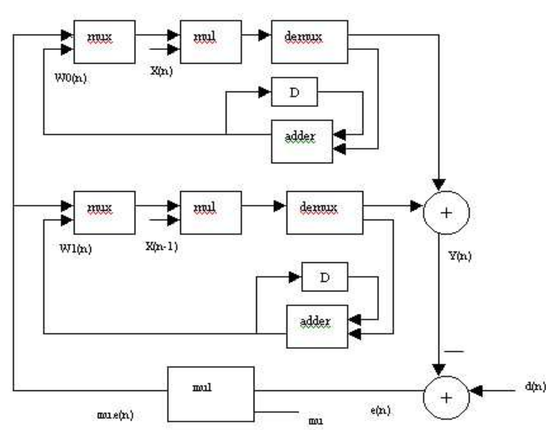

Fig. 13 Multiplexed Multiplier architecture for 2 tap LMS adaptive equalizer

4.3 Floating Point Format Representation

Many algorithms rely on floating point arithmetic for the dynamic range of representations and require millions of calculations per second [5]. The 18-bit floating point format was used in the design of architecture .This format was chosen to accommodate specific requirement: the dynamic range of the format needed to be quite large in order to represent very large and small, positive and negative real numbers accurately, Based on these requirements the format in Figure 14 was used.

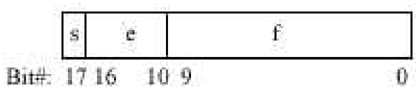

Fig. 14 : 18 bit floating point format

The 18 bit floating point value (v) is computed by: $v = -1^{s}\, 2^{(e - 63)}\, (1.f)$ The range of real numbers that this format can represent is $\pm 3.6875 \times 10^{19}$ to $\pm 1.626 \times 10^{-19}$.

In the design of LMS adaptive equalizer architecture, floating point representation is used in adders and multipliers. The input to VHDL design is in floating point representation. The real valued inputs ‘X’ and ‘d’ are taken from matlab and converted to floating point and stored in separate text files. The VHDL simulation output is taken which is in the floating point representation is converted to real values and output is plotted using matlab (figure 15).This VHDL simulation plot for 500 samples is similar to the reconstructed signal (figure 2) obtained in matlab.

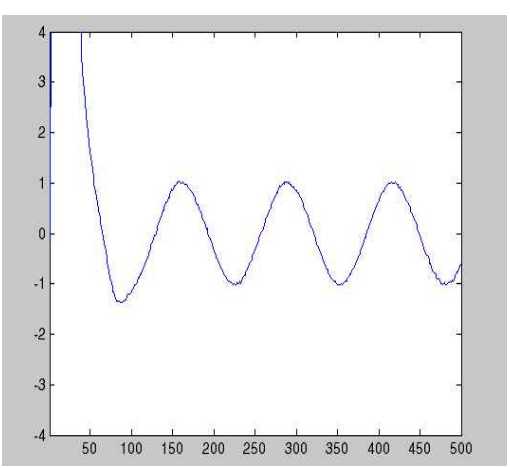

Fig. 15 : Reconstructed signal - VHDL simulation result for LMS adaptive equalizer(2 tap)

Modelsim timing output is shown in figure 16 for LMS two tap adaptive equalizer .

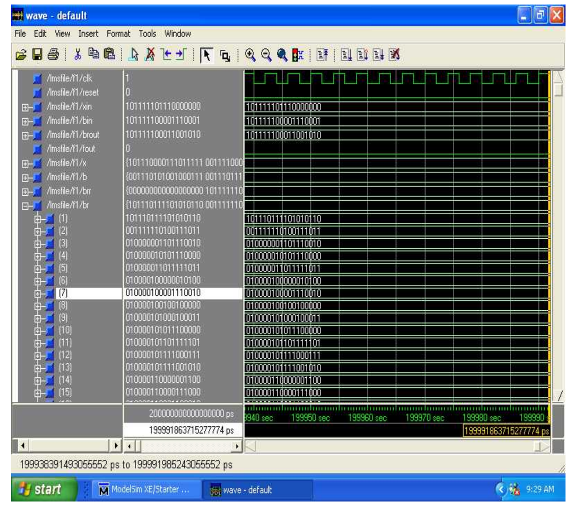

Fig. 16 : Modelsim Simulation waveform

5 Conclusion

Matlab simulations for the LMS algorithm and the variants of LMS algorithm sign-sign LMS, sign-error LMS and sign-data LMS are verified and their feasibility is tested for eleven tap adaptive equalizer. VHDL simulation of two tap adaptive equalizer is tested for LMS algorithm. Multiplexed multiplier architecture is proposed for LMS adaptive equalizer in order to reduce the number of multipliers .

To reduce the hardware complexity and feedback latency still more ,sign-sign LMS algorithm can be used for VHDL simulation of adaptive channel equalizer which results in area and power savings. On the other hand the converging speed is low compared to normal LMS algorithm. But this can be compensated by choosing proper value of step size. As the power consumption is very crucial for many portable applications, new techniques for the algorithm and the implementation of equalizers are still needed to further reduce their complexity and power consumption.

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