A HIGH SPEED CMOS INCREMENTER/DECREMENTER CIRCUIT WITH REDUCED POWER DELAY PRODUCT

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Abstract: – A novel circuit topology for the CMOS based Incrementer/Decrementer circuit is presented in this paper. The design methodology is extensively based on Domino logic and it utilizes a simple two level look-ahead structure. The highly parallel, regular structure of the proposed 8-bit decision module (DM) macro cell makes this design, especially advantageous for constructing higher order versions, facilitating an easier layout and test mechanism. For a 32-bit Incrementer/Decrementer circuit, based upon the proposed design, the savings in power delay product (PDP) are of the order of 65% and 38%, with a significant reduction in the number of transistors, in comparison with the best decision module designs reported in [1] and [2], based on a similar MOSIS 0.6 µm CMOS technology.

Key-Words: - Decision Module (DM), Incrementer/Decrementer, Proposed Priority Resolver (PPR), High Speed (HS) High Speed Low Power (HSLP), Power Delay Product (PDP)

1 Introduction
The Incrementer/Decrementer is a basic building block in digital systems, which counts up or down by one step in each clock cycle. It finds applications as program counter [4], frequency divider [5] etc. A general Incrementer/Decrementer circuit can be designed based on the Adder/Subtractor module or the Priority Resolution Module (PRM) block, as illustrated in [10]. The speed of operation of the Incrementer/Decrementer circuit is likely to reduce considerably, with an increase in the order of the bit-width or bit levels. The speed limitation of a conventional Incrementer/Decrementer circuit, based on the Adder/Subtractor module, comes from the carry signal propagation. For improvement in speed, we resort to a high-speed adder structure, such as the Carry Look-ahead Adder (CLA). But this is possible only with a greater compromise on the silicon real estate. On the other hand, if the Up/Down counter is used as an Incrementer/Decrementer, the speed limitation still springs from the carry propagation. This is due to the design of the Up/Down counter, relying upon the addition mechanism, although it utilizes a half adder circuit in place of a full adder structure. The PRM based Incrementer/Decrementer circuit design is somewhat area efficient, but its operating speed is however limited due to the delay, associated with the propagation of the priority token.

The rest of this paper is organized as follows. In Section 2, the conventional design approaches for the Incrementer/Decrementer circuit and their inherent limitations are described briefly. In Section 3, the basic circuit operation and a brief description of decision module design methodologies proposed in [2] are presented. In Section 4, we present our proposed 8-bit macro cell design of the decision module, the associated design equations and explain its operation. The performance evaluation results and comparisons are presented in Section 5. Finally, we make the concluding remarks in Section 6.

2 Conventional design approaches
2.1 Adder based Increment/Decrement Module
Fig.1 shows a 4-bit CLA based Incrementer/Decrementer [7]. The PG generator and the look-ahead carry generator are the root causes for the circuit complexity, though they are necessary for speeding up the operation of the circuit.

If only the increment or the decrement operation is required, then the circuit logic can be simplified. However, if both the operands are required simultaneously, then the adder/subtractor modules are required to remain. This acts as a deterrent from simplifying the complexity of the circuit. For the sake of increasing the bit-widths or in order to construct a higher order Incrementer/Decrementer, many such 4-bit units have to cascaded, which degrades the speed of operation due to the associated lengthy carry propagation chain.

2.2 Counter based Incrementer/Decrementer circuit
A 32-bit counter based Increment/Decrement module is shown in Fig.2 [4]. Since the half adder circuit is basically used for the function realization of the Incrementer/Decrementer, this circuit possesses a very regular structure.

This circuit has a long critical path, illustrated by the gray portion [1]. The critical path delay is directly and linearly proportional to the bit width of the circuit and this has an adverse impact on the speed of operation.

3 Basic circuit operation
In this section, we first explain the operation of the Incrementer/Decrementer circuit and then briefly discuss about the existing high-speed decision module (DM) blocks, cited in [2].

3.1 Circuit Operation
The Decision Module (DM) is the main functional block in the Incrementer/Decrementer circuit. It’s operation is similar to a Priority Encoder (PE) or a Priority Resolver (PR). Hereafter the terms DM, PE and PR will be used synonymously. Let the input data be 10111000. Each input bit should first be complemented. Assuming that the input data is still the same, the data to Decision Module (DM) will be 01000111 and the output
of DM will be 00000001, as illustrated in [2]. After the operation performed by the data-out selector, the output of DM is XORed with the input data and the final output is obtained as 10111001, which is the desired result. The decrement operation is somewhat similar and is elucidated in detail, available in [1] and [2].

3.2 High Speed 8-bit PR module

This high speed (HS) macro cell is implemented in the NP Domino CMOS logic. During the precharge phase (Clock=0), LA_inter and LA_out are 1 and 0 respectively and all the outputs are precharged to 1 in this phase. la0–la2 comprise the first level look-ahead signals. LA_inter is used to realize the second-level look-ahead functions, while LA_in and LA_out are used to realize the third level look-ahead function between two 8-bit macro cells. Though the circuit achieves a high speed performance, however the power consumption of this circuit is high. All the output bits are precharged to logic 1 in the precharge phase. During the evaluation phase (Clock=1), all but one output bit continues to remain in the high state, while others are pulled low. The high switching probability subsequently leads to higher power dissipation, as mentioned in [3].

3.3 High Speed and Low Power 8-bit PR module

Fig.5 shows the high speed and low power (HSLP) decision module macro. In comparison with the circuit in Fig.4, this circuit has two modifications. Firstly, for the first level look-ahead functions, the n-type dynamic gates with the series connected circuit structure are used to replace the p-type dynamic gates with an equivalent parallel-connected circuit structure. Secondly, several PMOS transistors MrFo–MrF7 controlled by the look-ahead signals are added, to prevent the circuit from going into the erroneous state.
This circuit still preserves the high speed characteristics, because of a similar multi-level look-ahead structure. Lower power consumption is possible, as all the outputs will evaluate in the evaluation phase, but with only one output, changing its state obtained in the precharge phase.

The power reduction is achieved with a slight trade-off with area and even with the introduction of multilevel look-ahead and multilevel folding techniques, reported in [2], there is slight speed improvement. However, this requires complex look-ahead signal routing, making the resulting circuit design and test mechanism difficult.

4 Proposed circuit design

4.1 Proposed 8-bit PR Module

Fig.6 shows the novel design of an 8-bit Priority Resolver macro cell (PPR), based on Domino CMOS logic. Fig.7 gives the circuit diagram for the 8-bit Incrementer/Decrementer macro, incorporating the proposed decision module block. This circuit design encompasses a highly regular and parallel architecture with a simple two level look-ahead structure. The proposed cell structure permits sharing of a similar evaluation chain of n-type transistors for the critical data path corresponding to the output EP7 and the look-ahead signal for the next subsequent stage, which is referred to as LA_inter, which is in sharp contrast to the separate transistor chains available for these signals, in the previous designs. This has enabled us in greatly reducing the transistor count for higher order versions, albeit improvement in performance.

4.2 Design Equations for the Macro cell

The design equations for the cell have been framed with an active high look-ahead or enable signal, in contrary to the active low signals, adopted in the earlier designs. This facilitates easier and a more regular realization of logic functionality for the different outputs, as indicated in Eqn. (1). This circuit implements the following simplified functions,

\[
\begin{align*}
EP0 &= LA_{\text{in}} \cdot D0 \\
EP1 &= LA_{\text{in}} \cdot D0 \cdot D1 \\
EP2 &= LA_{\text{in}} \cdot D0 \cdot D1 \cdot D2 \\
EP3 &= LA_{\text{in}} \cdot D0 \cdot D1 \cdot D2 \cdot D3 \\
EP4 &= LA_{\text{in}} \cdot D0 \cdot D1 \cdot D2 \cdot D3 \cdot D4 \\
EP5 &= LA_{\text{in}} \cdot D0 \cdot D1 \cdot D2 \cdot D3 \cdot D4 \cdot D5 \\
EP6 &= LA_{\text{in}} \cdot D0 \cdot D1 \cdot D2 \cdot D3 \cdot D4 \cdot D5 \cdot D6 \\
EP7 &= LA_{\text{in}} \cdot D0 \cdot D1 \cdot D2 \cdot D3 \cdot D4 \cdot D5 \cdot D6 \cdot D7
\end{align*}
\]
4.3 Operation of the PR Macro cell

In the PR macro, during the precharge phase of the clock, all the output bits EP0–EP7 are predischarged to logic low state, via p-type transistors mp0–mp7. When the clock signal becomes high, the circuit enters the evaluation phase and the outputs are evaluated according to the inputs present, in accordance with the design equations, given above. As a result, only one of the output bits switches to the high state, while the other bits assume the same previous state. In the priority resolver macro, LA_in acts as the look-ahead or enable signal for this stage, which forms the first level look-ahead, while LA_inter acts as the look-ahead signal for the next higher stage, which is an internal signal for a higher order circuit. This forms the second level look-ahead function and is described by the equation,

\[
\text{LA\_inter}=D_0.D_1.D_2.D_3.D_4.D_5.D_6.D_7 .\text{LA\_in}
\]  

(2)

4.4 8-bit Incrementer/Decrementer Macro cell

The operation of the Incrementer/Decrementer circuit is explained in detail and the complete block diagram for the 32-bit bit-width is available in [1]. The circuit, when incorporating the proposed DM block, results in greater power savings and area efficiency, as demonstrated by the simulation results, obtained using Mentor Graphics design tools.

5. Simulation results

\[
\text{Fig.8 : Waveform corresponding to Critical Path}
\]

Table 1: Post-Layout performance comparison

<table>
<thead>
<tr>
<th>32 bit DM macro cell</th>
<th>Critical Path Delay (ns)</th>
<th>Max. Freq. (MHz)</th>
<th>PDP</th>
<th>Device Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS</td>
<td>4.98</td>
<td>100.40</td>
<td>0.42</td>
<td>372</td>
</tr>
<tr>
<td>HSLP</td>
<td>4.11</td>
<td>121.65</td>
<td>0.17</td>
<td>396</td>
</tr>
<tr>
<td>PPR</td>
<td>3.99</td>
<td>125.31</td>
<td>0.11</td>
<td>322</td>
</tr>
</tbody>
</table>

Table 2: Post-layout Performance comparisons

<table>
<thead>
<tr>
<th>32 bit Inc./Dec. designs</th>
<th>Max. Freq. (MHz)</th>
<th>Power Dissipation (mW/MHz)</th>
<th>PDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS version</td>
<td>118.54</td>
<td>0.108</td>
<td>0.91</td>
</tr>
<tr>
<td>HSLP version</td>
<td>145.61</td>
<td>0.076</td>
<td>0.52</td>
</tr>
<tr>
<td>PPR version</td>
<td>158.79</td>
<td>0.051</td>
<td>0.32</td>
</tr>
</tbody>
</table>

6. Conclusion and Ongoing work

A novel topology for the 8-bit Decision Module macro cell is presented in this paper. The proposed design is especially suitable for realizing higher order Incrementer/Decrementer circuits. The 32-bit Incrementer/Decrementer
circuit, based on the proposed DM cell was designed in MOSIS 3V, 0.6µm CMOS technology on a Sun Solaris platform using an industry standard BSIM device model. The simulation results are very encouraging and they report significant savings in power dissipation and area occupancy, with simultaneous minimal improvement in speed performance.

Many higher order Incrementer/Decrementer circuits are also being designed based on the proposed strategy, to evaluate the feasibility and highlight the efficacy of the proposed design strategy.

Acknowledgement
The authors wish to thank the higher authorities and the faculty of the ECE department of their institution for their support and encouragement.

References: