

# A 2.5V 6.4mW 10-bit 140MS/s Digital-to-Analog Converter with Improved Current Mirror

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**Abstract:** - A 10-bit 140MS/s digital-to-analog converter (DAC) with improved current mirror is presented. In order to improve the resolution of a 10-bit DAC, a segmented decoding plus R-2R architecture will be introduced. DAC system modeling shows that the dynamic performance of the DAC is strongly dependent on the output impedance of DAC current source. The gain-boosting technique is applied to increase the output impedance of DAC current sources. It has been fabricated in a CMOS 0.35um 2P4M technology and the chip area with PADS is  $0.996 \times 1 \text{ mm}^2$ . The measured differential nonlinearity and integral nonlinearity of the DAC are  $\pm 0.8 \text{ LSB}$  and  $\pm 0.8 \text{ LSB}$ , respectively. The power dissipation is 6.4mW under 140MS/s clock rate at 2.5V supply voltage.

**Key-Words:** - DAC, segmented decoding structure, R-2R architecture, current mirror, low power

## 1 Introduction

The high-speed and high-accuracy DAC is one of the most crucial building blocks in the data communications, such as scanning graphic systems, computer systems, and digital TV. Particularly, on chip high-speed high-resolution DAC based on the same CMOS process as digital circuits are essential for system applications such as VDSL, WLAN, and GSM. (one more sentence)

The R-2R ladder DAC network requires less area at the expense of glitch-suffered structure. The segmented matrix DAC exhibits better performance with the penalty of area-consumed switches. To compromise this trade-off without corrupting the DAC resolution, a segmented DAC for 4 MSBs combines with an R-2R ladder network for 6 LSBs is presented to achieve a 10-bit 140MHz clock rate DAC.

The presented DAC consists of a current-cell matrix for 4 MSBs and a binary-weighted array for 6 LSBs to achieve high linearity. The linearity of the switches, which are used in the current cell, is improved by an extra dummy switch added each. To suppress the glitch energy, the thermometer decoding is adapted to reduce the switching times.

In section II, the architecture of the DAC is described. The circuit design is depicted in section III. In section IV, the measurement results are discussed. And a conclusion is given in section V.

## 2 Architecture

The presented DAC consists of a segmented matrix for upper bits and an R-2R ladder network for lower bits, as shown in Fig. 1. Since a great number of switches and decoding logic are required, which

consumes chip area and extra decoding delay, for the segmented matrix, an R-2R approach is adopted for the lower 6 digital bits. In the segmented matrix, the glitch energy can be attenuated due to dummy switches are applied in the current sources. Moreover, the LSB current sources will be turned on/off individually in each code transition because the thermometer decoding is employed. The resulted DNL of the presented DAC can be hence improved. In the R-2R ladder network, a smaller consumed area and a less delay are achieved due to few switches needed and no decoding logic is required.

The DAC architecture is shown in Fig.1 which is based on a segmented structure with four MSBs, and six LSBs. The MSBs is thermometer decoder and each drives 15 equal current sources. The LSBs are binary weighted. A bank of latches and switch drivers are used to synchronize the data prior to the current sources for improving switching performance.

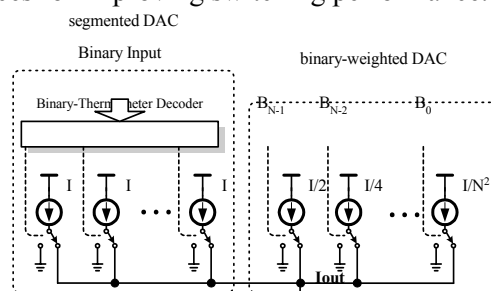


Fig. 1 Block diagram of the D/A converter

## 3 Circuit Design

In this section, the key circuit which was used to implement a 10-bit DAC will be described. These

circuits include a present current mirror with r-2r circuit, a current cell switching with deglitch circuit, and a decoding with segment array.

### 3.1 The Current Mirror with R-2R Circuit

The presented high accurate current mirror as shown in Fig. 1. It is based upon the gain-boosting circuit to improve the output impedance and also to improve the current accuracy of the current mirror. A novel feedback gain stage is used to increase the output impedance and matching accuracy significantly. Moreover, the presented new current mirror also has output swing similar as the traditional two-stage cascode current mirror [1 - 2].

In the presented current source, the MOS transistors M1 – M4 are used as a two-stage cascode current mirror, and the amplifier consists of M6, and M9, which provide a negative feedback to stable the output node voltage. The addition of this amplifier ideally increases the output impedance.

$$R_{out} = g_{m1} r_{ds1} r_{ds2} (1 + A) \quad (1)$$

This R-2R ladder DAC has only one negative-feedback amplifier structure, consisted in MSB, used to improve match accuracy and output impedance in six current mirror circuits. All of the current source circuits owned the only one negative-feedback amplifier circuit jointly, not only match the accuracy current-source, but also reduce the power dissipation and layout area.

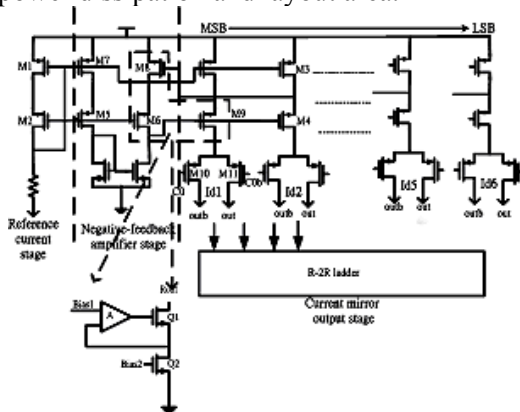


Fig. 2 Current Mirror with R-2R

### 3.2 Current Cell Switching and Deglitch Circuit

In the current cell switching, the differential switches reduce the output glitch and improve the settling time. At the same time, latches or some types of re-timing logic are required on the output of the decoding logic for the MSB thermometer code because different delays paths result in skewed arrival times at the switches. [4]

In this design, the latch circuit is into a single circuit as shown in Fig. 3. The switching level C0 and C0b are applied to M1 and M2 gates by means of two identical

stages S1 and S2 that are controlled by complementary signals. These stages have been scaled so that the output currents out and outb vary symmetrically during the switching of the cell. With a conventional drive circuit which generates symmetrical signals for C0 and C0b as shown in Fig. 4. [5] Both switching transistors are nearly off at the time, leading to an overshoot on one of the output. In this design, the low logic threshold of the driving stages delays the turning off of the current switch. The output waveforms C0 and C0b are overlap at higher level and the glitch of the output is reduced.

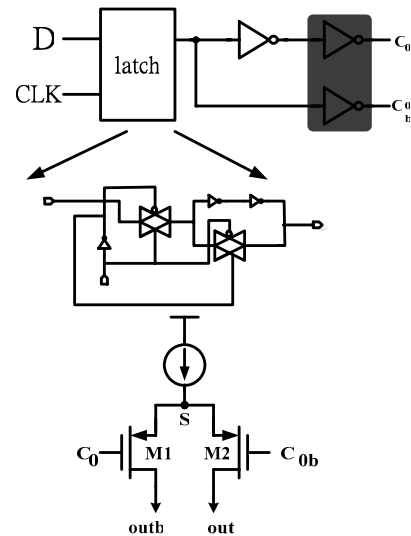


Fig. 3 Current Cell Switch

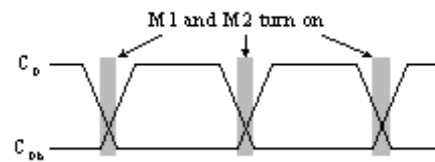


Fig. 4 The deglitch waveform of C0 and C0b

### 3.3 Decoding and Segment Array

A thermometer decoder is used for the higher four bits whereas each LSB bit directly controls one of the weighted cells. The decoder is made of 15 blocks. The output of a block is active if the input of the decoder is greater than or equal to its programmed value. Consequently as the input code increases on the 4MSBs, successive non-weighted cells turn on one by one. There are several advantages to this decoding scheme. First, it has the advantages of the higher speed due to the parallel input. Second, lower glitch energy because a minimal number of current units would switch activity for each D/A converter transition. The MSB segment cell is Q<sup>2</sup> Random as shown in Fig. 5. [3]

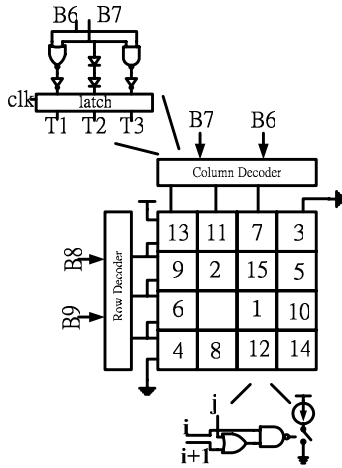


Fig. 5 The Segment Cells

### 3.4 DAC Implementation

The presented 10bits 140MHz DAC is implemented in a 0.35 double-poly four-metal CMOS process. The DAC chip micrograph is shown in Fig. 6 and the total chip area is 0.996 mm<sup>2</sup>. The DAC achieves the reasonable static and dynamic performance by being layout with the following considerations: First, fixed-biased narrow poly lines, laid out at both sides of current sources, minimize current mismatches. Second, separate power supplies for analog and digital blocks to reduce noise coupling.

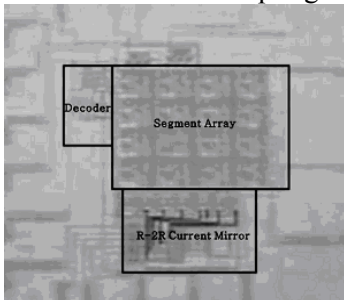


Fig. 6 The DAC Chip Micrograph

The transient time at this DAC step response is shown in Fig. 7. The settling time of this DAC could converge in 6.5ns so the DAC could operate at 140M sample/s.

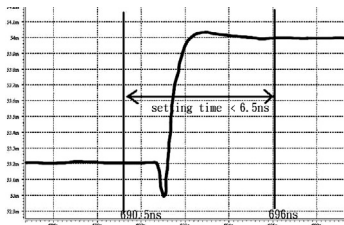


Fig. 7 settling time

## 4 Measurement Results

The measured DNL and INL data are shown in Fig. 8 and Fig. 9. The DNL is between +0.75LSB

and -0.8LSB. The INL is between +0.7LSB and -0.8LSB.

Table I. summarizes the measured performance of the presented DAC.

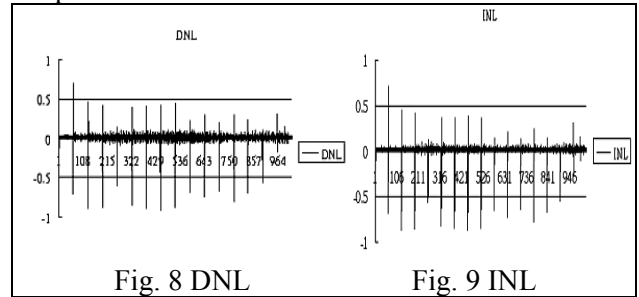


Table 1 Summary of the presented D/A converter

Supply voltage	2.5V
Resolution	10Bit
Update Rate	140MS/s
Full-scale output	1.6V/160uA
INL	± 0.8LSB
DNL	± 0.8LSB
Core Size of the Chip	0.996x1 mm <sup>2</sup>
Power @ 2.5V supply	6.4mW
Technology	0.35um CMOS

## 5 Conclusion

In this paper, the architecture and circuit approach to implement a 140MS/s, 10-bit DAC were presented. In detail, the segment array plus R-2R architecture, decoding logic, switch driver circuits and the gain-boosting current source arrays were applied to 10-bit DAC design. DAC system modeling showed that the dynamic performance of current-mode DACs is strongly contingent on the output impedance of DAC current sources. The gain-boosting current source satisfies the requirement of the unit current source impedance for 10-bit DAC. Measurement results demonstrate that these techniques are capable of achieving the performance of 140MS/s, 10-bit DAC.

### References:

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