Novel Frequency Doubler Circuits and Dividers Using Duty Cycle Control Buffers

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Abstract: - Novel frequency doubler circuits and dividers for clock signal generation are presented. In combination with two edge detectors and two duty cycle control buffers a low cost frequency doubler circuit is achieved as compared to Phase-Locked Loop (PLL) design. An input clock signal with an unpredictable duty cycle is inputted to a rising (or falling) edge detector. The edge detector converts the positive (or negative) transitions to a one shot pulse train whose frequency is the same as that of the input clock. However, the one shot pulse train has its duty cycle far less than 50%. By a first 50% duty cycle control buffer the output waveform of the resulted clock signal is symmetrical. The output of the first-stage duty cycle buffer is then edge detected by a rising and falling edge detector, so that the resulted one shot pulse train has twice the frequency of the incoming 50% duty cycle signal. Finally, the second one shot signals are duty cycle adjusted in the second-stage duty cycle control buffer, to restore its 50% duty cycle. Therefore, two times frequency multiplication is achieved with low cost as compared to Phase-Locked Loop (PLL) design. Furthermore, a novel design approach for frequency dividers using duty cycle control circuit is also demonstrated. Simulation results for both frequency multiplication and division confirm the validity of the proposed design approach.

Key-Words: - Frequency doubler, Dividers, Phase-locked loop, Duty cycle, XOR, Edge detector

1 Introduction

Phase-locked loop (PLL) circuits are well known and are often used for frequency multiplication purposes [1]--[6]. The main components of a PLL circuit comprise a phase detector, a loop filter (LPF) and a voltage-controlled oscillator (VCO). As shown in Figure 1(a), a PLL circuit is incorporated to generate an output clock signal (2f) at twice the frequency of the input clock signal (f). To ensure the 50 percent duty cycle of the output clock signal further frequency multiplication is needed. Therefore, both divide-by-4 and divide-by-2 counters have to be included in the closed feedback loop. While the PLL design approach offers flexibility for frequency multiplication, it does have at least two significant disadvantages: (1) increased power consumption due to the VCO operation at 4X frequency; and (2) complex analog design of the VCO circuit, including techniques for reducing power noise and frequency jitter.

Various types of improved VCO circuits have been disclosed in the literature. For example, a multi-stage ring oscillator with ring trip-point compensation is used to control the duty cycle of the VCO output [7]. Furthermore, a VCO circuit is disclosed which uses current mirrors to generate 50 percent duty cycle output which is derived directly from the VCO frequency [8], [9]. Therefore, there is no need to operate the VCO at 4 times the frequency of the input clock signal, as in the prior art circuit shown in Figure 1(a). This improved VCO can be used in a 2X PLL circuit, as shown in Figure 1(b). While the operating frequency of this VCO circuit has been reduced to half the frequency of the prior art circuit shown in Figure 1(a), the VCO circuit design is more complex and challenging.

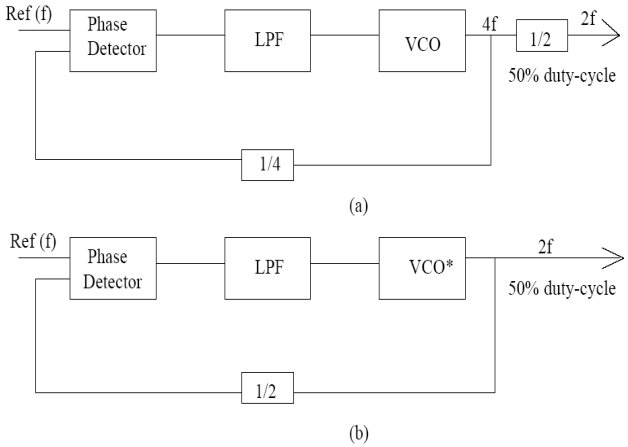


Fig. 1 Prior art (a) Phase-locked loop (b) Modified PLL with improved VCO design.

Still another conventional method to double the incoming clock frequency is through the use of an XOR gate. The XOR gate has its first input connected to an incoming signal stream and its second input connected through a delay element to the same incoming stream, as shown in Figure 2. If the input to such a circuit is a 50 percent duty cycle clock, the output will be a clock at twice the input frequency. However, the duty cycle of this output frequency can vary between 20 percent and 80 percent. For example, if the delay element provides a delay which is nominally 40 percent of the output clock period, the process variations in manufacturing the delay element will result in a delay which is as small as one half (20%), or as large as two times (80%), the nominal 40 percent delay. A 20 percent worst case duty cycle clock is unacceptable for most applications and effectively prohibits further multiplication. Therefore, there is still a need for a simplified and improved circuit and method for frequency multiplication with equalized duty cycle output.

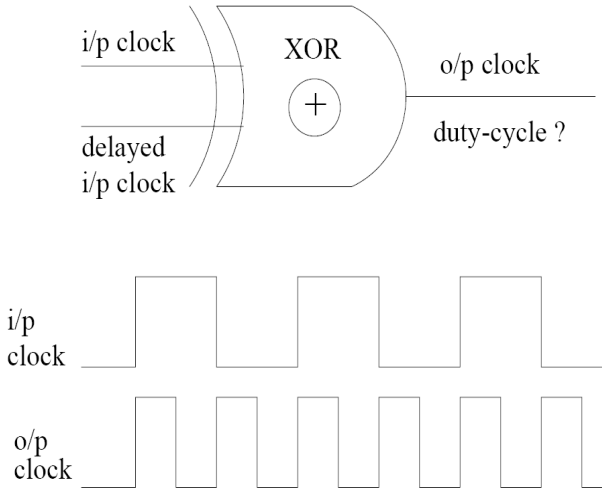


Fig. 2 Traditional frequency multiplication method by XOR gate.

2 The Proposed Circuits

Figure 3(a) shows the first proposed 2X frequency multiplication circuit. The proposed whole circuit consists of two edge detectors and two duty cycle control buffers. An input clock signal (f) with an unpredictable duty cycle is inputted to a rising (or falling) edge detector. The edge detector converts the positive (or negative) transitions to a one shot pulse train whose frequency is the same as that of the input clock. However, the one shot pulse train has its duty cycle far less than 50%. By a first 50% duty cycle control buffer the output waveform of the resulted clock signal is symmetrical. The output of the first-stage duty cycle buffer is then edge detected by a rising and falling edge detector, so that the resulted one shot pulse train has twice the frequency of the incoming 50% duty cycle signal. Finally, the second one shot signals are duty cycle adjusted in the second-stage duty cycle control buffer, to restore its 50% duty cycle. Further detailed operations can refer to Figure 3(b) for illustration.

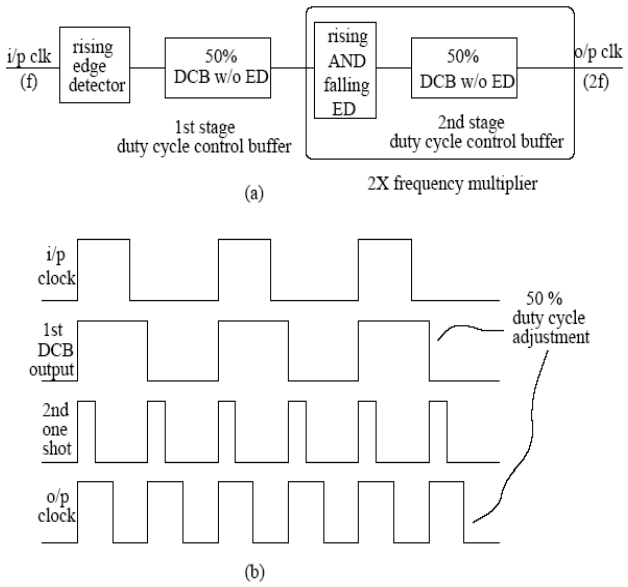


Fig. 3 (a) Proposed novel frequency doubler circuit using duty cycle control buffer (b) Timing diagram.

As for the circuit structure of the duty cycle control buffer without edge detector (DCB w/o ED) it is shown in Figure 4. This duty cycle control buffer consists of a monostable trigger, an inverter, an integrating circuit and an OPAMP. The detailed circuit descriptions are given in [10]. In brief, this duty cycle control buffer automatically adjusts the duty cycle of an input clock signal via a closed loop function. The desired duty cycle value is determined by the reference voltage Vref, which may be obtained by a bandgap voltage reference circuit.

If the input clock signal is a symmetrical square wave, that is, 50 percent duty cycle, the 2X frequency multiplier can be used directly. For general system applications an on-chip crystal oscillator is used for clock signal generation. In such cases, a clock generation circuit for approximately 50 percent duty cycle output is suggested, as shown in Figure 5. Since the output signals X1 and X2 from the on-chip crystal oscillator are always out of the same phase, a differential amplifier is carefully incorporated here to generate approximately

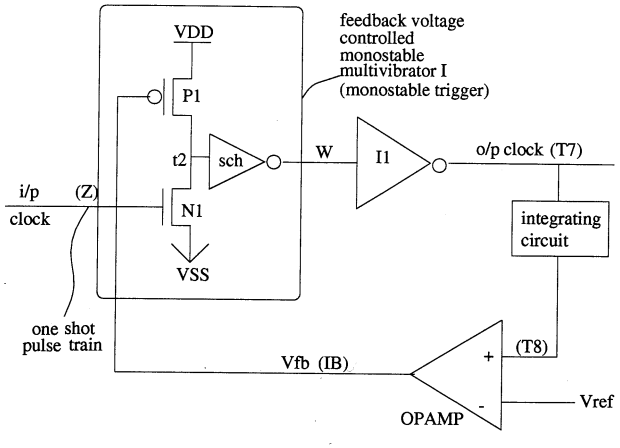
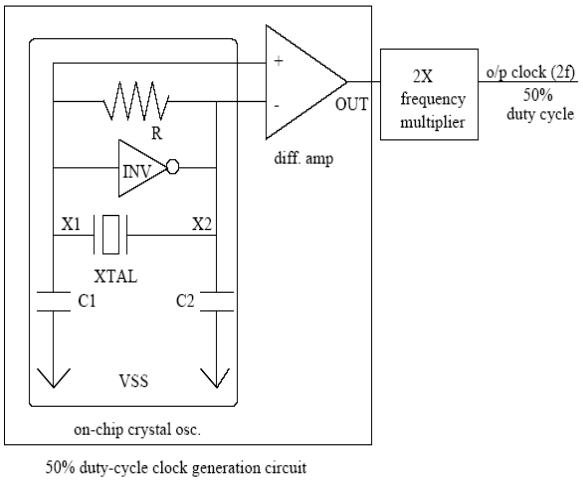


Fig. 4 Proposed "Precharged Low" type duty cycle control buffer [10].

equal duty cycle output. The suggested 2X frequency multiplier is simple in its design and therefore low cost in terms of implementation.



50% duty-cycle clock generation circuit

Fig. 5 Suggested 2X frequency multiplier in combination with an on-chip crystal oscillator

3 Frequency Dividers

For general applications of IC design or digital signal processing it is desirable that the clock signal is a symmetrical square wave with 50 percent duty cycle. However, in some situations, the operation of frequency division for clock signals is required. Under this condition, a novel design approach for frequency dividers is proposed in Figure 6.

The complete frequency divider consists of a finite state machine and a 50 percent duty cycle control circuit. Note that an edge detector is not needed in this duty cycle control circuit. This finite

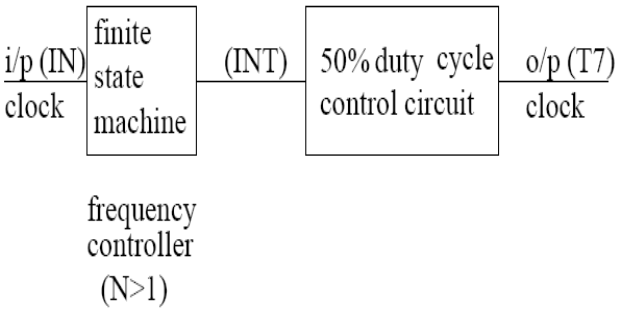


Fig. 6 Novel frequency divider applications.

state machine is actually a frequency controller. As shown in Figure 6, by selecting a desired value of N, the finite state machine output signal (INT) will have a frequency equal to the input frequency f divided by N. This divide-by-N signal is then 50% duty cycle adjusted. Therefore, the final clock signal (T7) has its frequency divided by N with symmetrical waveforms. The used finite state machine can be simply implemented by a simple modulo N circuit along with some control logic, as shown in Figure 7. Based on this novel design criterion, any clock signal of both divided frequency and 50% duty cycle can be easily obtained as compared to other complex digital design approach [11].

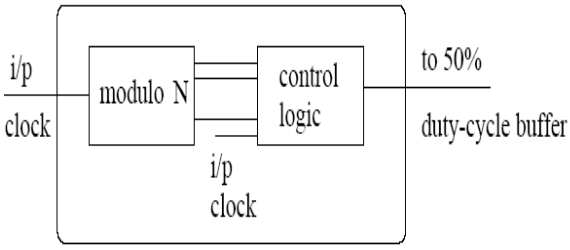


Fig. 7 Finite state machine by modulo circuit.

4 Results and Discussions

Simulation results of the proposed frequency doubler circuit (2X) are shown in Figure 8. The input clock signal IN has its frequency of 20MHz. This input clock signal is first 50 percent duty cycle adjusted, as indicated by T7. This clock signal of equal duty cycle is then frequency multiplied by 2 to obtain the final 40MHz output with 50 percent duty cycle, as represented as OUT. For this 2X frequency multiplication purpose, totally two duty cycle control buffer circuits are required. As for the simulations results of the duty cycle control buffer they have been presented in Reference [10], along with the operational advantage over prior art circuits.

In brief, the loop stability of the proposed circuit is superior over the prior art. Besides, the design complexity is greatly reduced compared to a PLL design since a duty cycle control buffer needs 32 MOS transistors only. Furthermore, the total power consumption can therefore be effectively reduced.

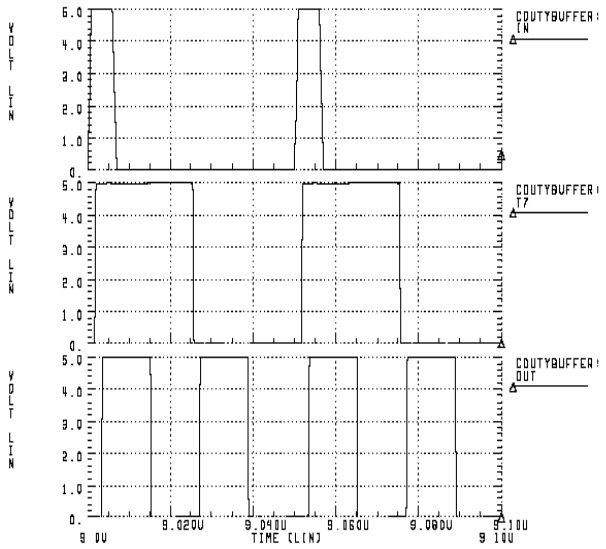


Fig. 8 Simulation results of the proposed frequency doubler circuit for input at 20Mhz.

As compared to the prior art such as a PLL, three main advantages may be summarized as follows: (1) less design complexity, as compared to the VCO design requirements of the PLL circuit; (2) equalized duty cycle output, which makes additional frequency multiplication feasible; and (3) less jitter problem, since noise from the power or ground line only affects the one shot pulse train signals, but does not change their frequency.

The suggested clock generation circuit for equalized duty cycle output is further simulated in Figure 9 for input at 20MHz. The oscillating signal at node X1 is usually a pure sine waveform with its frequency equal to the frequency of the used crystal. Moreover, since the amplifier is self-biased at VDD/2 (offset) by a self-bias resistor its waveform can be described as V(X1)=VDD/2 + Vswing*sin(f). Vswing is the amplitude of X1 signal and its value may depend on the frequency of the crystal, values of loading capacitors, gain of the amplifier and the operating voltage. As the sine signal is applied at X1, a square wave signal will be generated at X2 if the gain of the amplifier is large enough. Once these two out-of-phase signals X1 and X2 are generated, they are applied to both positive and negative input terminals of a differential amplifier to obtain an output clock signal OUT. Simulation results considering Vswing as small as 0.5V are shown for reference (VDD=5V). The resulted signal OUT has its duty cycle approximately equal to 50 percent as described before. Therefore, the proposed 2X frequency multiplier can advantageously combine the suggested on-chip crystal circuit for higher frequency clock signal generation with least cost.

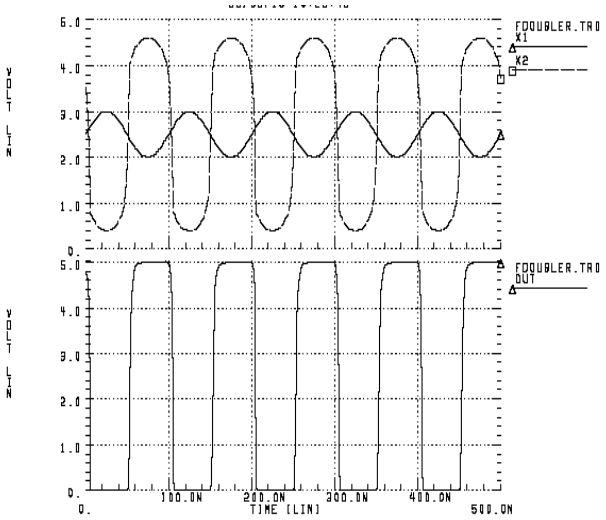


Fig. 9 Simulation results of suggested 50% duty cycle clock generation circuit for input at 20MHz.

Importantly, a duty cycle control circuit can also be applied to a frequency divider when combined with a finite state machine in the input stage. As shown in Figure 10, by selecting a desired value of 3, the finite state machine output signal (Z or INT) will have a 1/3 frequency of the input frequency f. This divide-by-3 signal is then 50% duty cycle adjusted. Therefore, the final clock signal (Zout or T7) has its frequency divided by 3 with symmetrical waveforms. Note that the original clock signal (INT) has its duty cycle of 1/6. Figure 11 illustrates simulation results of this divide-by-3 example.

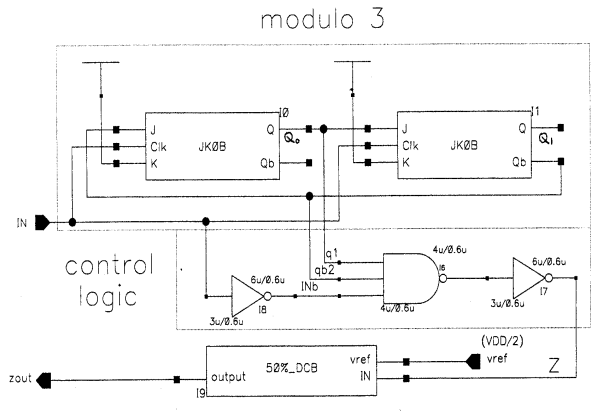


Fig. 10 Design example of divide-by-3.

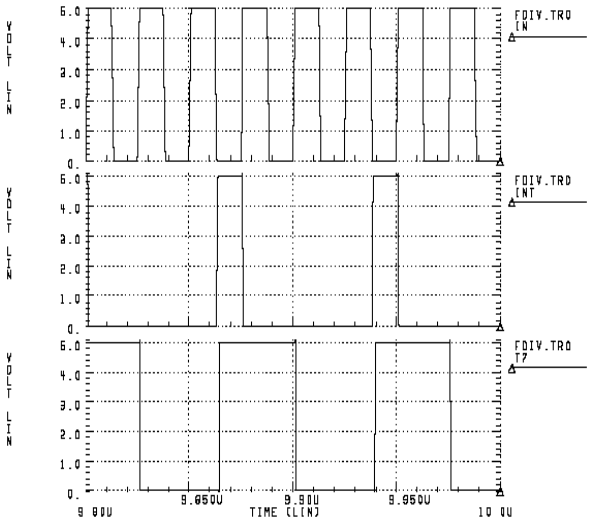


Fig. 11 Simulation results of divide-by-3 example with 50% duty cycle output.

5 Conclusion

In this paper, frequency multiplication circuits and dividers using duty cycle control buffers have been demonstrated for clock signal generation, which feature simple design, low cost and reduced power. According to simulation results the proposed circuit is effective in generating clock signal of higher frequency. In combination with an on-chip crystal oscillator this disclosed frequency doubler circuit can be used directly. This reason enables the inventive circuit very suitable for general integrated circuit applications. Moreover, novel frequency dividers by a duty cycle control buffer have also been illustrated.

References:

[1] R. E. Best, Phase locked loops, McGraw Hills, 1984.

[2] I. A. Young et al., A PLL clock generator with 5 to 110 MHz of lock range for microprocessors, *IEEE J. Solid-State Circuits*, Vol. 27, 1992, pp. 1599-1607.

[3] D.-L. Chen, Designing on-chip clock generators, *IEEE Circuits and Devices Magazine*, 1992, pp. 32-36.

[4] T. Olsson and P. Nilsson, A digitally controlled PLL for SoC applications *IEEE J. Solid-State Circuits*, Vol. 39, 2004, pp. 751-760.

[5] R. F. Bitting and W. P. Repasky, A 30--128 MHz frequency synthesizer standard cell, *Proc. IEEE Custom Integrated Circuits Conf.*, 1992, pp. 24.1.1-24.1.6.

[6] D. Mijuskovic et al., Cell-based fully integrated CMOS frequency synthesizers, *IEEE J. Solid-State Circuits*, Vol. 29, 1994, pp. 271-280.

[7] R. R. Rasmussen, High frequency CMOS VCO with gain constant and duty cycle compensation, *US Patent 5,061,907*, Oct. 1991.

[8] A. H. Atriss et al., Voltage controlled oscillator having 50% duty cycle clock, *US Patent 5,081,428*, Jan. 1992.

[9] J. E. Gersbach et al., Ring oscillator circuit having output with fifty percent duty, *US Patent 5,485,126*, Jan. 1996.

[10] H.-C. Chow, Duty cycle adjusting circuit for clock signals, *WSEAS Transactions on Electronics*, Vol. 2, 2005, pp. 66-71.

[11] R. Shankar and A. S. Leno, N+1 frequency divider counter and method therefore, *US Patent 5,526,391*, June 1996.